



Education

PCI Express and Storage

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PCI Express and Storage

- ◆ System IO Architectures are changing to PCI Express, 10 GbE and InfiniBand. As IO Virtualization is being defined, shared IO infrastructures are on the horizon. This session discusses the impacts of all these changes on storage connectivity, storage transfer rates, as well as the implications to Storage Industry and Data Center Infrastructures. This tutorial will provide the attendee with:
 - ◆ Basic knowledge of PCI Express and System Root Complexes and IO Virtualization.
 - ◆ Anticipated Impacts (benefits and exposures) of these Technologies on Storage Environments.
 - ◆ IO Virtualization connectivity possibilities provided by PCI Express.

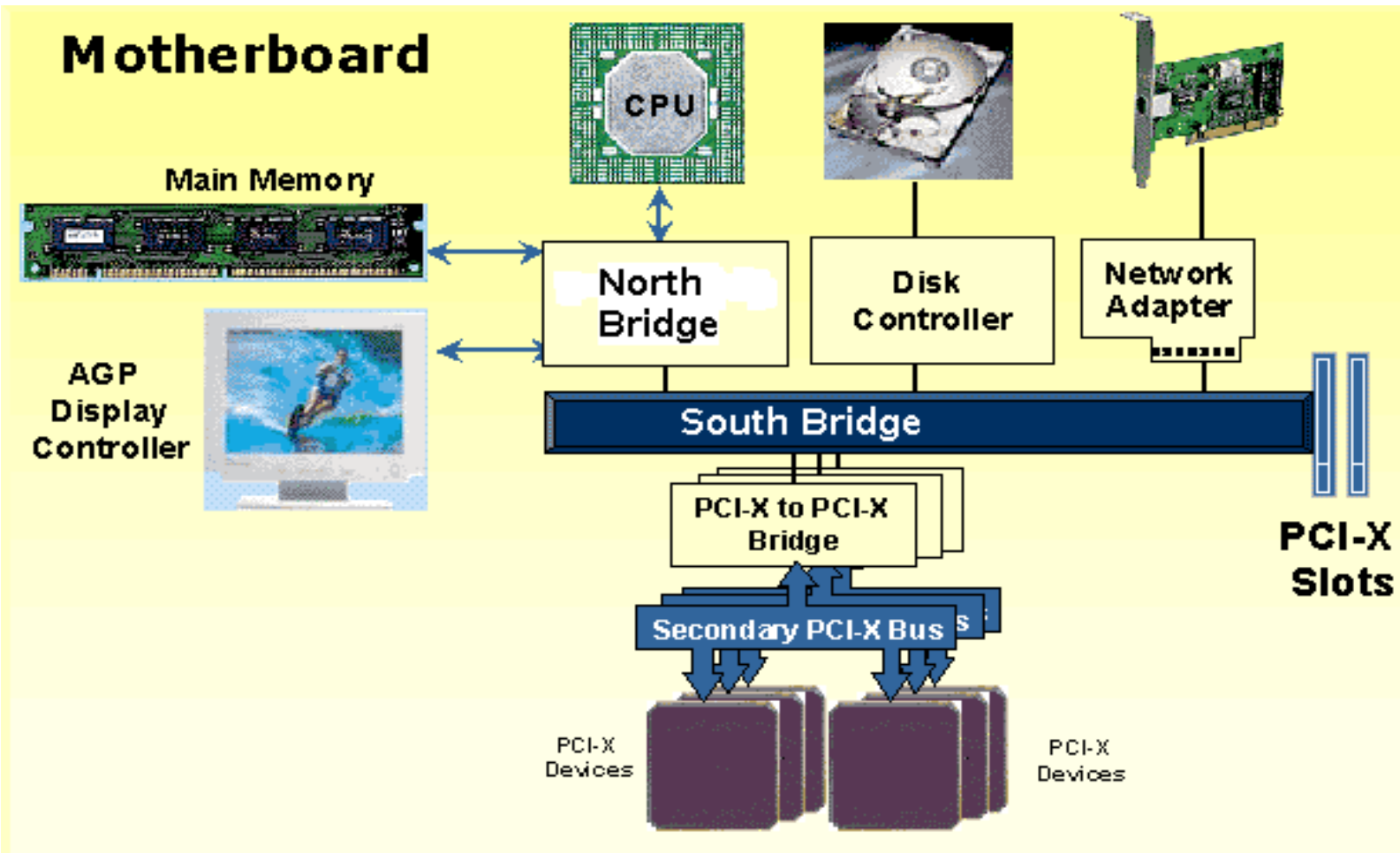
➤ IO Architectures

- ◆ PCI Changing to PCI Express
- ◆ PCI Express Tutorial
- ◆ New PCI Express based architectures
- ◆ How does PCI Express work

➤ IO Evolving Beyond the Motherboard

- ◆ Serial Interfaces
 - > InfiniBand, GbE & 10 GbE
 - > PCIe IO Virtualization
- ◆ Review of PCI Express IO Virtualization
- ◆ Impact of PCI Express on Storage

Typical PCI Implementation



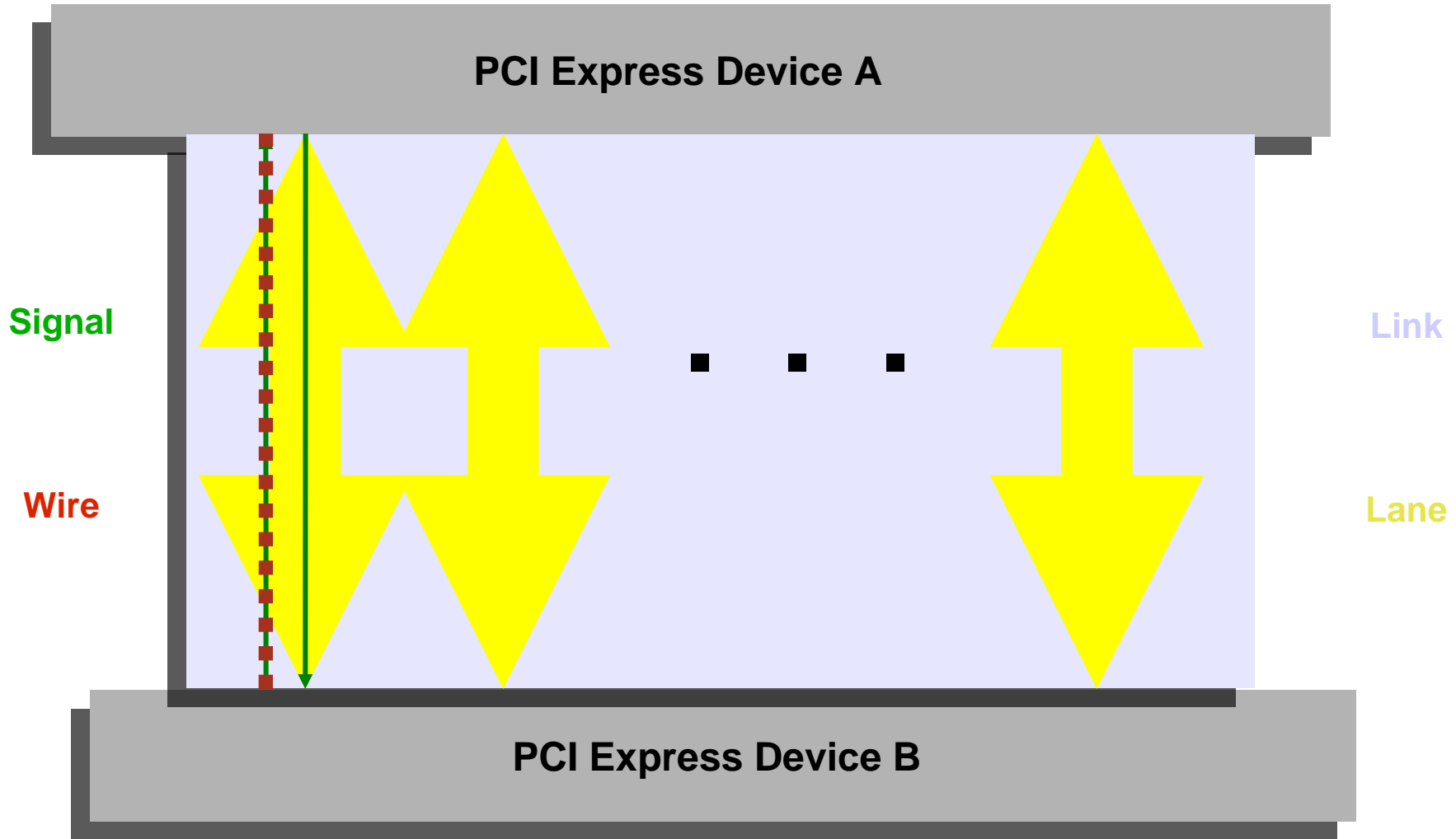
Changing I/O Architecture

- **PCI provides a solution to connect processor to IO**
 - ◆ Standard interface for peripherals – HBA, NIC etc
 - ◆ Many man years of code developed based on PCI
 - ◆ Would like to keep this software investment
- **Performance keeps pushing PCI speed**
 - ◆ Moved from 32bit/ 33Mhz to 64bit/ 66Mhz, then
 - ◆ PCI-X introduced to reduce layout challenges
 - > PCI-X 133Mhz well established
 - > Problems at PCI-X 266Mhz with load and trace lengths
- **Parallel interfaces gradually being replaced**
 - ◆ ATA to SATA (PATA is going away)
 - ◆ SCSI to SAS
- **Move parallel PCI to serial PCI Express**

PCI Express Introduction

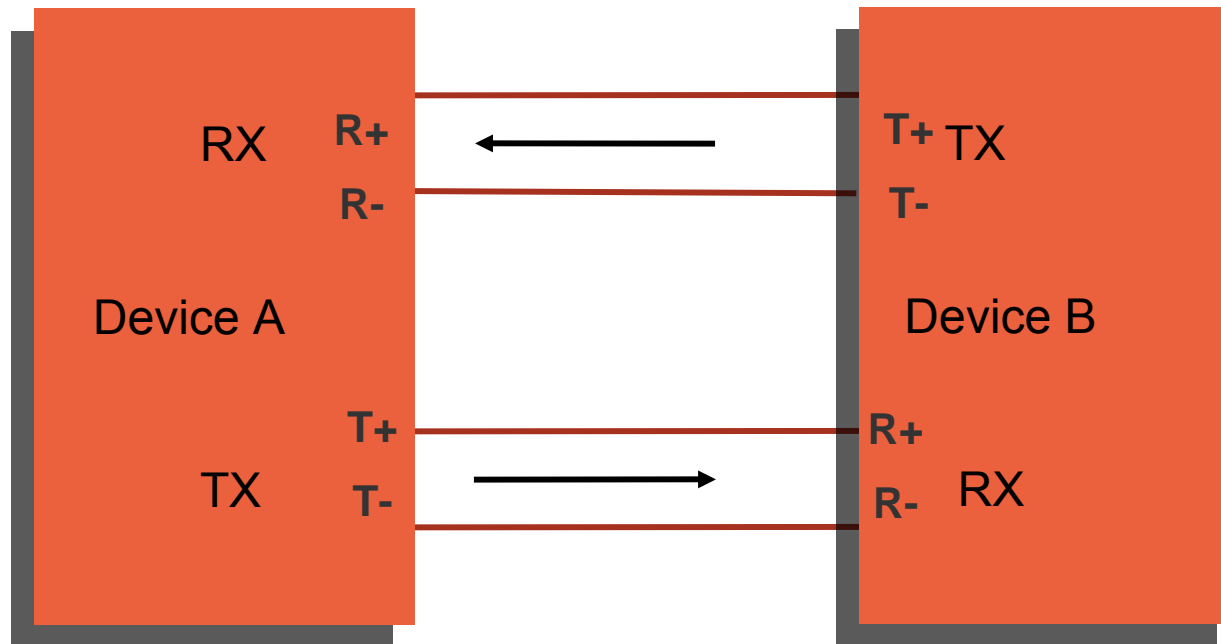
- PCI Express Architecture is a high performance, IO interconnect for peripherals in computing/ communication platforms
- Evolved from PCI and PCI-X™ Architectures
 - ◆ Yet PCI Express architecture is significantly different from its predecessors PCI and PCI-X
- PCI Express is a serial point- to- point interconnect between two devices
- Implements packet based protocol for information transfer
- Scalable performance based on the number of signal Lanes implemented on the interconnect

PCI Express Terminology



PCIe What's A Lane

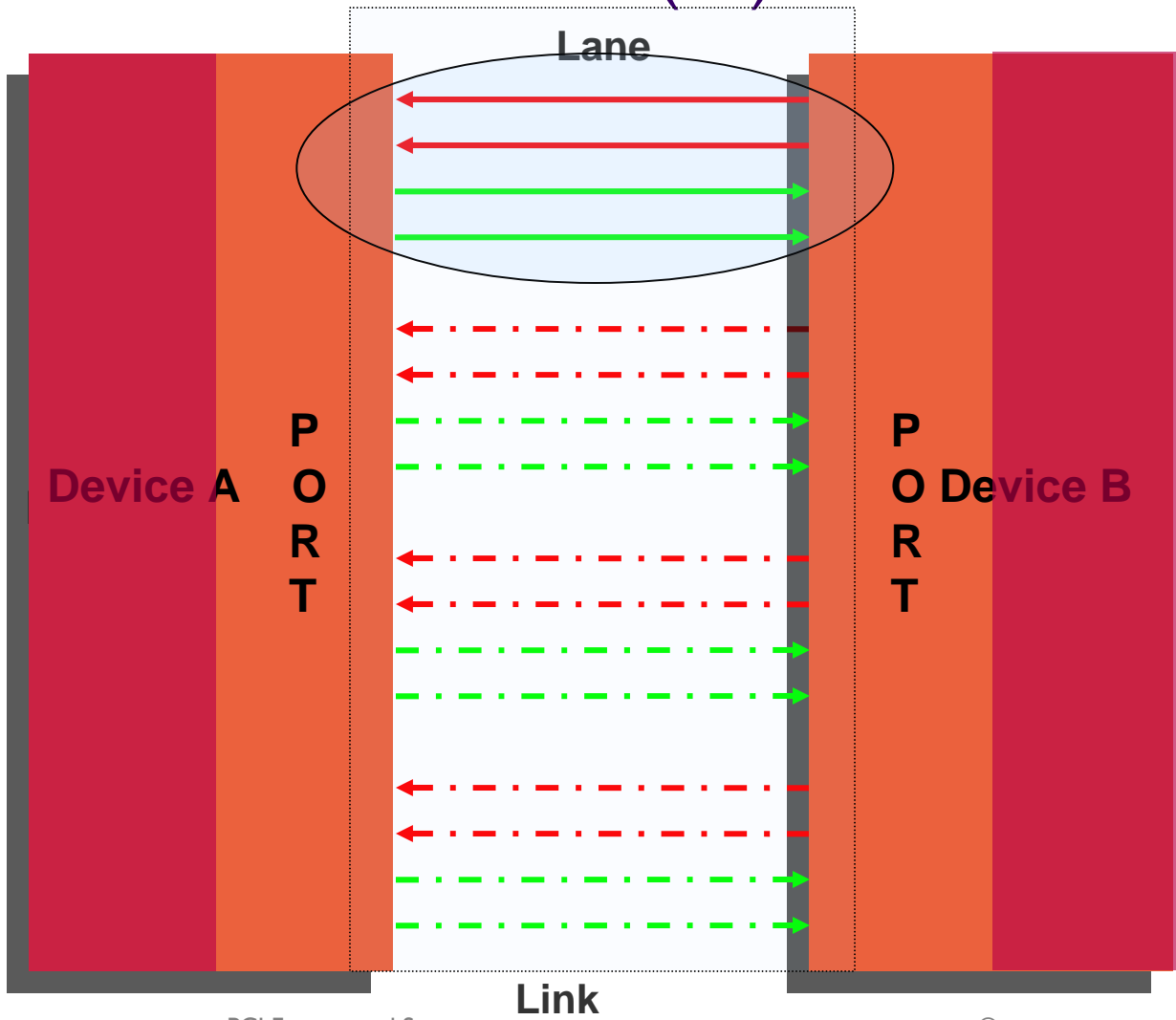
Point to Point Connection Between Two PCIe Devices



This Represents a Single Lane Using Two Pairs of Traces,
 TX of One to RX of the Other

PCIe – Multiple Lanes

Links, Lanes and Ports – 4 Lane (x4) Connection

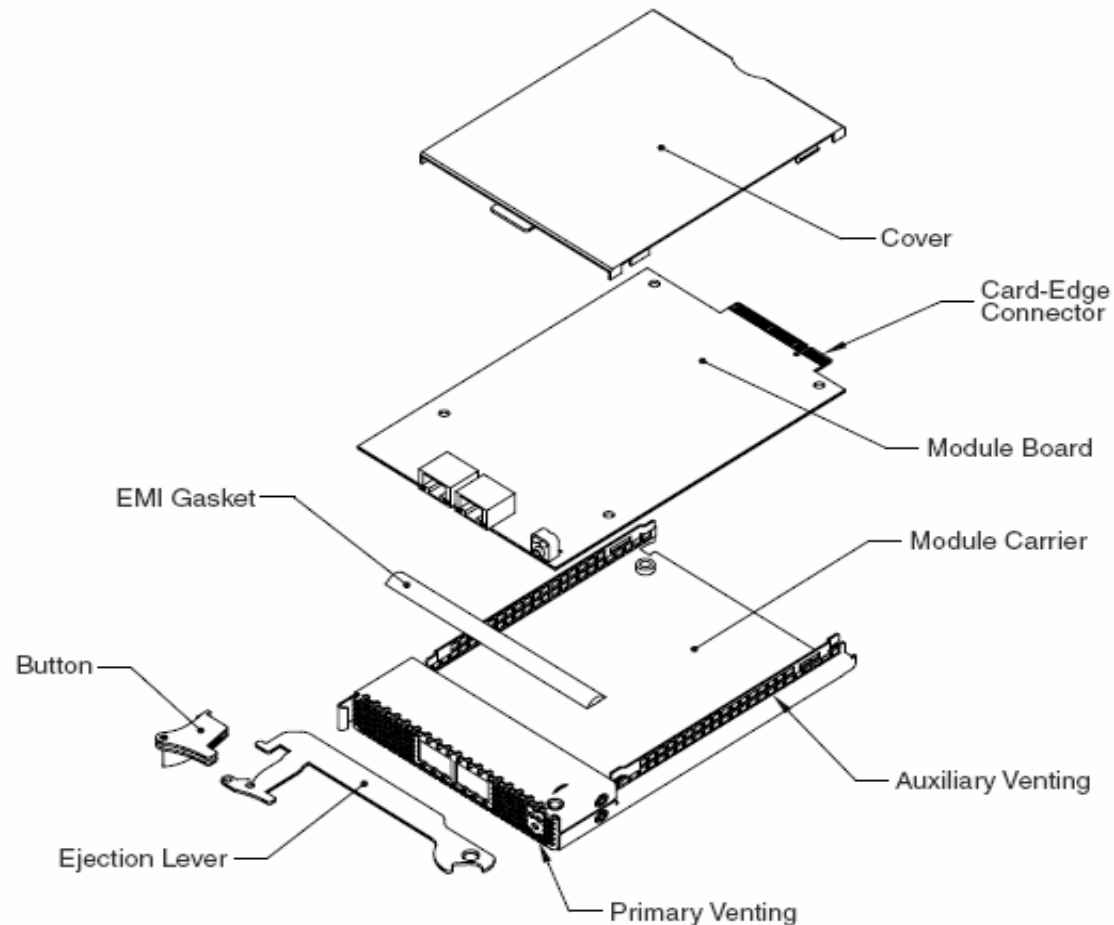


PCI Express Overview

- Uses PCI constructs
 - ◆ Same Memory, IO and Configuration Model
 - ◆ Supports growth via speed increases
- Uses PCI Usage and Load/ Store Model
 - ◆ Protects software investment
- Simple Serial, Point- to- Point Interconnect
 - ◆ Simplifies layout and reduces costs
- Chip- to- Chip and Board-to-Board
 - ◆ IO can exchange data
 - ◆ System boards can exchange data
- Receive and Transmit Lanes

Express Module (EM)

- ◆ **Developed by the PCI-SIG (Initially Server IO Modules)**
 - ◆ Fully compatible with latest PCI Express specification
 - ◆ Designed to support future generations of PCI Express
- ◆ **Adds the necessary Hot Plug hardware and software**
- ◆ **Commodity pricing model using standard PCI Express silicon and ½ size card**
- ◆ **PCIe EM Products available today providing:**
 - ◆ SAS Internal/ external
 - ◆ 4 Gb FC External
 - ◆ GbE External
 - ◆ 10 GbE External
 - ◆ IB External



Transaction Types

Requests are translated to one of four types by the Transaction Layer:

➤ Memory Read or Memory Write

- ◆ Used to transfer data to or from a memory mapped location. Protocol also supports a locked memory read transaction variant.

➤ IO Read or IO Write

- ◆ Used to transfer data to or from an IO location
- ◆ These transactions are restricted to supporting legacy endpoint devices.

Transactions Types (cont)

Requests can also be translated to:

➤ Configuration Read or Configuration Write:

- ◆ Used to discover device capabilities, program features, and check status in the 4KB PCI Express configuration space.

➤ Messages

- ◆ Handled like posted writes. Used for event signalling and general purpose messaging.

PCI Express Throughput

Link Width		X1	X2	X4	X8	X16	X32
Aggregate BW (Gbytes/s)	Gen1	0.5	1	2	4	8	16
	Gen2	1	N/A	4	8	16	32
	Gen3	2	N/A	8	16	32	64

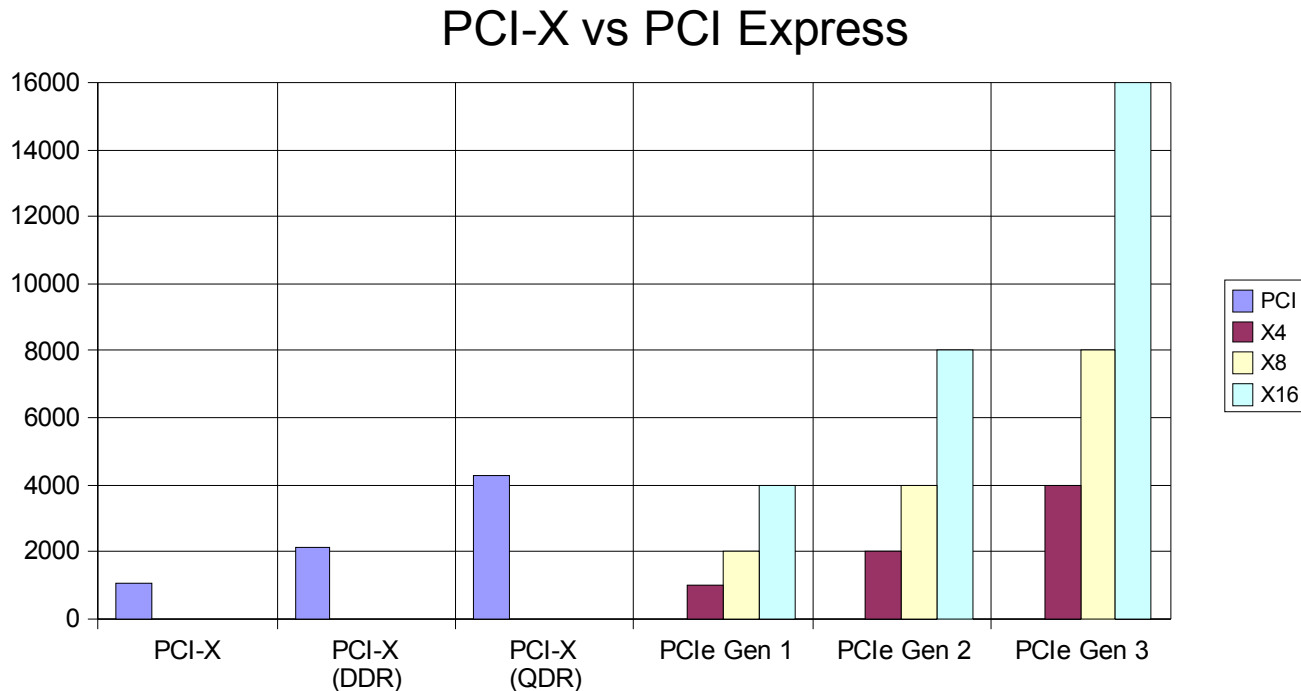
- Assumes 2.5 GT/ s signalling for Gen1
- Assumes 5 GT/ s signalling for Gen2
 - ◆ 80% BW available due to 8/ 10 bit encoding overhead
- Assumes 8 GT/ s signalling for Gen3

Aggregate bandwidth implies simultaneous traffic in both directions

Peak bandwidth is higher than any bus available

PCI-X vs PCI Express Throughput

How does PCI-X compare to PCI Express?

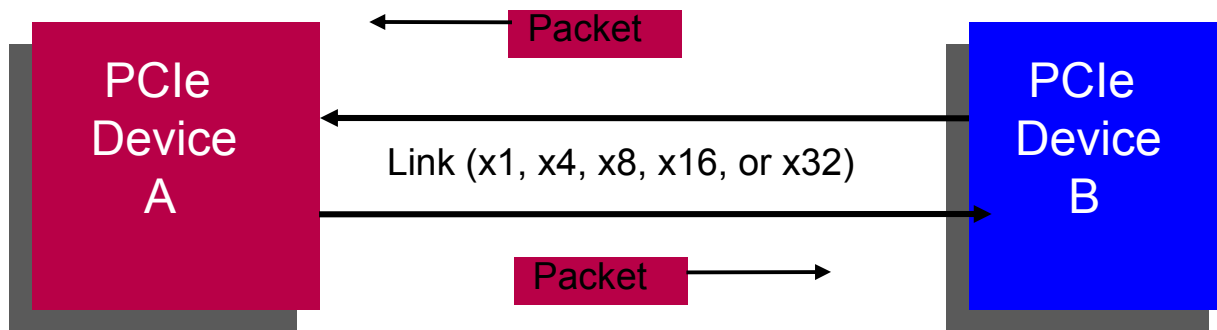


➤ PCI-X QDR maxs out at 4263 MB/ s per leaf

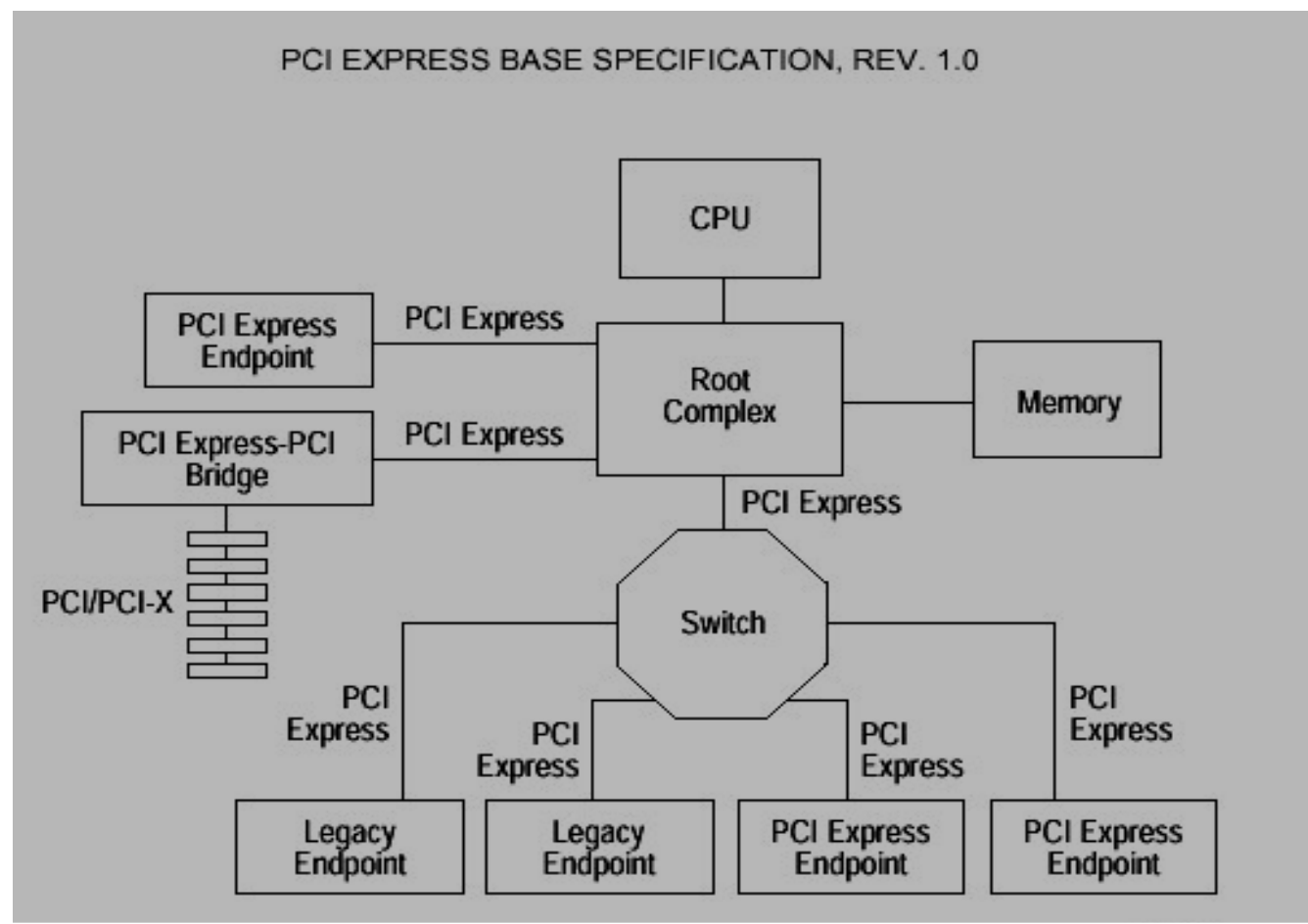
➤ PCIe x16 Gen1 maxs out at 4000 MB/ s

PCI Express Features

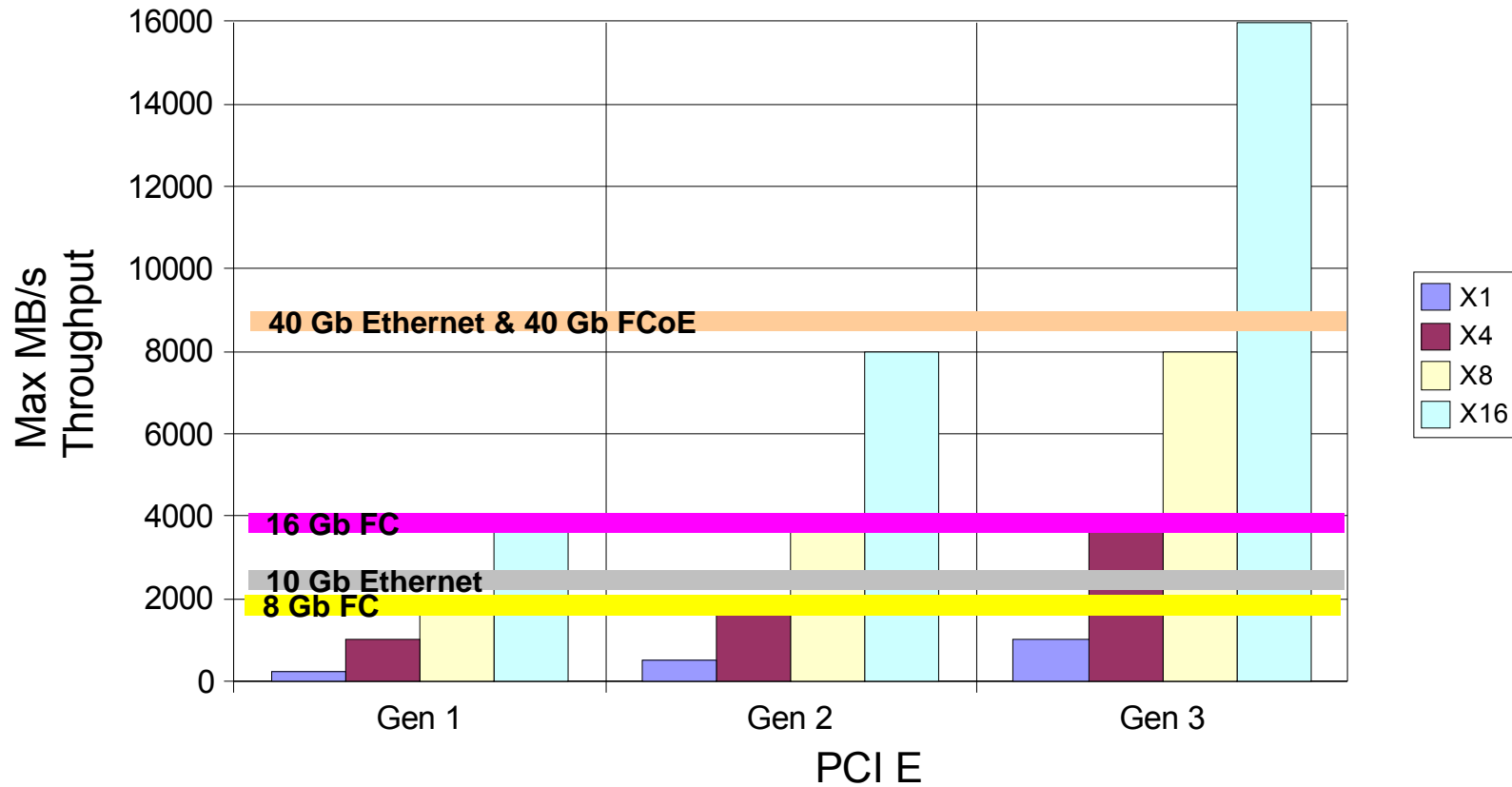
- Point- to- point connection
- Serial Bus means fewer pins (4 per lane)
- Scalable: x1, x4, x8, x16, x32 (x2 Gen I only)
- Dual Simplex connection
 - ◆ 50% of bandwidth in each direction
- 2.5 VGT/ s transfers/ direction/ s
- Packet based transaction protocol



Sample PCI Express Topology



PCI Express Bandwidth



Benefits of PCI Express

➤ Lane expansion to match need

- ◆ x1 Low Cost Simple Connector
- ◆ x4 or x8 PCIe Adapter Cards
- ◆ x16 PCIe High Performance Graphics Cards

➤ Point- to- Point Interconnect allows for:

- ◆ Extend PCIe via signal conditioners and repeaters
- ◆ Optical & Copper cabling to remote chassis
- ◆ External Graphics solutions
- ◆ External IO Expansion

➤ Infrastructure is in Place

- ◆ PCIe Switches and Bridges
- ◆ Signal Conditioners

PCI Express In Industry

➤ First Release of Slots in 2005

- ◆ x16 High Performance Graphics
- ◆ x1 Low Cost Simple Connector
- ◆ Desktop Systems

➤ Systems Currently Shipping

- ◆ Desktops with multiple x16 connectors
- ◆ Servers with multiple x4 and x8 connectors

➤ Cards Available

- ◆ x4, x8 cards - 10 GbE, Dual/Quad GbE, 4 Gb FC, SAS, IB
- ◆ x16 High Performance Graphics @ 150 W

➤ PCIe 2.0 Status

- ◆ First (x16 Gen2) slots shipped in Q4 CY2007
- ◆ Adoption is slower than Gen 1

Recent PCI Express Changes

- Power increase for Graphics Cards to 300 Watts
- Lanes can be grouped
 - ◆ 1x, 4x, 8x, 16x and 32x supported, x2 no longer supported
 - ◆ Must support all groupings lower than your width
- Performance roadmap
 - ◆ Gen 2.0 Doubled to 5Gbits/ sec (DDR) with 8/ 10bit encoding
 - ◆ Gen 3.0 Doubles again to 8Gbits/sec (no 8b/ 10b)
- External expansion
 - ◆ Copper connector and connector specified
- Geneseo enhancements to PCIe 2.0
 - ◆ Standard for co-processors, accelerators
 - ◆ Encryption, visualization, mathematical modelling
- PCIe IO Virtualization (SR/ MR IOV)
 - ◆ Architecture allows shared bandwidth

Evolving I/O Architectures

- Processor speed increase slowing
 - ◆ Multi core processors increasing
 - ◆ Requires multi root complex architectures

- Requires high speed interface for interconnect
 - ◆ Minimum 10Gb data rates
 - ◆ Must support backplane distances
 - > Bladed systems
 - > Single box clustered processors
 - ◆ Need backplane reach, cost effective interface to IO

- Options
 - ◆ Use an existing IO interface like 10GbE/ Infiniband
 - ◆ Enhance PCI Express

Drivers for New IO Architectures

- **Interface speeds are increasing**
 - ◆ Ethernet moving from GbE to 10G and FC from dual 4 Gb to dual 8 Gb
 - Single applications struggle to supply enough bandwidth to fill these links
 - ◆ Processor speed growth is being replaced by multiple core processors
 - Requires applications to share these links
 - ◆ PCI Express IOV would allow this to happen

- **High Availability Increasing in Importance**
 - ◆ Requires duplicated processors, IO modules and interconnect
 - ◆ Use of shared virtual IO simplifies and reduces costs and power
 - Shared IO support N+1 redundancy for IO, power and cooling
 - Remotely re-configurable solutions can help reduce operating cost
 - Hot plug of cards and cables provide ease of maintenance
 - ◆ PCI Express Modules with IOV enable this

- **Growth in backplane connected blades and clusters**
 - ◆ Blade centres from multiple vendors
 - ◆ Storage and server clusters
 - ◆ Storage Bridge Bay hot plug processor module
 - ◆ PCI Express IOV allows commodity I/O to be used

Existing Serial Interfaces

- Established external transport mechanisms exist
 - ◆ Fibre channel
 - > Storage area network standard
 - ◆ 10Gb Ethernet
 - > Provides a network based solution to SANs
 - ◆ InfiniBand
 - > Choice for high speed process to processor links
 - > Supports wide and fast data channels
 - ◆ SAS
 - > Serial version of SCSI offers low cost solution
- No need to add to these yet another solution
 - ◆ PCI Express is not intended to replace these
 - ◆ But backplane IO must support these bandwidths

Backplane Serial Interfaces

- Inside the box no clear solution today
 - ◆ 10G Ethernet
 - Provides a network based solution to SANs

 - ◆ InfiniBand
 - Choice for scalable, high speed, low latency processor to processor links
 - Supports wide and fast data channels

 - ◆ PCI Express
 - Requires multi root complex support

- Will it be 10GbE, InfiniBand or PCIe IOV?

10G Ethernet or InfiniBand?

➤ 10G Ethernet

- ◆ May seem like the obvious choice, but currently lacks
 - > QoS mechanisms required
 - > Direct interface to root complex
 - > Low overhead stack
 - > Fiber Channel over Ethernet



➤ InfiniBand

- ◆ Has established stack
- ◆ Has higher speed capability
 - > SDR, DDR and QDR data rates
 - > 4x to 12X widths
 - > 500 MB/s to 6 GB/s

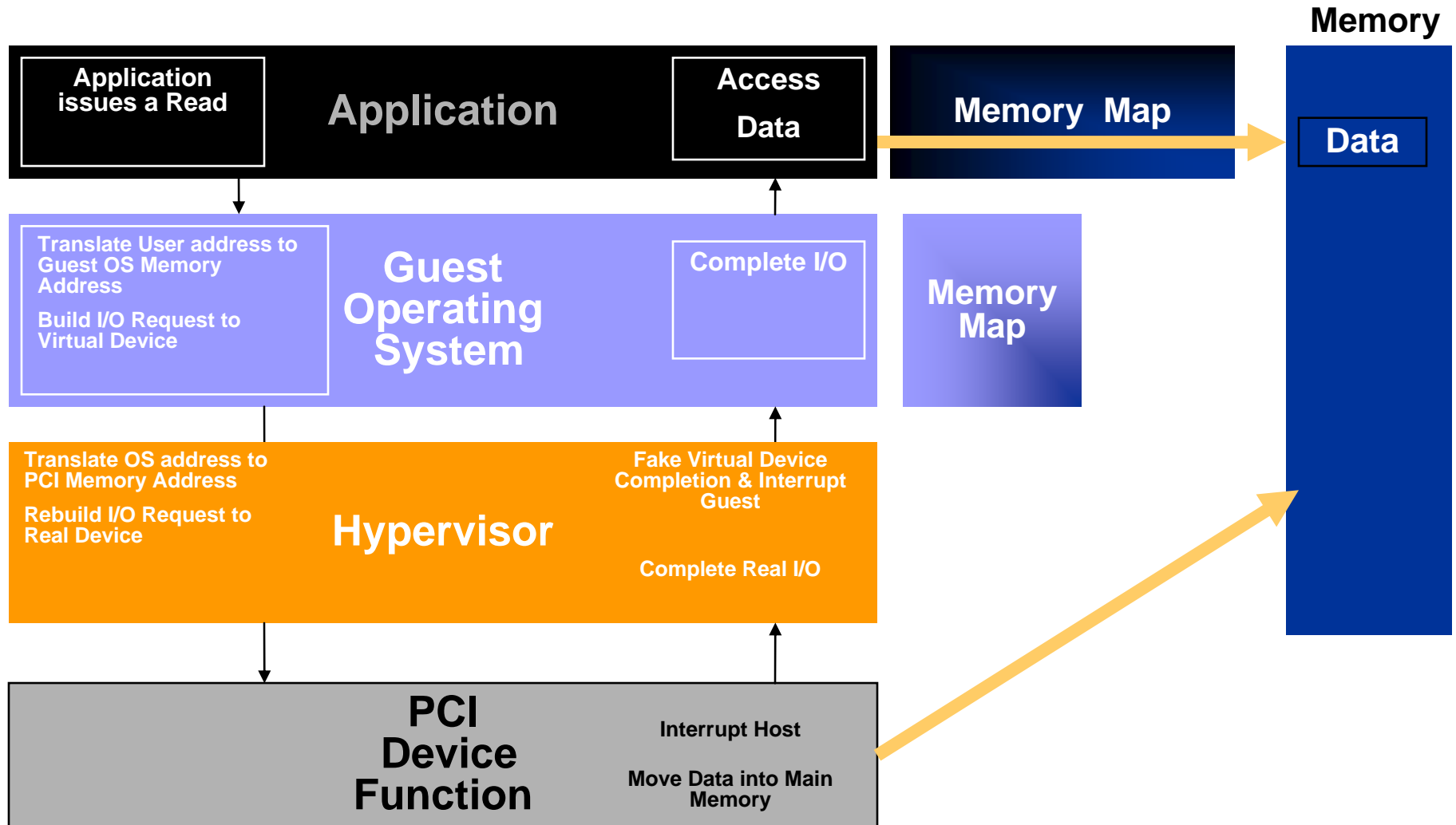
Check out SNIA Tutorials:

**FcoE: Fiber Channel Over Ethernet
InfiniBand Technology Overview**

Single Root IOV

Better IO Virtualization for Virtual Machines

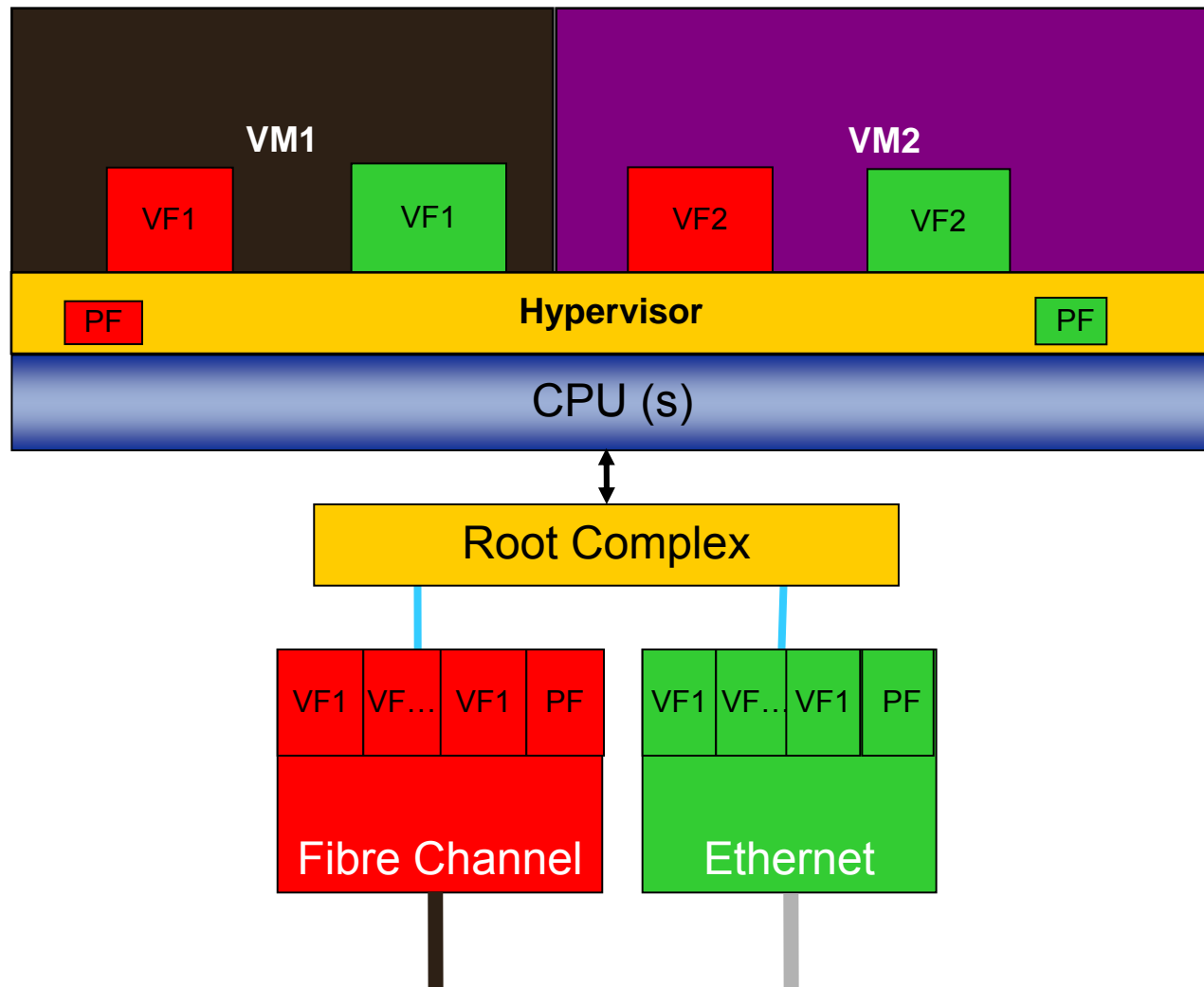
I/O with a Hypervisor



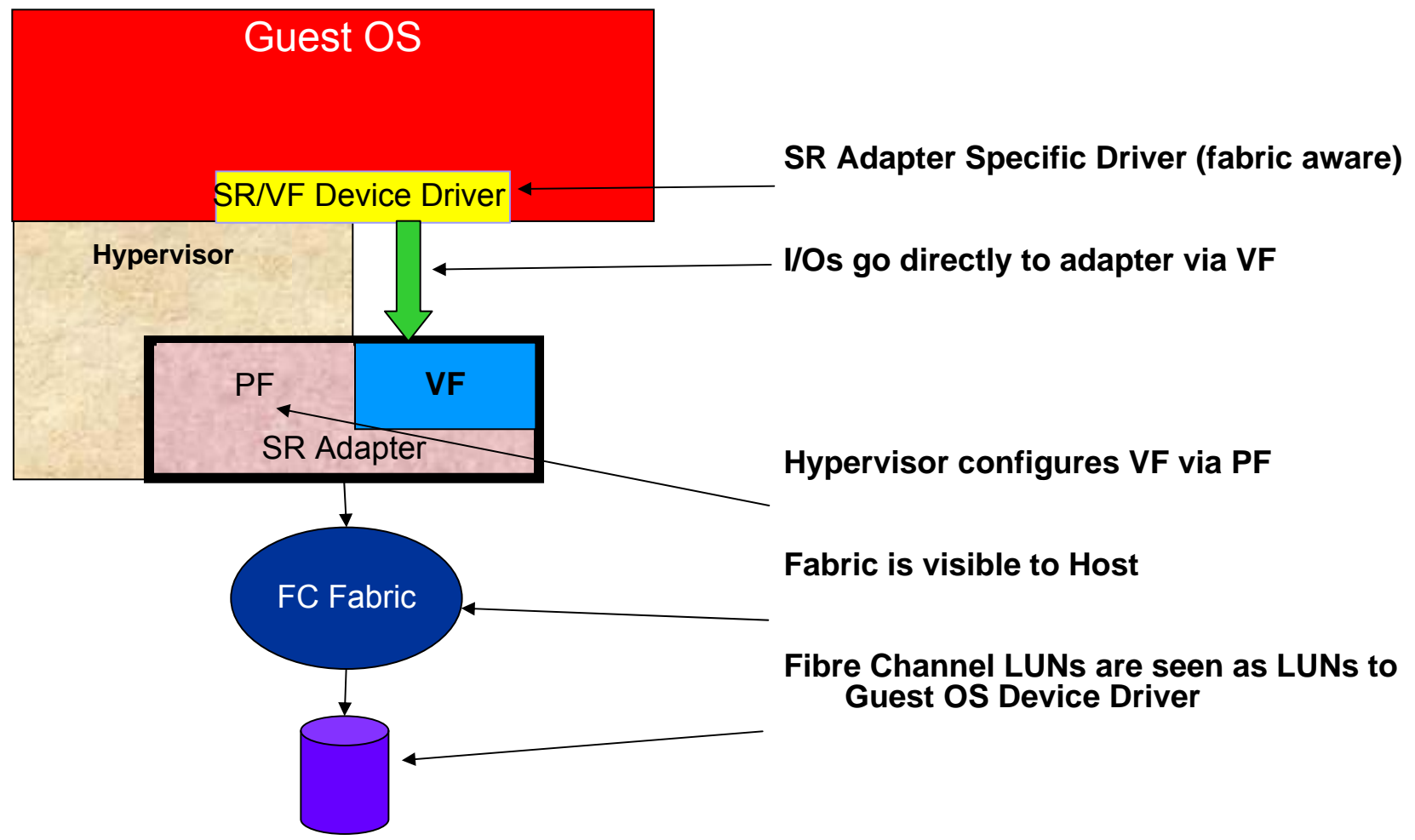
Single Root IOV

- Before Single Root IOV the Hypervisor was responsible for creating virtual IO adapters for a Virtual Machine
- This can greatly impact Performance
 - ◆ Especially Ethernet but also Storage (FC & SAS)
- Single Root IOV pushes much of the SW overhead into the IO adapter
 - ◆ Remove Hypervisor from IO Performance Path
- Leading to Improved better Performance for Guest OS applications

PCI-SIG Single Root



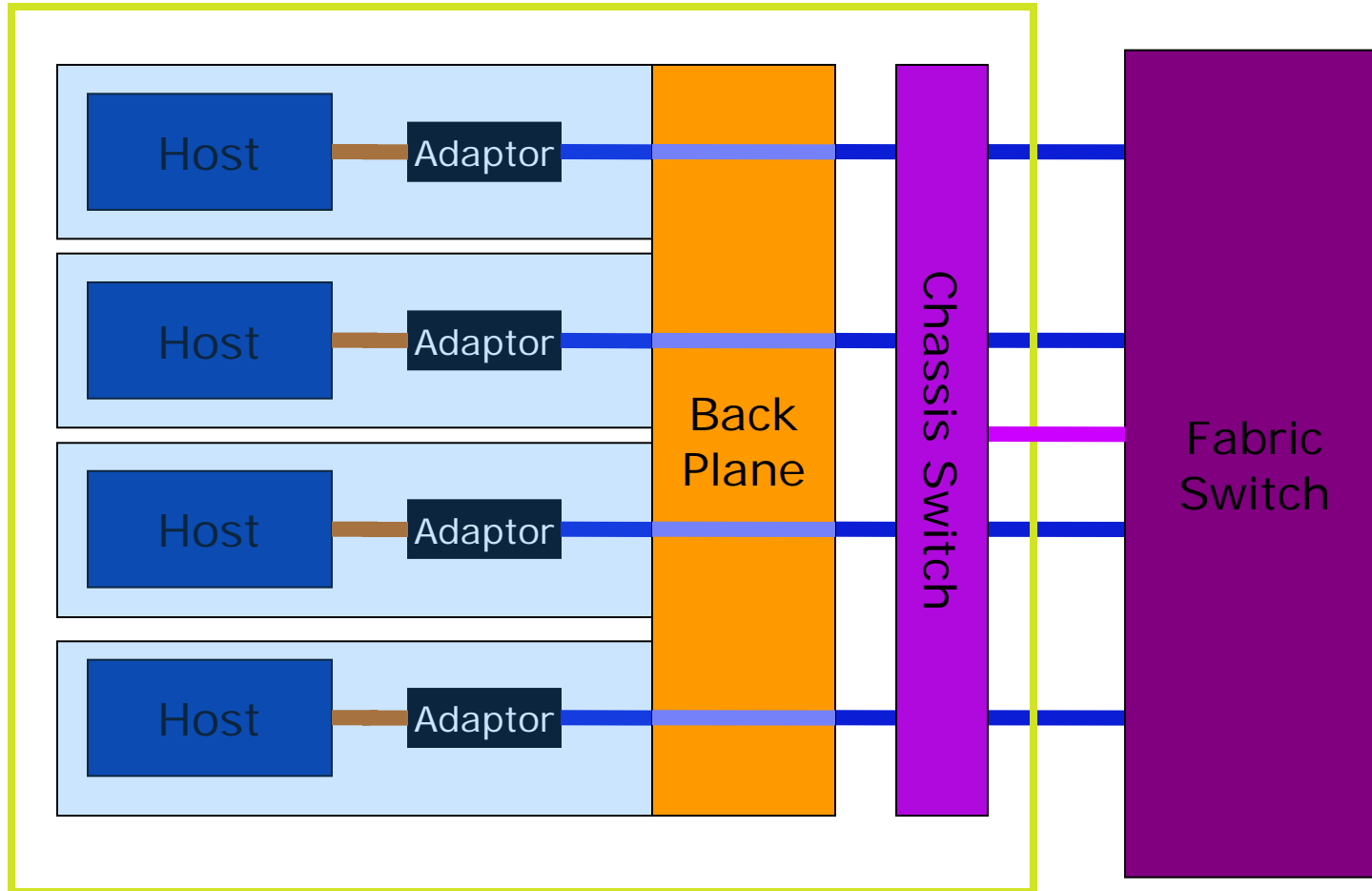
Fibre Channel and SR Virtualization



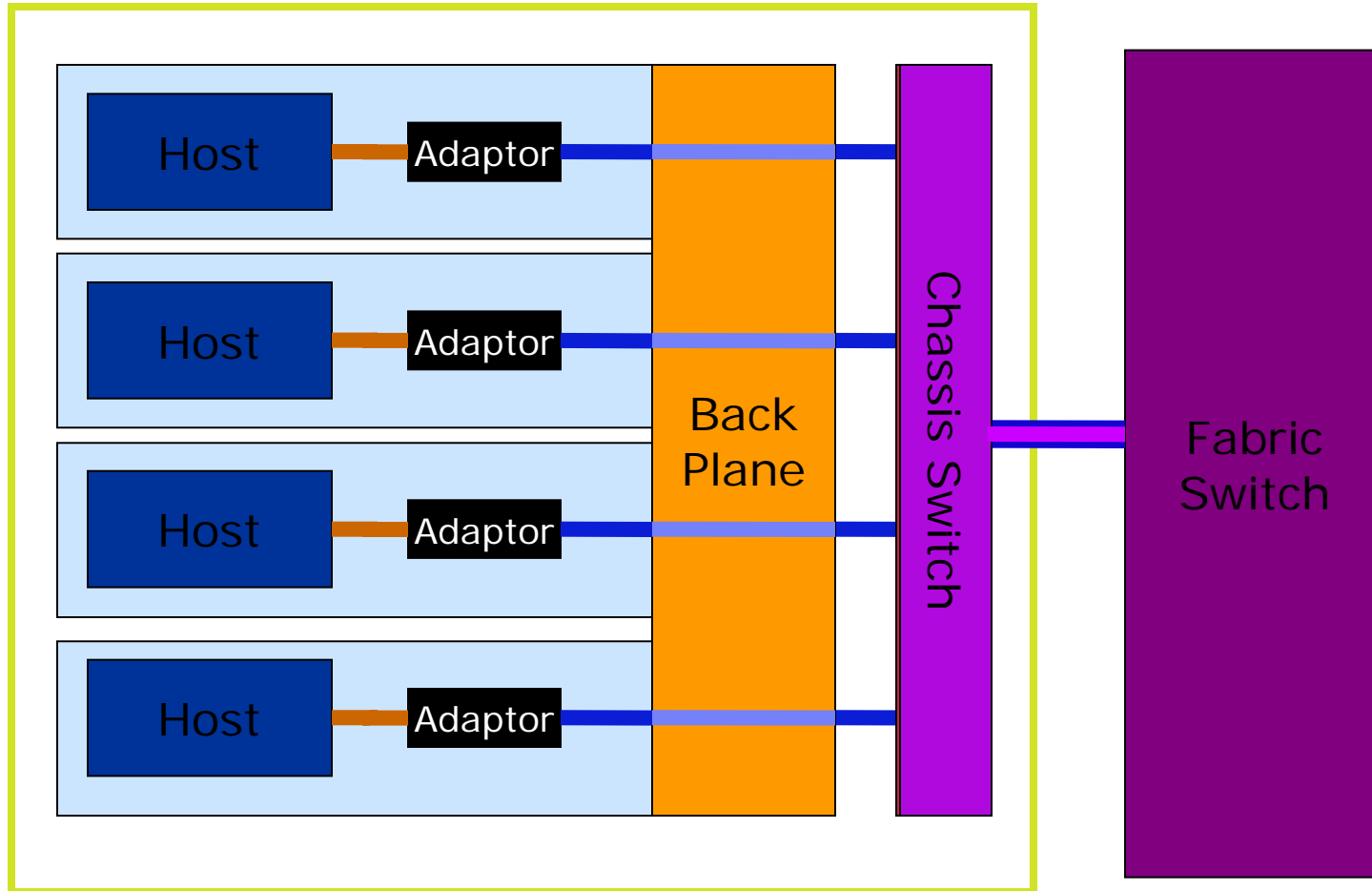
MultiRoot IOV

Virtualizing an IO adapter for multiple Hosts

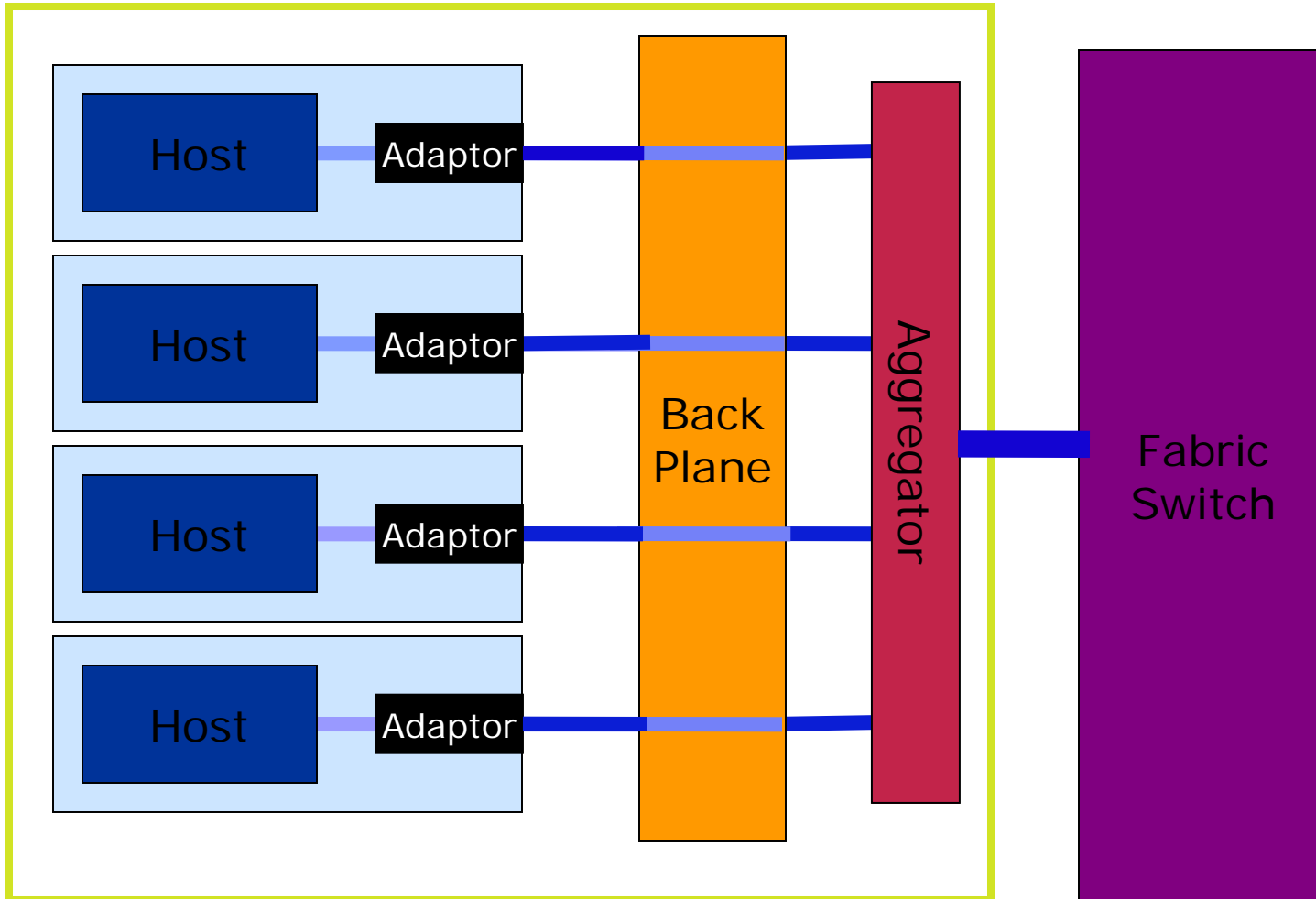
It Started With Pass Thru



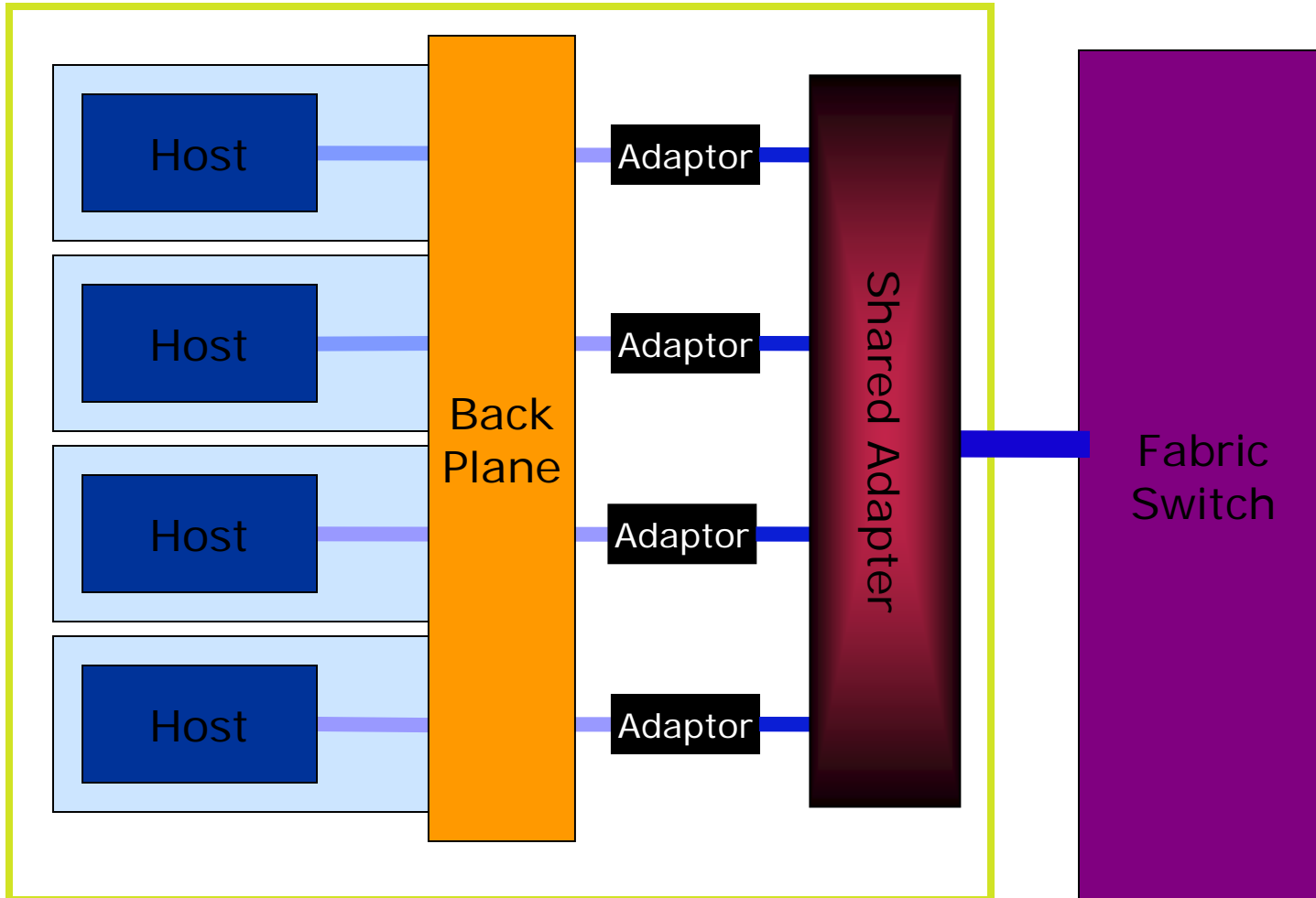
Chassis Switching to Aggregation



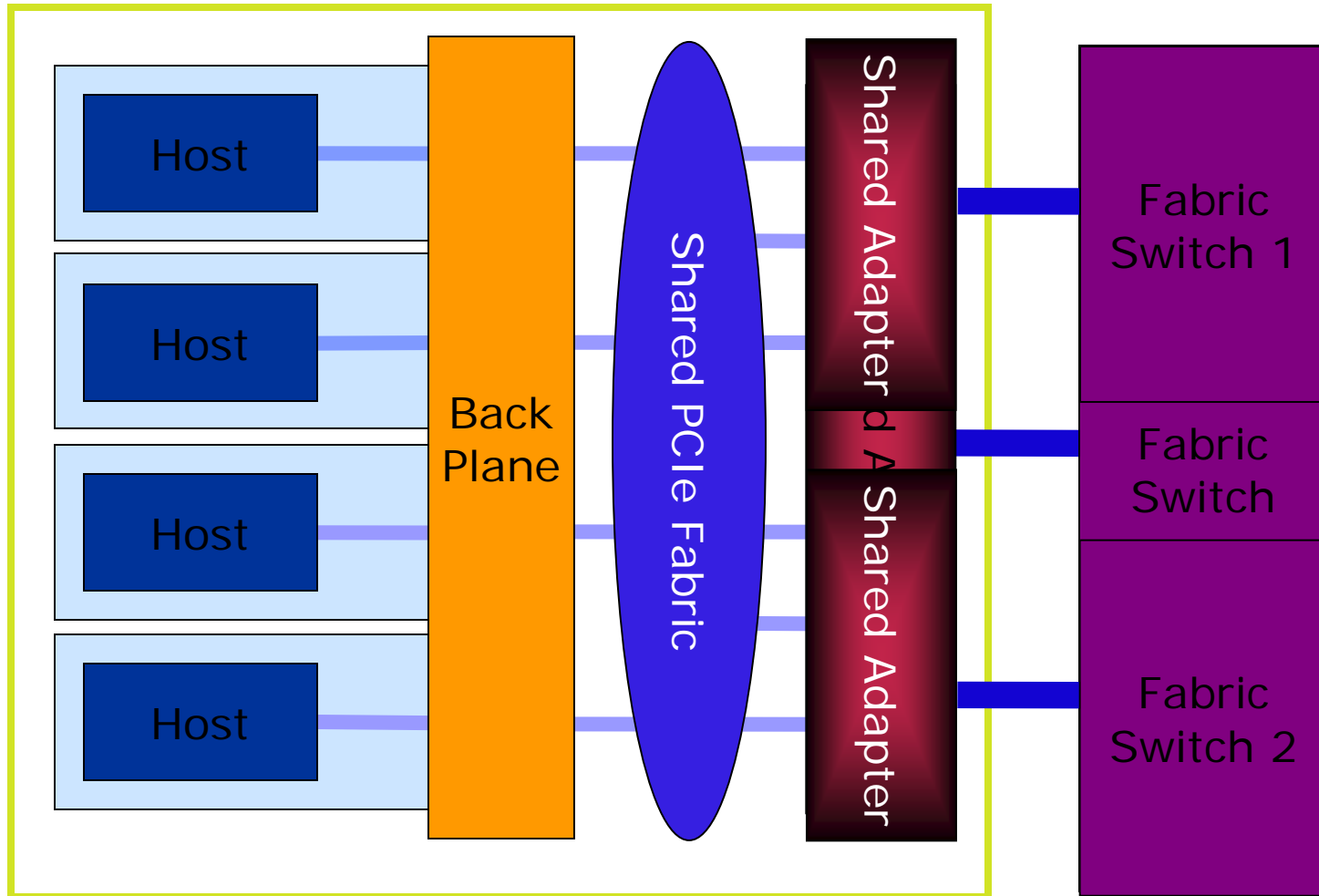
Stretch the PCIe Bus Across the Backplane



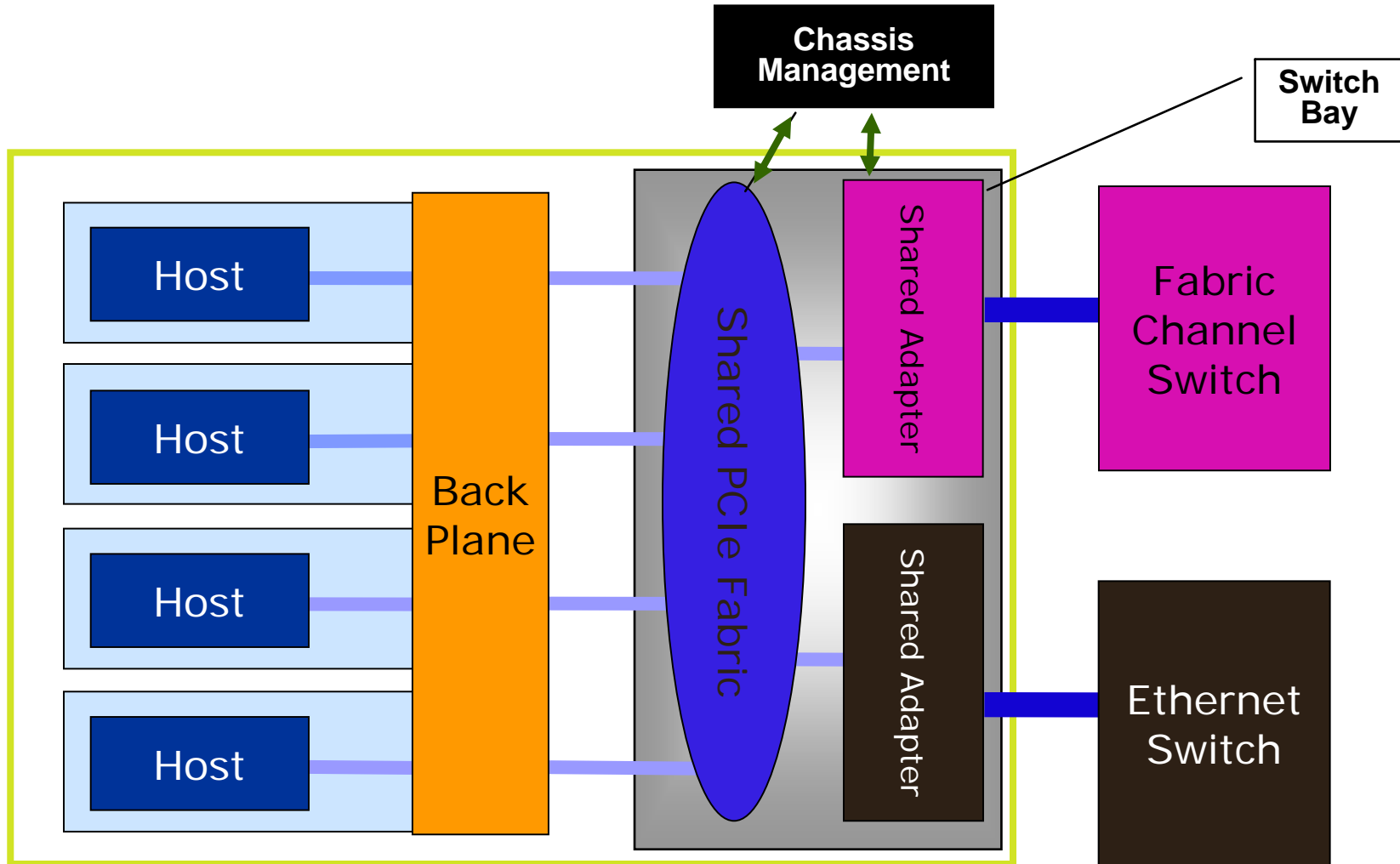
Merge the Adapter and Aggregator



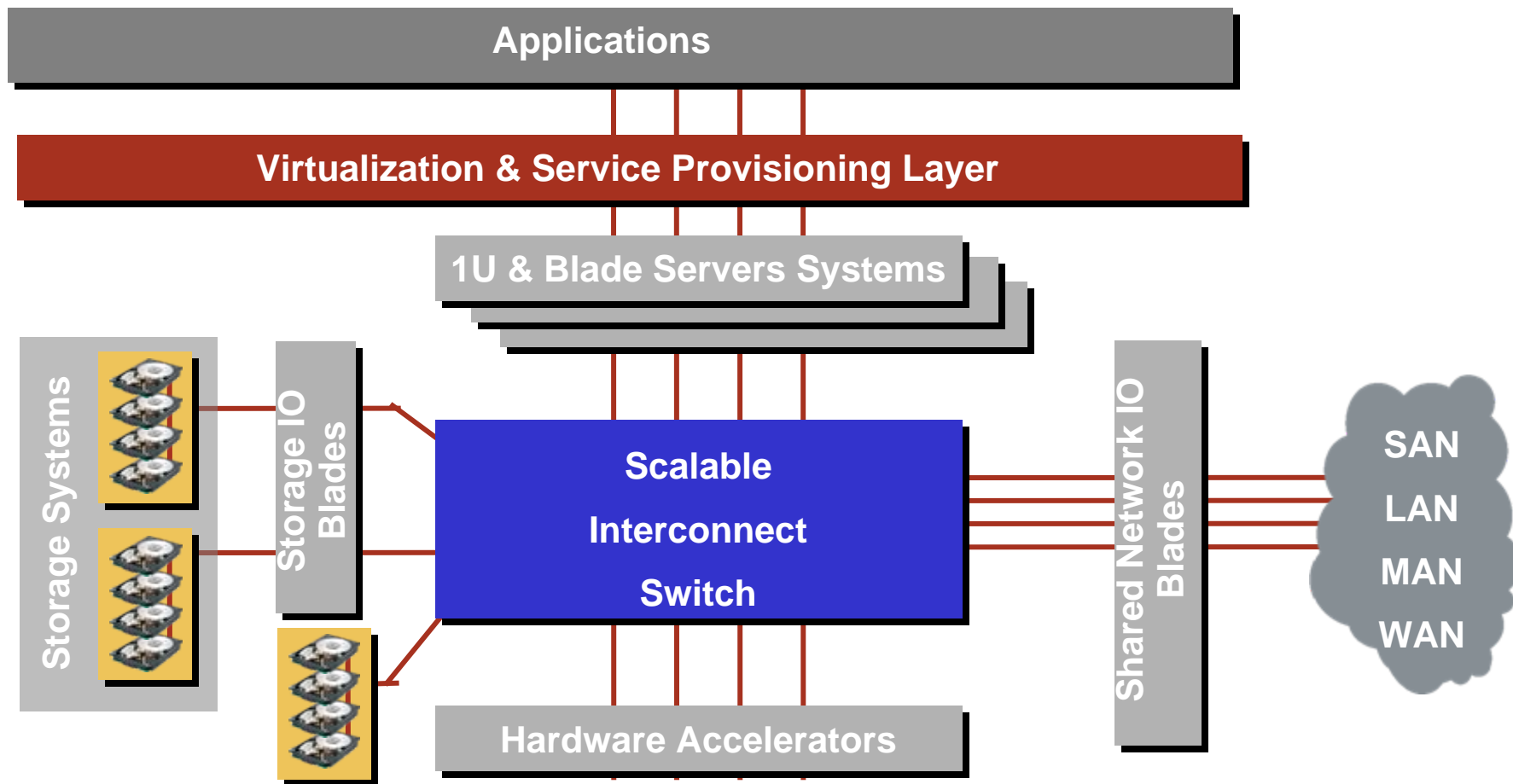
Insert a shared PCIe Fabric and add Multiprotocol



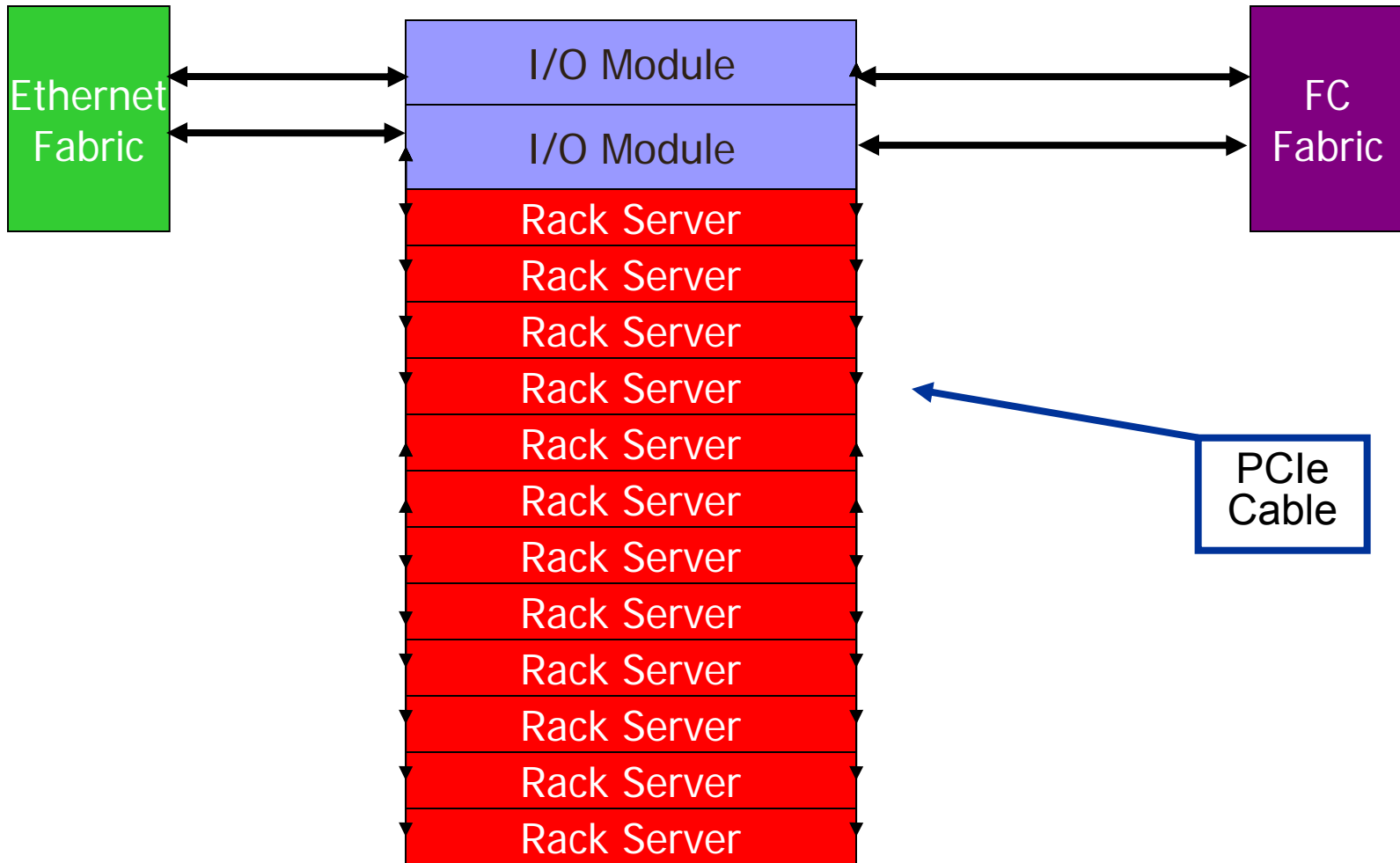
In a Blade Chassis



Mutli Root Virtualization in Blades



In a Rack



Impact / Benefit to Storage

➤ PCI Express provides

- ◆ Full Bandwidth Dual Ported 4 & 8 Gb FC
- ◆ Full Bandwidth SAS 1.0 & 2.0
- ◆ Legacy Support via PCI-X

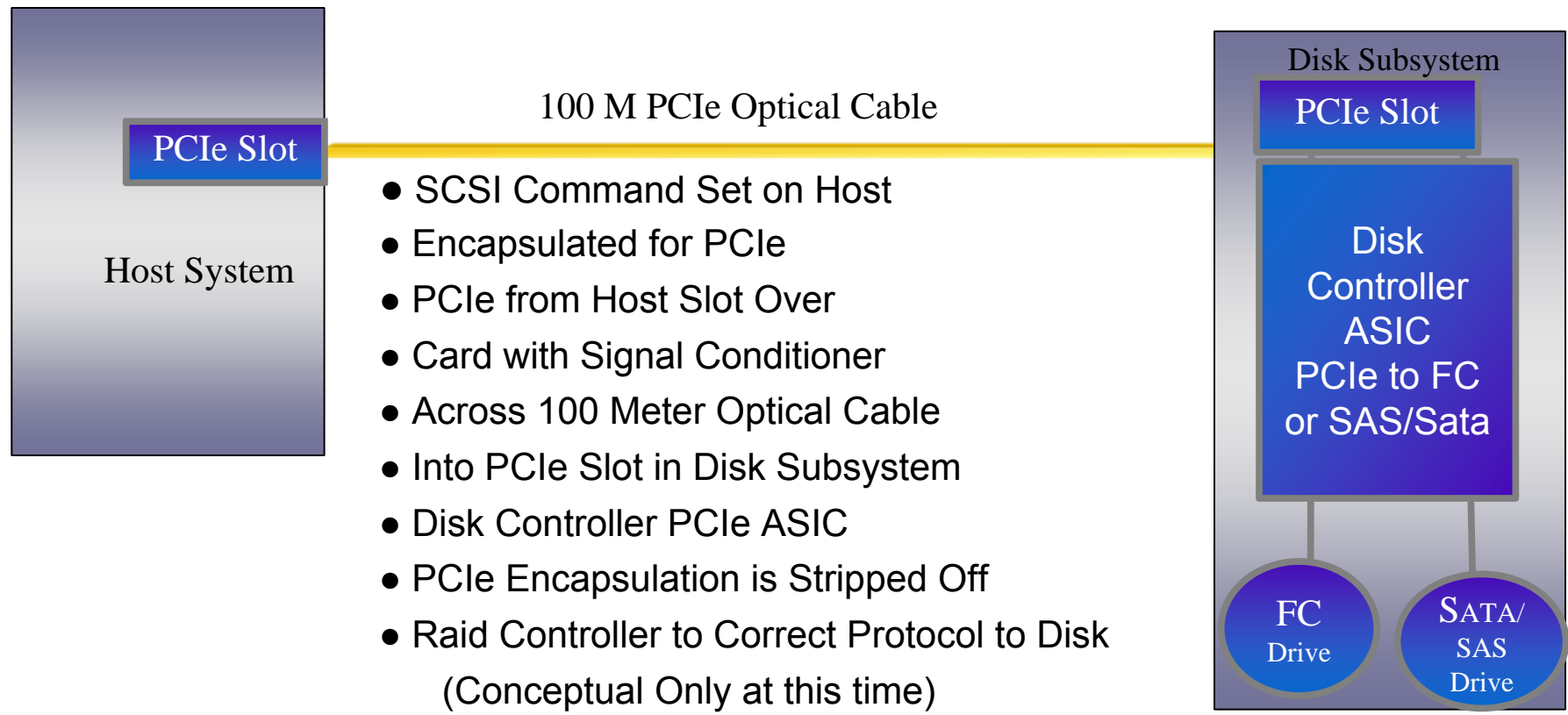
➤ IOV takes it one step further

- ◆ Ability for System Images to Share IO across OS Images
- ◆ Backplane for Bladed Environments

➤ Extension of PCIe

- ◆ Possible PCIe attached storage devices

Future Storage Attach Model



Glossary of Terms

PCI – Peripheral Component Interconnect. An open, versatile IO technology. Speeds range from 33 Mhz to 266 Mhz, with pay loads of 32 and 64 bit. Theoretical data transfer rates from 133 MB/ s to 2131 MB/ s.

PCI-SIG - Peripheral Component Interconnect Special Interest Group, organized in 1992 as a body of key industry players united in the goal of developing and promoting the PCI specification.

IB – InfiniBand, a specification defined by the InfiniBand Trade Association that describes a channel-based, switched fabric architecture.

Root complex – the head of the connection from the PCI Express IO system to the CPU and memory.

HBA – Host Bus Adapter.

IOV – IO Virtualization

Single root complex IOV – Sharing an IO resource between multiple operating systems on a HW Domain

Multi root complex IOV – Sharing an IO resource between multiple operating systems on multiple HW Domains

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