Emerging Non Volatile Memory
And
Spin Logic

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Outline

- Power is an issue
- New memories are coming
- Memory and logic can be combined
  - This will drive architectural advancements
- Summary, Q&A
Technical “Ages”

1. The Industrial Age (1800’s)
2. The Age of Electricity
3. The Age of Flight
4. The Age of Communications
5. The Atomic Age
6. The Space Age
7. The Information Age of Data Storage (2000’s)
Power Consumption Gains Focus
Today’s Memory/Storage Selection Criteria

- Cost
- Reliability
- Performance
Today’s Memory/Storage Selection Criteria

Tomorrow’s

Cost

Power

Reliability

Performance

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## Storage Products Roadmap

<table>
<thead>
<tr>
<th>Storage Type</th>
<th>HDD</th>
<th>Flash</th>
<th>STT RAM</th>
<th>ReRAM</th>
<th>FeRAM</th>
<th>PCM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Availability Year</strong></td>
<td>2014</td>
<td>2015</td>
<td>2016</td>
<td>2017</td>
<td>2018</td>
<td>2019</td>
</tr>
<tr>
<td><strong>HDD</strong></td>
<td>3.5 inch</td>
<td>8-10 TB</td>
<td>12 TB</td>
<td>16 TB</td>
<td>20 TB</td>
<td></td>
</tr>
<tr>
<td><strong>Flash</strong></td>
<td>128 Mb</td>
<td>256 Mb</td>
<td>256 Mb</td>
<td>3D NAND</td>
<td>512 Gb</td>
<td>1 Tb</td>
</tr>
<tr>
<td><strong>STT RAM</strong></td>
<td>64 Mb</td>
<td>256 Mb</td>
<td>1 Gb</td>
<td>4 Gb</td>
<td></td>
<td>16 Gb</td>
</tr>
<tr>
<td><strong>ReRAM</strong></td>
<td>2 Mb</td>
<td>8 Mb</td>
<td>64 Mb</td>
<td>1 Gb</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FeRAM</strong></td>
<td>1 Kb</td>
<td>8 Kb</td>
<td>16 Kb</td>
<td>256 Kb</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PCM</strong></td>
<td>2 Mb</td>
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<td>256 Gb</td>
<td>512 Gb</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Estimates**

- **HDD:** 8-10 TB, 12 TB, 16 TB, 20 TB
- **Flash:** 128 Mb, 256 Mb, Planar NAND, 3D NAND, 512 Gb, 1 Tb
- **STT RAM:** 64 Mb, 256 Mb, 1 Gb, 4 Gb
- **ReRAM:** 2 Mb, 8 Mb, 64 Mb, 1 Gb
- **FeRAM:** 1 Kb, 8 Kb, 16 Kb, 256 Kb
- **PCM:** 2 Mb, 128 Gb, 256 Gb, 512 Gb
NVM Cell Designs

STTRAM Cell

- Tantalum Top Metallurgy
- CoFeB Free Layer
- MgO Tunnel Insulator
- CoFeB Pinned Layer
- Tantalum Bottom Metallurgy

Resistive element

Diode

ReRAM Cell

- Iridium Top Metallurgy
- Ta$_2$O$_5$
- TaO$_x$
- TaN
- SiN$_x$
- TaN

Diode

PCRAM Cell

Crystalline Chalcogenide as GeSbTe

Resistive Electrode Heat Source

Diode

Schottky Diode
Spin Torque Tunneling Mechanism

Dr. Edward Grochowski
Computer Memory/Storage Consultant

Animation by Casey Straka
STT in the Memory/Storage Hierarchy

Source: Objective Analysis
MRAM Beats Flash & EEPROM Energy Consumption

Ref: D. Bennett and A. Pockson, ED April 2016
6T SRAM vs. 1T STT

6 CMOS Transistor SRAM Circuit

1 CMOS Transistor + 1 STTRAM Circuit

Result: MRAM Beats SRAM Cost

MRAM Can Be Stacked

Single-bit STT RAM Stack

Multi-bit STT RAM Stack

Ref: A. Shukh NVMTS 8/2013
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The cMem Cell: Logic + NVM

http://repository.cmu.edu/cgi/viewcontent.cgi?article=1418&context=dissertations
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Packaging and Performance

Total Interconnect length
- Chip level: 10’s mm
- Board level: 10’s inches
  i.e. Circuit Delay + Power

Ref: A. Shukh NVMTS 8/2013
STT Advantage:
Smaller Chip or More Functionality

Based On Rajiv Ranjan (Avalanche Technology)
Changing Von Neuman’s Computer Architecture Concept

CPU/Memory/Storage

- CPU Logic
- DRAM Memory
- Interface
- Storage

STTRAM/Spin Logic

- CPU
- STT RAM/Logic/Storage
- Inactive CPU/Memory (Dark Silicon)
Summary

- Power issues can be solved
  - NVM is a big contributor
- New memories are coming
  - STT is a promising candidate
- Memory and logic can be combined
  - This will drive architectural advancements
Questions?