NVDIMM Hands on Lab

Presented by:
AgigA Tech, Netlist, SMART

Flash Memory Summit 2014
August 5-6, 2014
Participating Companies:

Thanks to our Infrastructure Sponsors:
Agenda

✧ Part I
  ◆ NVDIMMs – Overview of how they work

✧ Part II
  ◆ NVDIMM Demonstration

✧ Part III
  ◆ Ultracapacitors – Overview of how they work

✧ Part IV
  ◆ Ultracapacitor Demonstration
NVDIMM – How it Works

- NVDIMM combines DRAM and Flash onto a single DIMM
- Operates as standard DRAM RDIMM
  - Fast, low latency performance.
- Host only addresses the DRAM and has no direct access to the flash (NVDIMM-N classification)
- NVDIMM contains switches to switch control back and forth between host and NVDIMM controller
- NVDIMM controller moves data from DRAM to flash upon power loss or other trigger; can back up portions or all of DRAM upon command
- If power fails, Supercaps (or other power source) provide back up power while DRAM is backed up to Flash
- MRC (Memory Reference Code) configures NVDIMM controller to move data back from Flash to DRAM when recovery is needed
- All the benefits of SSD with none of the performance limitations and best endurance
**NVDIMM Application Scenario**

<table>
<thead>
<tr>
<th>SSD/HDD has low throughput</th>
<th>&gt; 10X higher throughput for persistent data access</th>
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<tr>
<td>Software Overhead slows effective performance</td>
<td>No software overhead. Runs at HW speeds</td>
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System Memory Map
- Mapping NVM into application
  - BIOS table created at POST (Power on Self Test). This allows the driver to be made available

Data Access Method
- Byte: Direct access to NVM, no driver layer required
- Block/File: port ramdisk or file system to NVM

Other considerations
  (when the BIOS is set up some choices can be made)
- Processor cache policy for NV space
- Processor memory consistency model
- Impact of reduced data access time
Switching control to/from NVDIMM Controller

- NVDIMM Controllers typically run the DRAM at the lower speed than the host
  - Saves power allowing smaller Supercap pack
- The only way to switch clocks speeds or clock sources is to first put the DRAM into self-refresh
- Upon power loss or other entry condition, the host must insure that DIMMs are placed in self-refresh
- Main methods of putting the DIMMs in self-refresh
  - Standard ADR (see next page)
Intel ADR

• Asynchronous DRAM Refresh
• Hardware method for placing the DIMMs in self-refresh
• No software involvement
• Takes < 150us, removing the need for extra bulk capacitance

• Pros
  • Simplest self-refresh entry method
  • Hardware controlled. Not impacted by software hangs

• Cons
  • CPU caches are not flushed. Certain I/O buffers are not flushed either
  • Requires modifications to run-time software to implement fencing requirements

NVDIMM training slides provided by Intel
NVDIMM Entry Process using ADR

- Letters correspond to the timing diagram on the next page
SAVE Operation

![Diagram showing the SAVE operation process.]

- **SAVE Operation Flow:**
  - AC Power Supply
  - System DC Voltage and Powergood
  - CPLD
  - SAVE_Trigger
  - Processor / Chipset
  - NVDIMM

- **Timeline Details:**
  - **A:** AC Power Supply
  - **B:** DC Holdup Time (1-12 msec)
  - **C:** SAVE_Trigger
  - **D:** Normal Execution
  - **E:** Flush Data
  - **F:** SAVE
  - **G:** SR

Source: Viking NVDIMM tutorial for SNIA
NVDIMM Restore/Recovery MRC Flow

MRC Start

Yes

Save in Progress?

No

Train all DIMMs (including NVDIMMs) like standard DIMM

Does NVDIMM contain valid Data?

No

Did the NVDIMM Log an error?

Yes

Note Error in output Structure

No

Configure Memory Controller to drive CKE low

Configure NVDIMM to Start Restore

Is Restore Complete?

No

Note Restore Status in MRC Output Structure

Rewrite RC registers

Yes

End of Restore Process

Yes

Assert CKE

Rewrite MRS Registers

Run MemTest and MemInit on all DIMMs that didn’t have a successful restore

No

Save in Progress?

No

Yes

NVDIMM training slides provided by Intel
Population Rules

- There are no NVDIMM specific population rules
  - Normal DIMM population rules still apply (e.g., RDIMMs and LRDIMMs can’t be mixed)
  - NVDIMMs and normal DIMMs may be mixed in the same channel
  - NVDIMMs from different vendors may be mixed in the same system and even the same channel.
- How the DIMMs are installed in a system will affect performance, so thought should be put into how DIMMs are populated
- NVDIMM population tips
  - Interleaving DIMMs within a channel provides a very small performance benefit
  - Interleaving DIMMS across a channel provides a very large performance benefit
  - Two DIMMs of the same type should not be installed in the same channel unless all other channels in the system have at least one of that type DIMM.
Memory Map

- MRC interleave code will insure that NVDIMMs are not interleaved with normal DIMMs while maintaining optimal interleaving

- General Memory map assuming NUMA is enabled (Non Uniform memory Architecture)
  - All normal DIMM from Socket 0 interleaved together
  - All NVDIMMs from Socket 0 interleaved together
  - All normal DIMM from Socket 1 interleaved together
  - All NVDIMMs from Socket 1 interleaved together
Example Optimal Interleaves

Has a 4-way Interleave between normal DIMMs

Has a 4-way Interleave between normal DIMMs, and optionally a 4-way interleave between the NVDIMMs

Has a 4-way Interleave between normal DIMMs, and optionally a 2-way interleave between the NVDIMMs

Has a 2-way Interleave between normal DIMMs, and optionally a 2-way interleave between the NVDIMMs

NVDIMM training slides provided by Intel
Industry Standardization

- NVDIMM gaining support from ecosystem
  - Intel DDR4 NVDIMM support for Grantley
  - Supermicro DDR4 NVDIMM support

- JEDEC Hybrid Memory Task Group
  - 12V and SAVE_n pins added to DDR4 DIMM socket
  - 12V in DDR4 socket will simplify NVDIMM power circuitry and cable routing

- SNIA NVDIMM SIG
  - Established in 2013 to promote adoption of NVDIMMs
Part II NVDIMM Demonstration
Goals

- Explain the hardware and software configuration
- Demonstrate interoperability among NVDIMM vendors
- Show how the system recognizes the NVDIMM
- Perform a Backup/Restore cycle with data validation
- Configure the NVDIMM memory as a RAM Drive
- Answer any questions about NVDIMM functionality
Configuration

Hardware
- System: Supermicro X9DRH-iF-NV
- BIOS: Supermicro 06/27/2104
  - Erase/Arm in BIOS
- Processor: Intel Ivy Bridge
  - Xeon E5-2690 V2 3.00GHz
- Installed Memory Configuration
  - 4GB RDIMM (standard)
  - 4GB Agigatech NVDIMM
  - 4GB Netlist NVDIMM
  - 4GB SMART NVDIMM

Software
- Operating System: CentOS 6.5 x86_64
- Kernel Version: 3.14 with Intel Storage Patch
  - 3.14.0-stor4.2
NVDIMM Configuration Menu
- Advance – Chipset Configuration – North Bridge
Interoperability and Recognition

▷ Boot the system
  - Observe no issues

▷ Display the E820 Memory Map Table
  - Observe all 12 GB of NVDIMM RAM grouped as (protected)
  - Defined as Type 12 (0xC) memory by Intel

```
[ 0.000000] e820: BIOS-provided physical RAM map:
[ 0.000000] BIOS-e820: [mem 0x0000000000000000-0x00000000000000ff] usable
[ 0.000000] BIOS-e820: [mem 0x0000000000000000-0x00000000000009ff] reserved
[ 0.000000] BIOS-e820: [mem 0x0000000000000000-0x0000000000000fff] reserved
[ 0.000000] BIOS-e820: [mem 0x0000000000000000-0x00000000000733d4ff] usable
[ 0.000000] BIOS-e820: [mem 0x00000000733d5000-0x000000007d02fff] ACPI NVS
[ 0.000000] BIOS-e820: [mem 0x000000007d03000-0x000000007d257fff] reserved
[ 0.000000] BIOS-e820: [mem 0x000000007d258000-0x000000007d619fff] ACPI NVS
[ 0.000000] BIOS-e820: [mem 0x000000007d61a000-0x000000007f353fff] reserved
[ 0.000000] BIOS-e820: [mem 0x000000007f354000-0x000000007f7fffff] ACPI NVS
[ 0.000000] BIOS-e820: [mem 0x000000007f7fffff-0x000000007f9b0000] usable
[ 0.000000] BIOS-e820: [mem 0x0000000000000000-0x00000000000000ff] (protected)
[ 0.000000] e820: update [mem 0x0000000000000000-0x0000000000000fff] usable ==> reserved
[ 0.000000] e820: remove [mem 0x0000000000000000-0x0000000000000fff] usable
[ 0.000000] e820: last_pfn = 0x480000 max_arch_pfn = 0x40000000
[ 0.000000] e820: last_pfn = 0x733d5 max_arch_pfn = 0x40000000
[ 0.000000] e820: [mem 0x0000000000000000-0x0000000000000fff] available for PCI devices
[ 0.846932] e820: reserve RAM buffer [mem 0x00008f0000-0x00008fff]
[ 0.846934] e820: reserve RAM buffer [mem 0x01000000-0x010000000]
```

[20]
Backup / Restore and Verify

- Write a data pattern to the protected RAM
- Verify the data pattern
- Shut off system power
- Observe Backup operation
- Restore system power
- Observe Restore and Erase operations
- Verify the data pattern
Configure a RAM Drive

- Add the ADR driver to the kernel
  - Modprobe

- Create and format a drive partition
  - Fdisk

- Create a mount point and mount the drive
  - Mount

- Display the newly mounted drive
  - df
Part III Ultracapacitors
Overview of how they work
What is an Ultracapacitor?
(also known as supercaps)

Invented in U.S. by Robert A. Rightmire of SOHIO Company.

- U.S. Patent 3,288,641 “ELECTRICAL ENERGY STORAGE APPARATUS: This invention relates generally to the utilization of an electrostatic field across the interphase boundary between an electron conductor and an ion conductor to promote the storage of energy by ionic adsorption at the interphase boundary.” Nov. 29, 1966

Electrochemical storage batteries and capacitors have been in existence for over 2000 years (Baghdad battery BC), Volta “pile” 1800, to Ben Franklin 1848 who coined the term “battery”.

- Battery stores energy in chemical bonds that follow reduction-oxidation (REDOX) reactions. Mass transfer is involved.
- Capacitors store energy in electrostatic fields between ions in solution and a material. No mass transfer involved – hence no electrochemical wear out.

Source: Joel Schindall, “Concept and Status of Nano-sculpted Capacitor Battery,” Presented at 16th Annual Seminar on Double Layer Capacitors and Hybrid Energy Storage Devices December 4-6, Deerfield Beach, Florida
Capacitor Terminology

- **Electrolyte**: An ionic conducting liquid, type varies for each type of electrochemical capacitor.

- **Separator**: Porous paper, polymer or ceramic that prevents EC electrodes from shorting together. Must be ion conducting (porous) and electron blocking.

- **Current collectors**: Metal foils used in each electrode to which the carbon electrode films are laminated. Typically aluminum foil.

- **Charge**: Ionic molecules in solution, electrons in conducting medium.
What is an EDLC Ultracapacitor?

Electrochemical double layer capacitors (EDLCs) or ultracapacitors are electrochemical capacitors that have an unusually high energy density when compared to common capacitors, typically several orders of magnitude greater than a high-capacity electrolytic capacitor.
Schematic construction of a wound Ultracapacitor

1. Terminals
2. Safety vent
3. Sealing disc
4. Aluminum can
5. Positive pole
6. Separator
7. Carbon electrode
8. Collector
9. Carbon electrode
10. Negative pole
Construction of a wound Ultracapacitor
Layman example for difference between:

Ultracapacitor

More power required for small time interval in 200 m race

Battery

Constant but less power required for large time in 20 km race
Ultracapacitors

Advantages:

- **High energy storage.** This is a result of using a porous activated carbon electrode to achieve a high surface area.
- **Low Equivalent Series Resistance (ESR).** Compared to batteries, EDLCs have a low internal resistance, hence providing high power density capability.
- **Wide Temperature range.** Capable of delivering energy down to -40 °C with minimal effect on efficiency and can operate up 65 °C and withstand storage up to 85 °C.
- **Fast charge/discharge.** Since EDLCs achieve charging and discharging through the absorption and release of ions and coupled with its low ESR, high current charging and discharging is achievable without any damage to the parts.

Disadvantages:

- **Low per cell voltage.** EDLC cells have a typical voltage of 2.7V. Since, for most applications a higher voltage is needed, the cells have to be connected in series.
This product is NOT classified as dangerous goods, per U.S. DOT regulations, under (see § 173,176). Ultracapacitors as articles are not specifically listed nor exempted from hazardous materials regulations (HMR). The materials comprising the ultracapacitors are “…in a quantity and form that does not pose a hazard in transportation”. Therefore, the ultracapacitors are not subject to the HMR.
Ultracapacitor Equations

Energy = P x ∆t

Energy = \( \frac{1}{2} C \left( V_{\text{max}}^2 - V_{\text{min}}^2 \right) \)

\[
C = \frac{2 \left( P \times \Delta t \right)}{\left( V_{\text{max}}^2 - V_{\text{min}}^2 \right)}
\]
Cell Balancing

5.14 V
2.28 V  ~2.86 V
0.00 V  ~2.24 V

V+
2.86V
2.24V

R

BALANCING RESISTOR

~2.55V
~2.55V
Operating Life Range

Lifetime vs Temperature

Lifetime in Years

Temperature

Ultracapacitor Voltage

- 2.0
- 2.1
- 2.2
- 2.3
- 2.4
- 2.5
- 2.6
- 2.7
Ultracapacitor Testing

Reliability Test Data

- Operating Voltage, accelerated Temp
- Accelerated operating conditions B
- Accelerated operating conditions A
- Max rated operating conditions
Ultracapacitor Testing

Datasheet EOL
1000 hrs @ 70%

Vendor A
Vendor B
Vendor C
Failed

Not all Ultracaps are created equal!!
Ultracapacitor Testing

Accelerated Life Testing at Operating Voltage and Elevated Temp

Vendor A
Vendor B
Vendor C
Size will be dictated by:
- Form Factor Constraints (x, y, z)
- NVDIMM Density/Power
- Backup Time
- Lifetime Requirements
- Max Temperature
Part IV Ultracapacitor Demonstration
NVDIMM Lab Sponsor’s Company Profiles
Headquarters: San Diego, CA

Company History: Early technology development began in 2006 as part of Simtek (acquired by Cypress in 2008), Cypress now sole investor

Sole focus since company inception has been on Non-Volatile RAM technology (better known today as NVDIMM)

Contact Us: info@agigatech.com

Visit Us: www.agigatech.com
Established: 2000
Headquarters: Irvine, CA
NASDAQ Symbol: NLST
Memory IP: 81 Patents (issued and pending)

“24x7, 18 month power cycling without single bit error”
– Jeff Rabe, Dell Compellent

Contact Information: vault@netlist.com
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Established: 1988
Headquarters: Newark, CA
Wide portfolio of memory products
Vertically integrated from wafer to final product
Worldwide footprint to support OEM customers
Helping to drive the adoption and standardization of NVDIMMs
SMART provides a variety of NVDIMM and supercap module form factors

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Thank You!