VM Futures Panel: Are We Near the Beginning of a New Solid State Epoch, or Is That Just a Big Fireball in the Sky?

- Moderator: Tom Coughlin, Coughlin Associates
- Panelists:
  - Dave Eggleston, Intuitive Cognition Consulting
  - Barry Hoberman, Spin Transfer Technologies
  - Tanmay Kumar, Crossbar
  - Joseph O'Hare, Everspin
  - Saul Zales, Contour Semiconductor

STORAGE INDUSTRY SUMMIT

Realizing the Benefits of the Convergence of Storage and Memory

JANUARY 20, 2015, SAN JOSE, CA

David Eggleston
Intuitive Cognition Consulting
Principal

Roadmap for New NVM

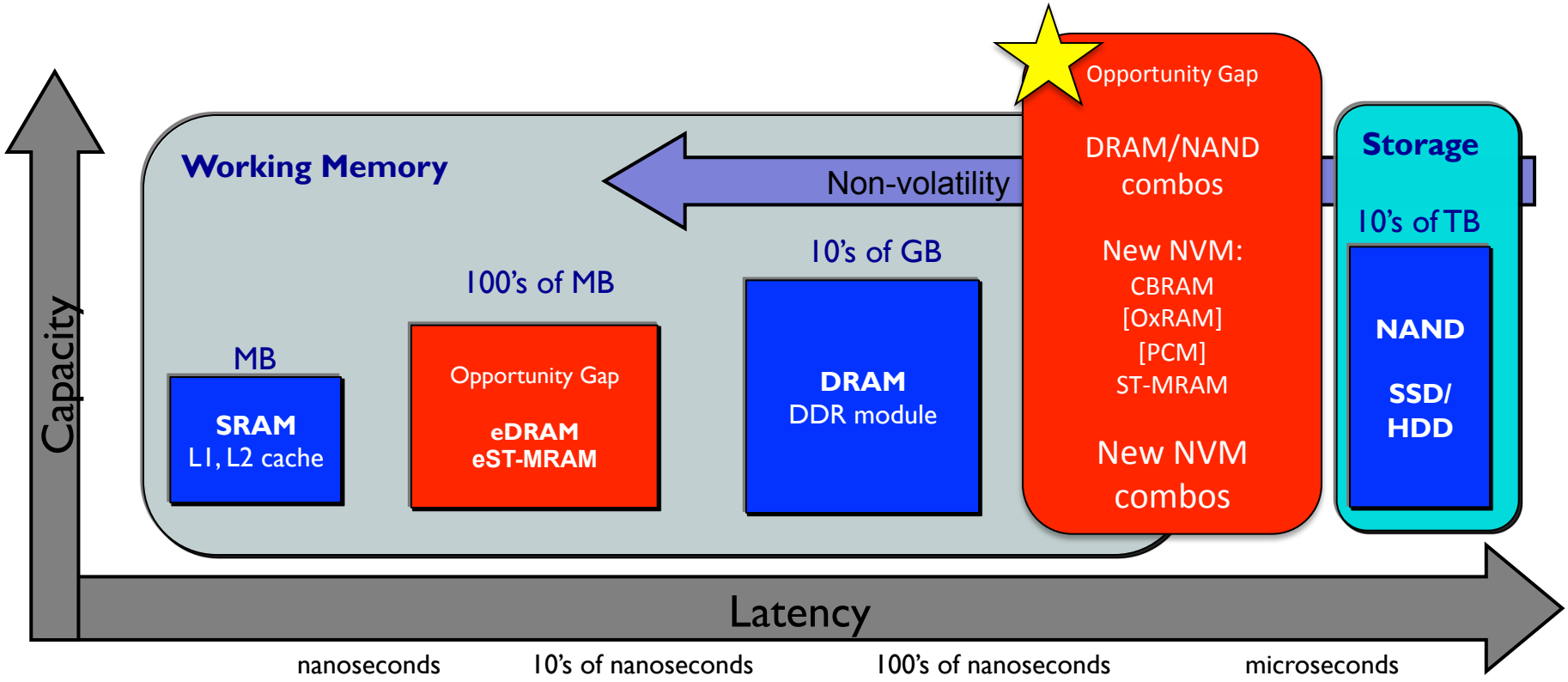
SNIA™
Solid State Storage Initiative

Looking through the Windshield

SNIA™ Solid State Storage Initiative

- Planar NAND scaling is drawing to a close
- 3D NAND succeeds planar NAND (until 2025)
- So how and where do new NVM technologies fit in?
- Role for new NVM before 2025?
- Requirements for new NVM on the memory bus:
  - 100's of GB's to TB's of capacity (per module)
  - Latencies in the high 100's of ns to low us
  - Cost <50% of DRAM
  - Bring non-volatility into the cache coherent network

Latency, Latency, Latency



- The best opportunity for new NVM over the next 10 years lies between NAND and DRAM, with latency in the low to sub microsecond range.
- With system changes, new NVM moves into the working memory space.

New NVM Contenders for this Memory Bus Opportunity Gap

SNIA™ Solid State Storage Initiative

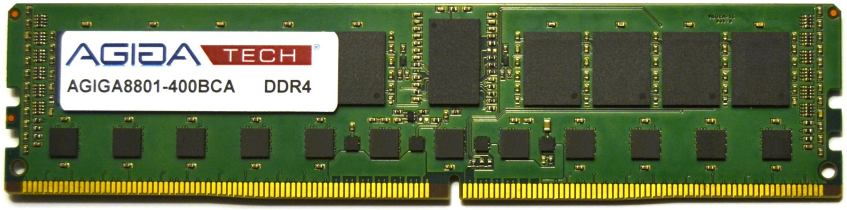
- Technologies:
  - RRAM
    - 1S-1R Conductive Bridging RAM (CBRAM)
      - Small cell size, but endurance limitations
    - 1R Oxide RRAM (OxRAM)
      - Will be used for 3D data storage in 2021+
      - Dense, but too slow for low latency memory
  - PCM
    - 1S-1R Phase Change Memory
      - Scaling challenges, fallen out of favor?
  - ST-MRAM
    - 1T-1MTJ ST-MRAM
      - Great performance and endurance, but cell size limitations

Barriers to New NVM Adoption

SNIA™ Solid State Storage Initiative

- Lots of money to be made on NAND and DRAM.
- Investments are in 3D NAND manufacturing, not in new NVM manufacturing.
- Intense material science, takes a very long time.
- Process integration is challenging and expensive.
- New NVM will be imperfect memory, and will require controller technology
- New system architectures that accept memory non-deterministic behavior must be deployed.

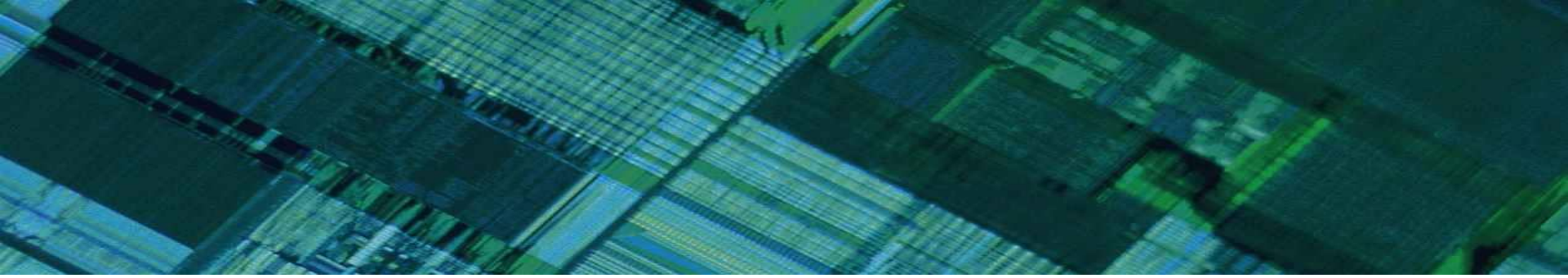
Don’t want to wait?



- Combinations of DRAM and Flash on modules solve some of these problems today!
  - NVDIMM-N, NVDIMM-F both available now
- Expect new NVM (low latency memory) to arrive on modules by 2018.
- SNIA NVM-PTWG is paving the way with the programming models – so applications can be aware and take advantage of non-volatility in the system.

Thank you!

DAVID EGGLESTON
INTUITIVE COGNITION CONSULTING
DAVE@IN-COG.COM



Spin Transfer Technologies

An Allied Minds Company

Orthogonal Spin Transfer (OST)

A Better Approach

SNIA NVM Summit
January 2015

Company Background

History

- Formed in 2007 by Allied Minds and NYU to commercialize Orthogonal Spin Transfer (OST) MRAM research led by Professor Andrew Kent
- In 2012, raised $36 million financing, plus additional $70 million in 2014, from Allied Minds, Invesco, & WIM, and established Silicon Valley headquarters

Technology

- OST-MRAM is a disruptive innovation in the field of spin transfer MRAM devices and offers advantages over other MRAM
- Higher speed, lower cost, lower power consumption, higher reliability, and enhanced lithographic scalability

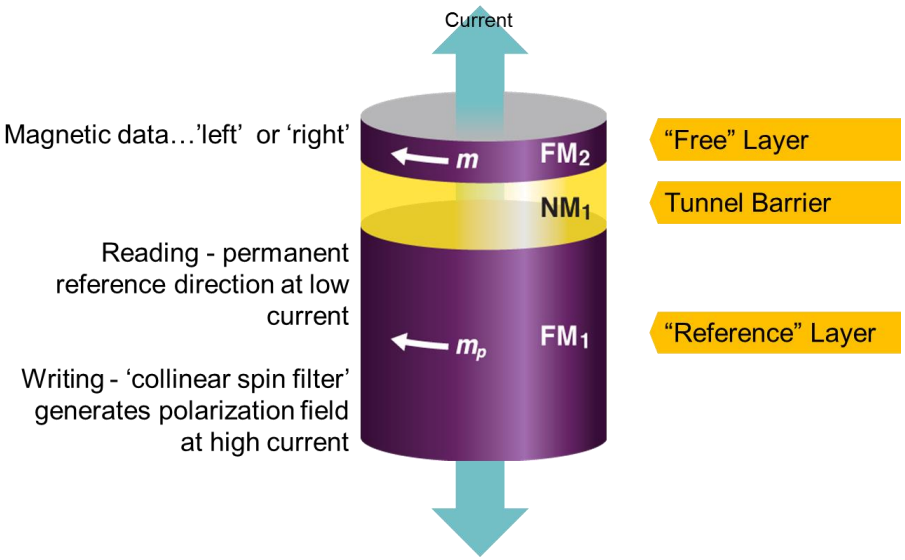
Opportunity

- Served Market Opportunity of $150 Billion in 2015
- Targeted as a replacement for DRAM, SRAM or flash memory
- Markets in storage systems, mobile devices, computing, microcontrollers and SOCs in standalone or embedded configurations

OST MRAM

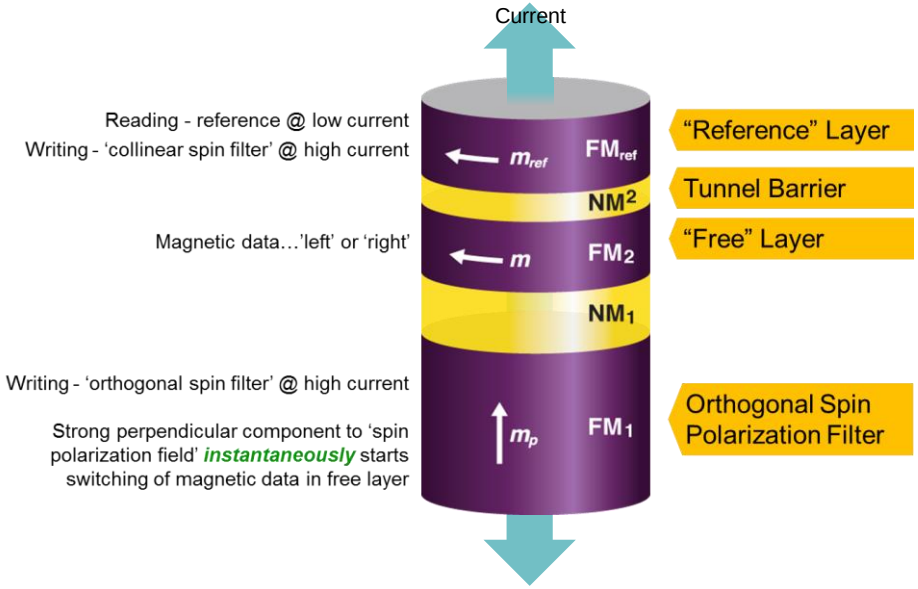
Combining Orthogonal Spin Filter with Collinear MTJ

Conventional Collinear Spin Transfer MTJ Structure



'Brand X'

'Spin Balanced' Orthogonal Spin Transfer MTJ Structure



'Spin Transfer Technologies'

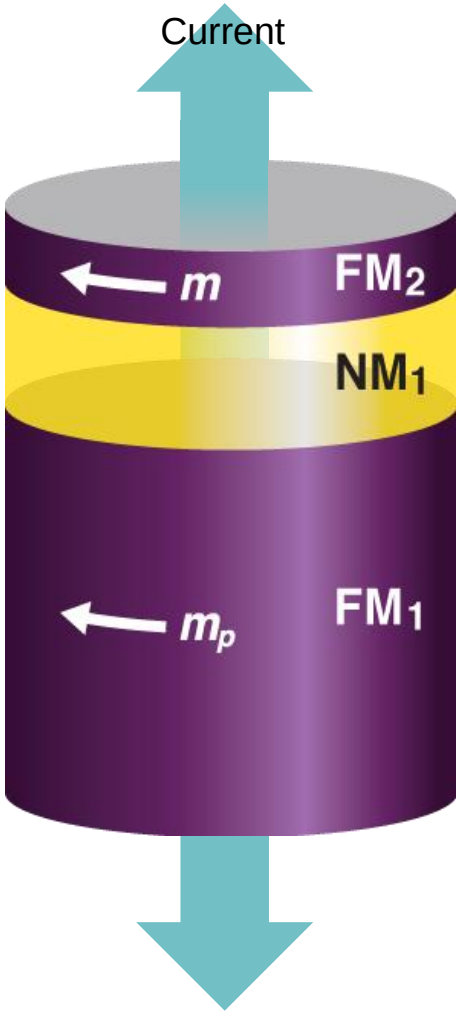
Not to scale

Magnetic Tunnel Junction with Collinear Spin Filter

Magnetic data…'left' or 'right'

Reading - permanent reference direction at low current

Writing - 'collinear spin filter' generates polarization field at high current



"Free" Layer

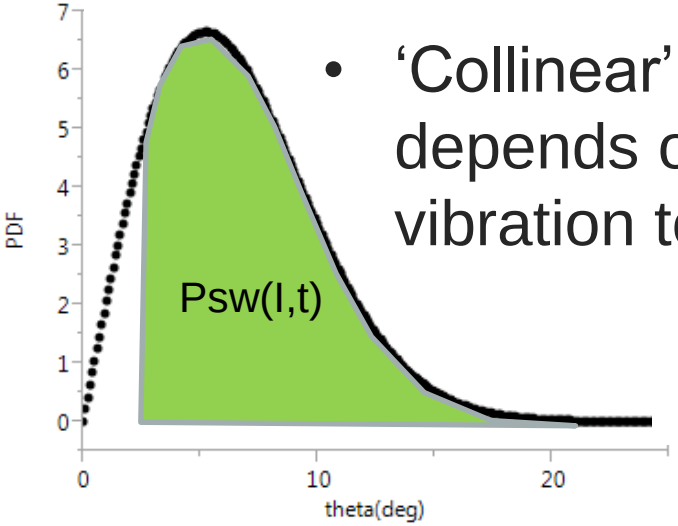
Tunnel Barrier

"Reference" Layer

Not to scale

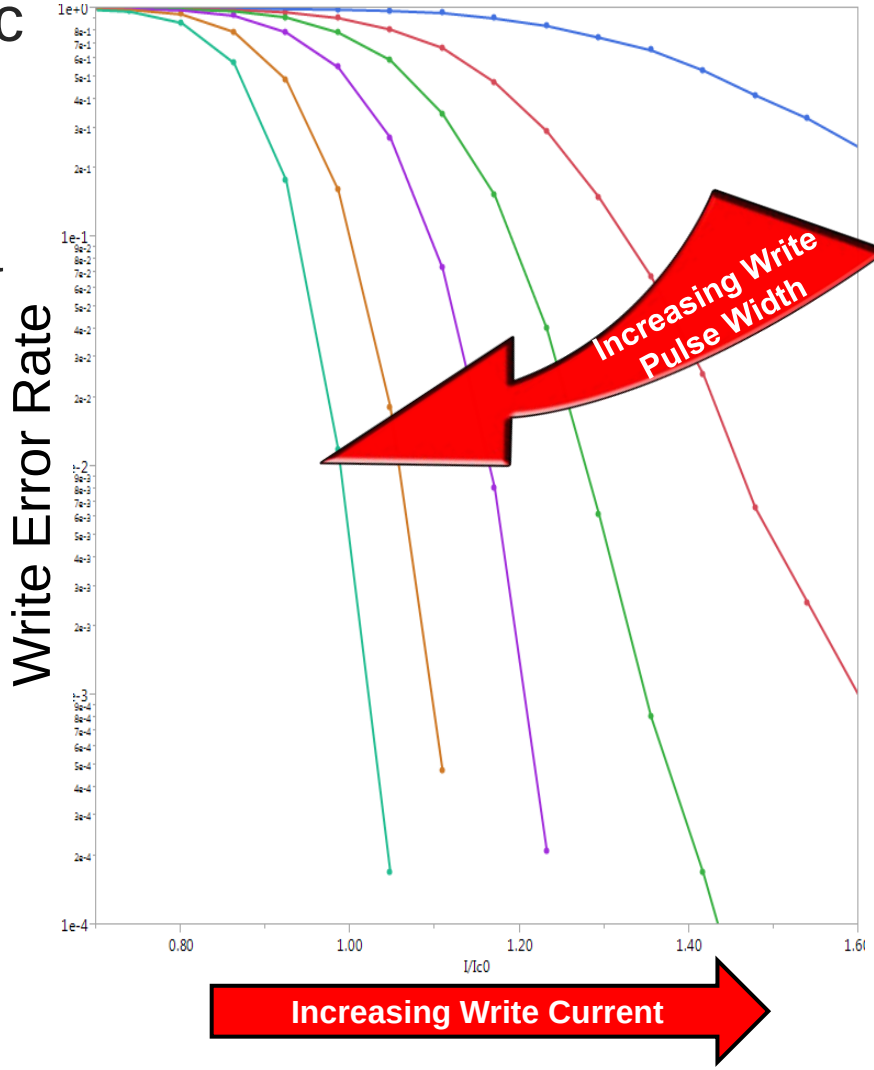
Challenge getting the 'write' started in Collinear Spin Transfer

- Torque on the magnetic storage requires a perpendicular component – just like a compass



Boltzmann thermal distribution of initial angle

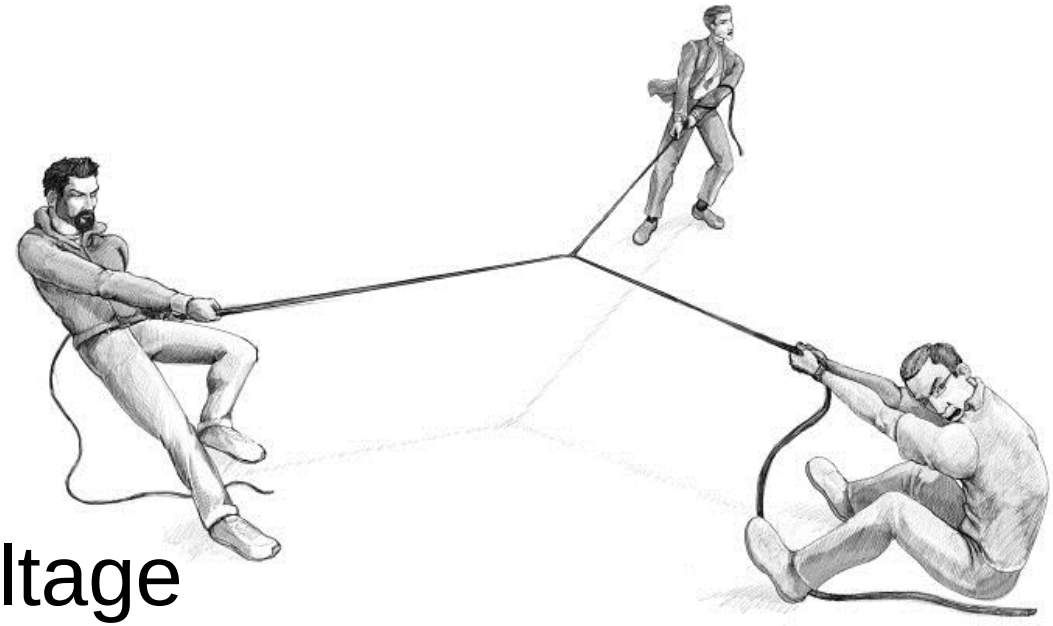
- 'Collinear' switching depends on thermal vibration to get started



Collinear Spin Transfer – In a Performance Box

Write Error Rate (WER)

→Cost, i.e. ECC



Write Voltage

→Power and Endurance

Write Pulse Width

→Performance and Power

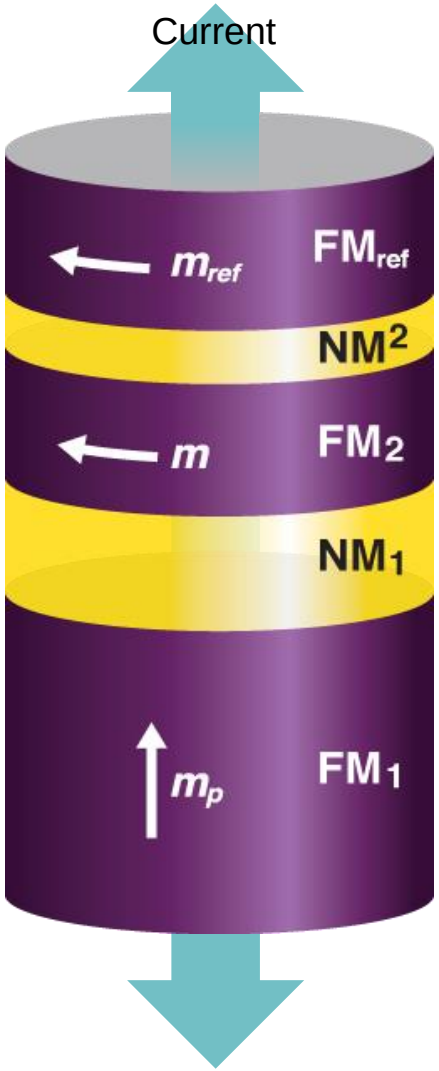
Magnetic Tunnel Junction with Orthogonal Spin Filter

Reading - reference @ low current
Writing - ‘collinear spin filter’ @ high current

Magnetic data…’left’ or ‘right’

Writing - ‘orthogonal spin filter’ @ high current

Strong perpendicular component to ‘spin polarization field’ ***instantaneously*** starts switching of magnetic data in free layer



“Reference” Layer

Tunnel Barrier

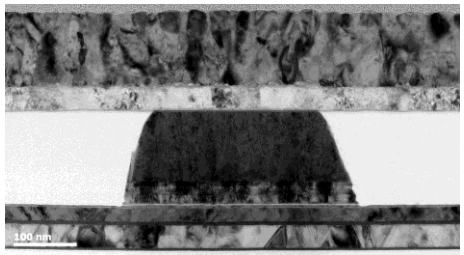
“Free” Layer

Orthogonal Spin Polarization Filter

Not to scale

OST Technology
Benefits And Advantages

Deterministic Write Onset & Shorter Write Pulse



Benefit	Advantage
Faster Write Cycle	5-10x $T_{WriteCycle}$ reduction <5ns writing High Speed RAM Application
Lower Write Energy	5-10x power reduction
Less Oxide Stress	>>10x write endurance advantage
Less Peak Current to Switch With Low Error Rate	Smaller CMOS cell transistor → Lower cost per bit
Lower Write Error Rate per Write Time	Scales to smaller lithography with higher speed and lower write energy

Technology *Benefit* *Advantage*

NVM Futures Panel

Crossbar Resistive RAM (RRAM)

Enabling New Generation of Extremely Dense and High Performance Solid-State Storage

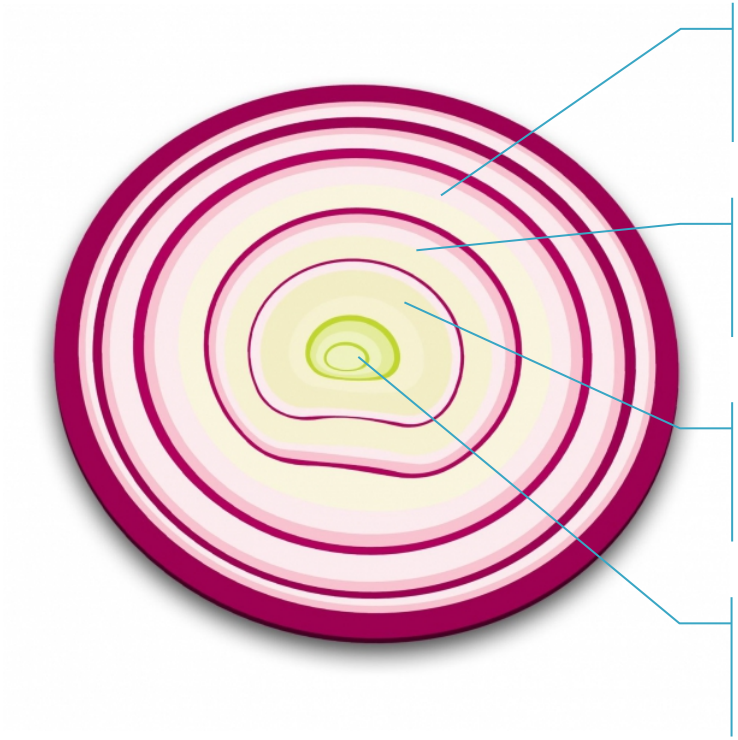
Tanmay Kumar
VP Device Engineering

www.crossbar-inc.com

Confidential

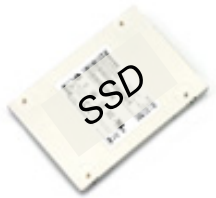
From storage solutions to memory cell technology

Peeling the onion of storage solutions

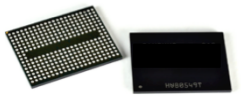


Storage solution
e.g. 24 SSDs in 2U server

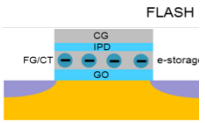
Solid-State Drives
e.g. NVMe controller + DRAM + 8 memory chips



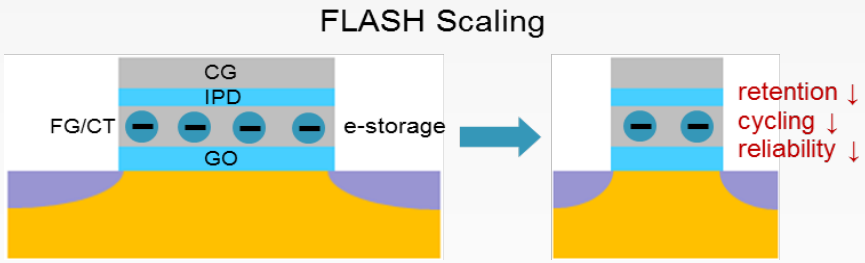
Memory chips
e.g. 8 dies of 128Gbit 3D-NAND TLC

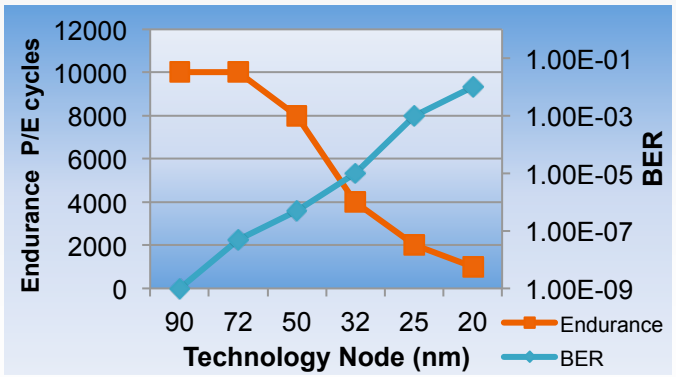


Memory cell technology
e.g. Flash, RRAM, MRAM

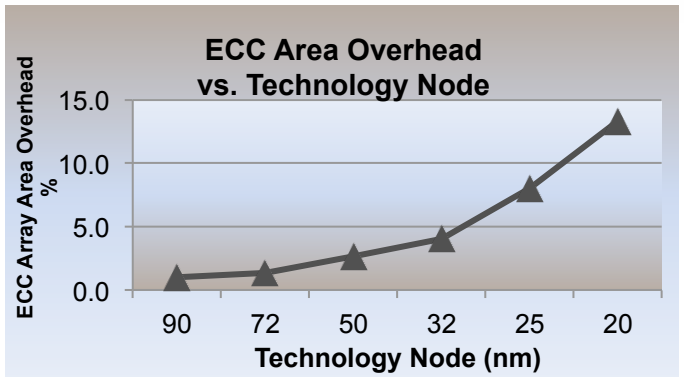


Challenges in Flash scalability path

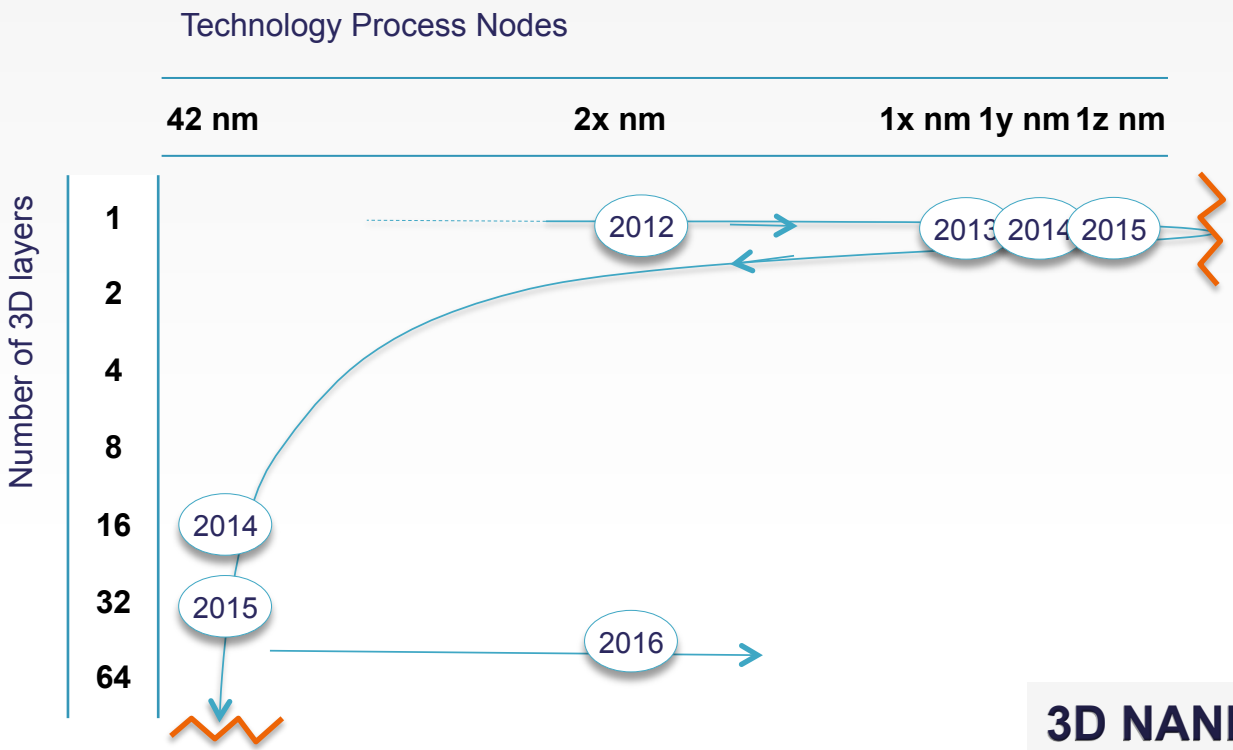




- Information storage in Flash is based on charge density (C/cm^2)
- At 20nm, ~100 electrons are stored in the FG (ΔVt = 1V)
- Losing a few electrons can cause severe reliability issues
- 3D Flash manufacturing challenges impact cost (2x Fab cost)
- **Scaling causes exponentially increasing BER, reduced reliability and cycling and deteriorating performances**



Flash Technology is Running out of Steam



Flash Scalability Challenges

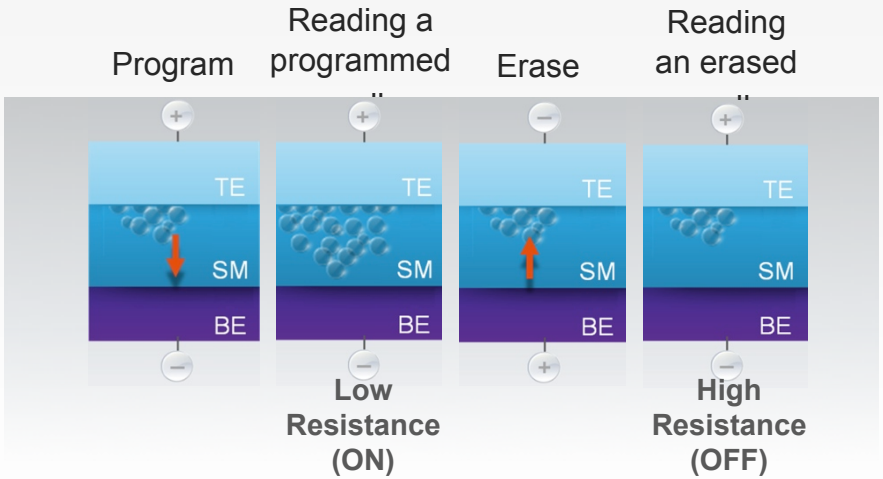
> *The current storage medium, planar NAND, is seeing challenges as it reaches the lower lithographies, pushing against physical and engineering limits.*
> **- Michael Yang**

3D Flash Manufacturing Challenges

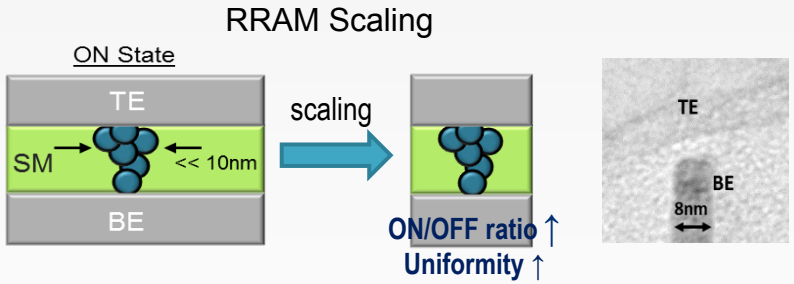
> *The investment in a 100k wpm 32 layer 3D NAND fab is 80-100% or more than a similar sized 16nm 2D NAND fab*
> **- Forward Insights**

3D NAND will replace 2D by 2016
3D NAND is already facing same scalability challenges as planar NAND

Long-term Scalability Path with Crossbar RRAM



- CMOS Fab friendly materials and process
- Standard semiconductor manufacturing equipment
- Back-End-Of-Line standard CMOS integration
- RRAM layer(s) on top of CMOS logic wafers



- Information is stored in the form of metallic nano-filament in a non-conducting layer
- Below 10nm, on/off current ratio exceeds 10,000x
- Increasing on/off ratio enables reliable scaling path options: increasing memory effect with reduced operating voltage and faster switching
- **Scaling improves increased on/off ratio therefore improved reliability**

Crossbar RRAM Proven Advantages vs. NAND Flash

Characteristics	NAND	Crossbar RRAM	Comments
Effective Cell Size (SLC)	5.44F^2	4.28F^2	RRAM provides better array efficiency and smaller die size
Technology Scalability	Severe limitations below 20 nm	Scales <10nm	Scales since it is filament based memory
Page Size	8~32KBytes	2KBytes	Smaller page sizes improves system performance
Read Latency	50~75us	20ns Embedded 5us Mass Storage	RRAM supports code execution
Page Program	2.2ms per 16KBytes	16us per 2KBytes 128us per 16KBytes	RRAM has faster performance
Erase Block	10ms	Not Applicable	RRAM Improves system performance
Byte Program	Not Available	Available	RRAM Improves system performance
RBER	1E-03 ~ 1E-02	< 1E-06	RRAM scales without performance degradation
Data Retention	1 year	10 years	RRAM has significant advantages in retention
Endurance	<3K ~ <1K cycles	10K cycles	RRAM has significant advantages in endurance cycles
Process Complexity	Complex FEOL. Periphery High Voltage transistors do not scale	Simpler BEOL Compatible with CMOS tech scaling	RRAM is stacked on standard CMOS technology Easier to integrated and scale

Crossbar RRAM Ready for Commercialization

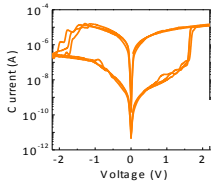
Physics
Fundamental Physics
Characterization

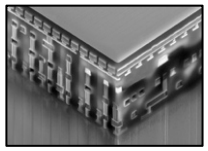
Products
Repeatable Arrays
Integrated Products

Fab Transfer
Optimization
High-Volume Partner

Commercialization
Design and Qualification
Go to Market

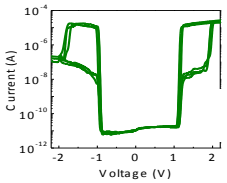
Demonstration of successful Crossbar RRAM + CMOS integration

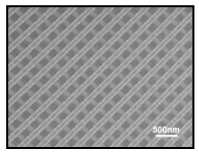




✓ **Proving our RRAM technology**
Enabling cost- efficient fast read array

Demonstration of successful Selector + RRAM integration





✓ **Proving scalability to ultra-high density and low power RRAM storage device**
Solving the sneak path current challenge of crosspoint arrays

Crossbar achieved another major milestone needed to bring high-density low power 3D Resistive RAM to market


Crossbar

MRAM TO THE MAINSTREAM

January 2015

SNIA NVM Summit January 20, 2015

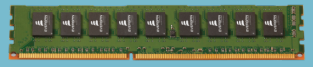
Memory Industry Challenge, Everspin Solution, Market, & Customers

CHALLENGE

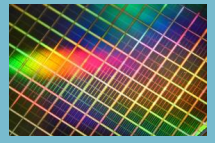
RAM is volatile… and Flash is slow.
The World needs a Fast, Robust, and
Versatile Non-Volatile Memory…
fueled by an *Experienced Company*…
and *Scalable* to the Mainstream Market.

SOLUTION

Discrete MRAM



Modular MRAM



Embedded MRAM

MARKET

MRAM
Over $2B
By 2019*

MRAM	Industrial/Auto ($0.3B)
ST-MRAM	Drives ($1.2B)
ST-MRAM	I/O Accelerators ($0.6B)
ST-MRAM	Storage ($0.2B)
ST-MRAM	Server ($0.1B)

CUSTOMERS

LSI, DELL, AIRBUS, BUFFALO, skyera, AEWIN, SIEMENS, EMERSON, BMW

EVERSPIN TECHNOLOGIES
The MRAM Company™

MRAM (Field-Switched)

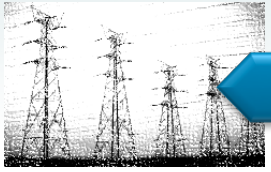
ST-MRAM (Spin Torque)

256K MRAM
1M MRAM
4M MRAM
16M MRAM
16M QSPI (in dev)
64M DDR3
256M (in dev)
1Gb (in dev)
4Gb (future)

Instantly Recoverable Transportation

Everlasting & Resilient Medical Equipment

Fault-Recoverable Industrial Automation

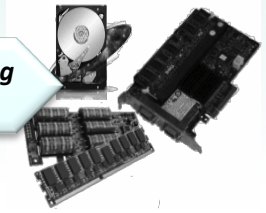


Secure & Reliable Smart Grid

Immediately Reliable Storage, File, & Backup Systems

Rapidly Proficient Enterprise Storage & Networks

Power Fail Safe, Write Caching for HDD and RAID



$0.3B TAM **$2B TAM**

ST-MRAM Design-In Ecosystem

- Ramping to Production with ST-MRAM
  - Mangstor accelerates Enterprise nvm EXPRESS™ Storage devices with ST-MRAM from Everspin
  - Buffalo memory announced SATA III SSD with ST-MRAM cache

BUFFALO Mangstor

- Delivered *NV*DIMM modules in a FPGA based evaluation platform

- Enabling system design with ST-MRAM compatible DDR3 controllers
  - Cadence Denali DDR3 supports Everspin ST-MRAM
  - Altera FPGA DDR3 controller available
  - Accelerated PCIe / NVMe Development through SMART
  - Working with major SSD controller IP providers and microprocessor solutions

SMART® Modular Technologies cadence™ NORTHWEST LOGIC ALTERA mobiveil Investors in Innovation™

ST-MRAM Use Cases

- Persistent DRAM for Storage Applications
  - Write Buffer for Flash Arrays/SSD
    - Small buffer of 40MB to 128MB provides inherent protection of data not committed to Flash
    - Table storage
  - RAID Cache
    - 512MB to 1GB of persistent write cache

      Hybrid memory with DRAM on DDR3 or DDR4 channel
  - Storage Server Cache -1GB/4GB/8GB as ST-MRAM Gigabit+ chips emerge
    - Critical metadata, last write protection, fast reboot from the memory channel
    - Inherent NVDIMM without SuperCap or backup routine
    - Hybrid memory system ST-MRAM + DRAM, OS can use memory as storage
- Enterprise HDD data protection on power loss
  - Serial interface to µP/SoC with very fast writes to capture data in flight

EVERSPIN® TECHNOLOGIES
The MRAM Company™

THANK YOU

STORAGE INDUSTRY SUMMIT

Realizing the Benefits of the Convergence of Storage and Memory

JANUARY 20, 2015, SAN JOSE, CA

Saul Zales

Contour Semiconductor

President & CEO

DTM™ Technology– Driving NVM Economics

SNIA™

Solid State Storage Initiative

Background

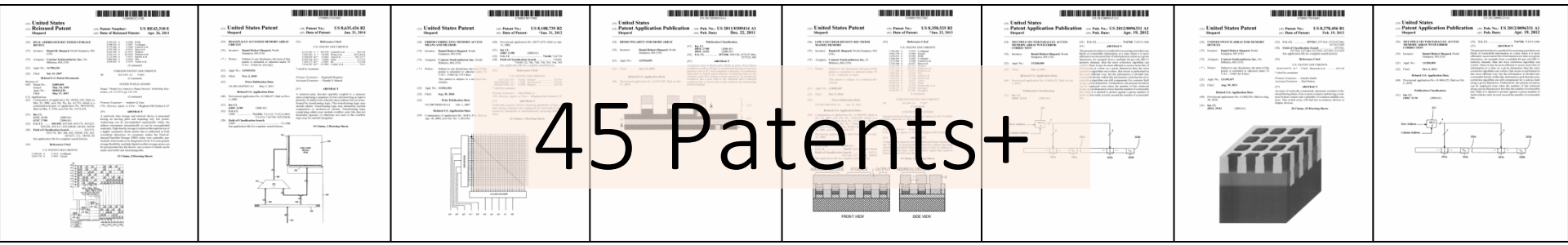
SNIA™
Solid State Storage Initiative

- Founded in 2001
- 1st VC Funding in 2004
- Focused on Delivering Streamlined NVM
- N. Billerica, MA & San Jose, CA
- 3rd Generation Development – 4Gb @ 52nm

DTM Technology Overview

SNIA™ Solid State Storage Initiative

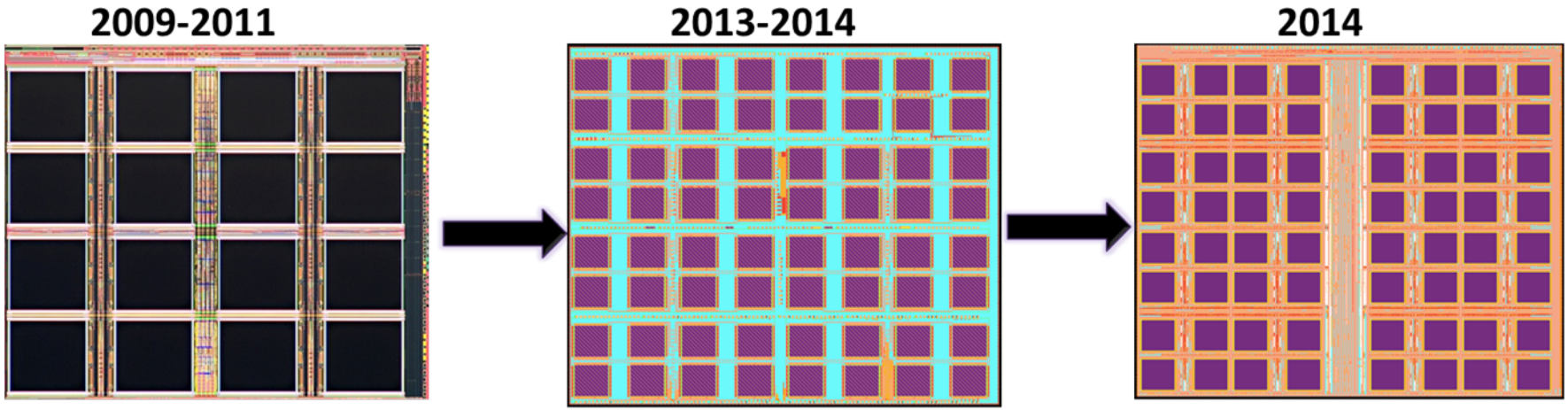
- DTM = Diode Transistor Memory
- Innovative Low-Mask Count Architecture
- High Density NAND-like Memory
- Granular Cross-Point Array
- Proven Phase-Change Technology



DTM Technology

SNIA™
Solid State Storage Initiative

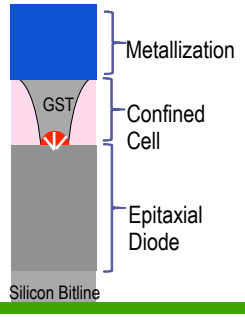
- Epi Diode: $4F^2$ Cell Size, Density
- Efficient Memory Cell: Very Low iReset
- Streamlined Architecture: Reduced CapEx
- Now Debugging 4Gb Component

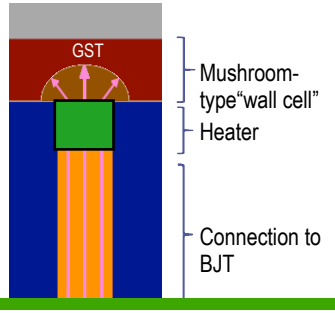


Contour PCM Architecture – Big Leap Forward

SNIA™ Solid State Storage Initiative

	Contour Semi	Micron
Technology Node	45/52nm	45/52nm
# of Masks	16→14	>35??
Select Device	Epi Diode	BJT
Ireset	35-100uA	200-400uA
Density	4Gb	1Gb
Die Area/Gb	30mm²/Gb	36mm²/Gb
Interface	NAND	LPDDR





4x the Density, 3.3x the Area
<¼ Ireset, <½ the Masks

Streamlining Production Drives NVM Economics