VM Futures Panel: Are We Near the Beginning of a New Solid State Epoch, or Is That Just a Big Fireball in the Sky?

• Moderator: Tom Coughlin, Coughlin Associates

• Panelists:
  – Dave Eggleston, Intuitive Cognition Consulting
  – Barry Hoberman, Spin Transfer Technologies
  – Tanmay Kumar, Crossbar
  – Joseph O'Hare, Everspin
  – Saul Zales, Contour Semiconductor
STORAGE INDUSTRY SUMMIT

Realizing the Benefits of the Convergence of Storage and Memory

JANUARY 20, 2015, SAN JOSE, CA

David Eggleston
Intuitive Cognition Consulting
Principal
Roadmap for New NVM
Looking through the Windshield

- Planar NAND scaling is drawing to a close
- 3D NAND succeeds planar NAND (until 2025)
- So how and where do new NVM technologies fit in?
- Role for new NVM before 2025?
- Requirements for new NVM on the memory bus:
  - 100’s of GB’s to TB’s of capacity (per module)
  - Latencies in the high 100’s of ns to low us
  - Cost <50% of DRAM
  - Bring non-volatility into the cache coherent network
The best opportunity for new NVM over the next 10 years lies between NAND and DRAM, with latency in the low to sub microsecond range.

With system changes, new NVM moves into the working memory space.
New NVM Contenders for this Memory Bus Opportunity Gap

- **Technologies:**
  - **RRAM**
    - 1S-1R Conductive Bridging RAM (CBRAM)
      - Small cell size, but endurance limitations
    - 1R Oxide RRAM (OxRAM)
      - Will be used for 3D data storage in 2021+
      - Dense, but too slow for low latency memory
  - **PCM**
    - 1S-1R Phase Change Memory
      - Scaling challenges, fallen out of favor?
  - **ST-MRAM**
    - 1T-1MTJ ST-MRAM
      - Great performance and endurance, but cell size limitations
Barriers to New NVM Adoption

- Lots of money to be made on NAND and DRAM.
- Investments are in 3D NAND manufacturing, not in new NVM manufacturing.
- Intense material science, takes a very long time.
- Process integration is challenging and expensive.
- New NVM will be imperfect memory, and will require controller technology.
- New system architectures that accept memory non-deterministic behavior must be deployed.
Don’t want to wait?

- Combinations of DRAM and Flash on modules solve some of these problems today!
  - NVDIMM-N, NVDIMM-F both available now

- Expect new NVM (low latency memory) to arrive on modules by 2018.

- SNIA NVM-PTWG is paving the way with the programming models – so applications can be aware and take advantage of non-volatility in the system.
Thank you!

DAVID EGGLESTON
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Orthogonal Spin Transfer (OST)
A Better Approach
Company Background

History
- Formed in 2007 by Allied Minds and NYU to commercialize Orthogonal Spin Transfer (OST) MRAM research led by Professor Andrew Kent.
- In 2012, raised $36 million financing, plus additional $70 million in 2014, from Allied Minds, Invesco, & WIM, and established Silicon Valley headquarters.

Technology
- OST-MRAM is a disruptive innovation in the field of spin transfer MRAM devices and offers advantages over other MRAM:
  - Higher speed, lower cost, lower power consumption, higher reliability, and enhanced lithographic scalability.

Opportunity
- Targeted as a replacement for DRAM, SRAM or flash memory.
- Markets in storage systems, mobile devices, computing, microcontrollers and SOCs in standalone or embedded configurations.
OST MRAM
Combining Orthogonal Spin Filter with Collinear MTJ

Conventional Collinear Spin Transfer MTJ Structure

- Magnetic data...'left' or 'right'
- Reading - permanent reference direction at low current
- Writing - 'collinear spin filter' generates polarization field at high current

‘Brand X’

‘Spin Balanced’ Orthogonal Spin Transfer MTJ Structure

- Magnetic data...'left' or 'right'
- Writing - 'orthogonal spin filter' at high current
- Strong perpendicular component to 'spin polarization field' instantaneously starts switching of magnetic data in free layer

‘Spin Transfer Technologies’
Magnetic Tunnel Junction with Collinear Spin Filter

Magnetic data...’left’ or ‘right’

Reading - permanent reference direction at low current

Writing - ‘collinear spin filter’ generates polarization field at high current

Not to scale
Challenge getting the ‘write’ started in Collinear Spin Transfer

- Torque on the magnetic storage requires a perpendicular component – just like a compass
- ‘Collinear’ switching depends on thermal vibration to get started

Boltzmann thermal distribution of initial angle

Increasing Write Current

Increasing Write Pulse Width

Write Error Rate

Psw(I,t)
Collinear Spin Transfer
– In a Performance Box

Write Error Rate (WER)
➔ Cost, i.e. ECC

Write Voltage
➔ Power and Endurance

Write Pulse Width
➔ Performance and Power
Magnetic Tunnel Junction with Orthogonal Spin Filter

Reading - reference @ low current
Writing - ‘collinear spin filter’ @ high current

Magnetic data…’left’ or ‘right’

Writing - ‘orthogonal spin filter’ @ high current

Strong perpendicular component to ‘spin polarization field’ *instantaneously* starts switching of magnetic data in free layer
<table>
<thead>
<tr>
<th>Technology</th>
<th>Benefit</th>
<th>Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deterministic Write Onset &amp;</td>
<td>Faster Write Cycle</td>
<td>5-10x $T_{\text{WriteCycle}}$ reduction</td>
</tr>
<tr>
<td>Shorter Write Pulse</td>
<td></td>
<td>&lt;5ns writing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Speed RAM Application</td>
</tr>
<tr>
<td></td>
<td>Lower Write Energy</td>
<td>5-10x power reduction</td>
</tr>
<tr>
<td></td>
<td>Less Oxide Stress</td>
<td>&gt;&gt;10x write endurance advantage</td>
</tr>
<tr>
<td></td>
<td>Less Peak Current to Switch With Low Error Rate</td>
<td>Smaller CMOS cell transistor → Lower cost per bit</td>
</tr>
<tr>
<td></td>
<td>Lower Write Error Rate per Write Time</td>
<td>Scales to smaller lithography with higher speed and lower write energy</td>
</tr>
</tbody>
</table>
NVM Futures Panel

Crossbar Resistive RAM (RRAM)
Enabling New Generation of Extremely Dense and High Performance Solid-State Storage

Tanmay Kumar
VP Device Engineering

www.crossbar-inc.com
From storage solutions to memory cell technology

Peeling the onion of storage solutions

Storage solution
e.g. 24 SSDs in 2U server

Solid-State Drives
e.g. NVMe controller + DRAM + 8 memory chips

Memory chips
e.g. 8 dies of 128Gbit 3D-NAND TLC

Memory cell technology
e.g. Flash, RRAM, MRAM
Challenges in Flash scalability path

- Information storage in Flash is based on charge density (C/cm²)
- At 20nm, ~100 electrons are stored in the FG (ΔVt = 1V)
- Losing a few electrons can cause severe reliability issues
- 3D Flash manufacturing challenges impact cost (2x Fab cost)
- Scaling causes exponentially increasing BER, reduced reliability and cycling and deteriorating performances
Flash Technology is Running out of Steam

<table>
<thead>
<tr>
<th>Technology Process Nodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>42 nm</td>
</tr>
<tr>
<td>2x nm</td>
</tr>
<tr>
<td>1x nm 1y nm 1z nm</td>
</tr>
</tbody>
</table>

### Flash Scalability Challenges

The current storage medium, planar NAND, is seeing challenges as it reaches the lower lithographies, pushing against physical and engineering limits.

> - Michael Yang

### 3D Flash Manufacturing Challenges

The investment in a 100k wpm 32 layer 3D NAND fab is 80-100% or more than a similar sized 16nm 2D NAND fab.

> - Forward Insights

3D NAND will replace 2D by 2016.

3D NAND is already facing same scalability challenges as planar NAND.
Long-term Scalability Path with Crossbar RRAM

- Information is stored in the form of metallic nano-filament in a non-conducting layer
- Below 10nm, on/off current ratio exceeds 10,000x
- Increasing on/off ratio enables reliable scaling path options: increasing memory effect with reduced operating voltage and faster switching
- **Scaling improves increased on/off ratio therefore improved reliability**

- CMOS Fab friendly materials and process
- Standard semiconductor manufacturing equipment
- Back-End-Of-Line standard CMOS integration
- RRAM layer(s) on top of CMOS logic wafers
## Crossbar RRAM Proven Advantages vs. NAND Flash

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>NAND</th>
<th>Crossbar RRAM</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Effective Cell Size (SLC)</td>
<td>5.44F²</td>
<td>4.28F²</td>
<td>RRAM provides better array efficiency and smaller die size</td>
</tr>
<tr>
<td>Technology Scalability</td>
<td>Severe limitations below 20 nm</td>
<td>Scales &lt;10nm</td>
<td>Scales since it is filament based memory</td>
</tr>
<tr>
<td>Page Size</td>
<td>8~32KBytes</td>
<td>2KBytes</td>
<td>Smaller page sizes improves system performance</td>
</tr>
<tr>
<td>Read Latency</td>
<td>50~75us</td>
<td>20ns Embedded 5us Mass Storage</td>
<td>RRAM supports code execution</td>
</tr>
<tr>
<td>Page Program</td>
<td>2.2ms per 16KBytes</td>
<td>16us per 2KBytes 128us per 16KBytes</td>
<td>RRAM has faster performance</td>
</tr>
<tr>
<td>Erase Block</td>
<td>10ms</td>
<td>Not Applicable</td>
<td>RRAM Improves system performance</td>
</tr>
<tr>
<td>Byte Program</td>
<td>Not Available</td>
<td>Available</td>
<td>RRAM Improves system performance</td>
</tr>
<tr>
<td>RBER</td>
<td>1E-03 ~ 1E-02</td>
<td>&lt; 1E-06</td>
<td>RRAM scales without performance degradation</td>
</tr>
<tr>
<td>Data Retention</td>
<td>1 year</td>
<td>10 years</td>
<td>RRAM has significant advantages in retention</td>
</tr>
<tr>
<td>Endurance</td>
<td>&lt;3K ~ &lt;1K cycles</td>
<td>10K cycles</td>
<td>RRAM has significant advantages in endurance cycles</td>
</tr>
<tr>
<td>Process Complexity</td>
<td>Complex</td>
<td>Simpler</td>
<td>RRAM is stacked on standard CMOS technology Easier to integrated and scale</td>
</tr>
</tbody>
</table>

FEOL. Periphery High Voltage transistors do not scale
BEOL Compatible with CMOS tech scaling
Crossbar RRAM Ready for Commercialization

- **Physics**
  - Fundamental Physics Characterization
- **Products**
  - Repeatable Arrays
  - Integrated Products
- **Fab Transfer**
  - Optimization
  - High-Volume Partner
- **Commercialization**
  - Design and Qualification
  - Go to Market

**Demonstration of successful Crossbar RRAM + CMOS integration**

- Proving our RRAM technology
  - Enabling cost-efficient fast read array

**Demonstration of successful Selector + RRAM integration**

- Proving scalability to ultra-high density and low power RRAM storage device
  - Solving the sneak path current challenge of crosspoint arrays

Crossbar achieved another major milestone needed to bring high-density low power 3D Resistive RAM to market
MRAM TO THE MAINSTREAM
Memory Industry Challenge, Everspin Solution, Market, & Customers

**CHALLENGE**
RAM is volatile... and Flash is slow. The World needs a Fast, Robust, and Versatile Non-Volatile Memory... fueled by an Experienced Company... and Scalable to the Mainstream Market.

**SOLUTION**
- Discrete MRAM
- Modular MRAM
- Embedded MRAM

**MARKET**
- MRAM
- ST-MRAM
- Industrial/Auto ($0.3B)
- Drives ($1.2B)
- I/O Accelerators ($0.6B)
- Storage ($0.2B)
- Server ($0.1B)
- Over $2B By 2019*

**CUSTOMERS**
- LSI
- skyera
- DELL
- AIRBUS
- AEWIN
- EMERSON
- SIEMENS
- BUFFALO
- BMW

SNIA NVM Summit  1/20/2015
Instantly Recoverable Transportation

Everlasting & Resilient Medical Equipment

Fault-Recoverable Industrial Automation

Secure & Reliable Smart Grid

Immediately Reliable Storage, File, & Backup Systems

Rapidly Proficient Enterprise Storage & Networks

Power Fail Safe, Write Caching for HDD and RAID

$0.3B TAM

$2B TAM

SNIA NVM Summit 1/20/2015
ST-MRAM Design-In Ecosystem

- Ramping to Production with ST-MRAM
  - Mangstor accelerates Enterprise Storage devices with ST-MRAM from Everspin
  - Buffalo memory announced SATA III SSD with ST-MRAM cache

- Delivered NVDIMM modules in a FPGA based evaluation platform

- Enabling system design with ST-MRAM compatible DDR3 controllers
  - Cadence Denali DDR3 supports Everspin ST-MRAM
  - Altera FPGA DDR3 controller available
  - Accelerated PCIe / NVMe Development through SMART
  - Working with major SSD controller IP providers and microprocessor solutions
ST-MRAM Use Cases

- **Persistent DRAM for Storage Applications**
  - Write Buffer for Flash Arrays/SSD
    - Small buffer of 40MB to 128MB provides inherent protection of data not committed to Flash
    - Table storage
  - RAID Cache
    - 512MB to 1GB of persistent write cache
      - Hybrid memory with DRAM on DDR3 or DDR4 channel
  - Storage Server Cache - 1GB/4GB/8GB as ST-MRAM Gigabit+ chips emerge
    - Critical metadata, last write protection, fast reboot from the memory channel
    - Inherent NVDIMM without SuperCap or backup routine
    - Hybrid memory system ST-MRAM + DRAM, OS can use memory as storage

- **Enterprise HDD data protection on power loss**
  - Serial interface to µP/SoC with very fast writes to capture data in flight
Saul Zales
Contour Semiconductor
President & CEO

DTM™ Technology—Driving NVM Economics
Background

- Founded in 2001
- 1st VC Funding in 2004
- Focused on Delivering Streamlined NVM
- N. Billerica, MA & San Jose, CA
- 3rd Generation Development – 4Gb @ 52nm
DTM Technology Overview

- DTM = Diode Transistor Memory
- Innovative Low-Mask Count Architecture
- High Density NAND-like Memory
- Granular Cross-Point Array
- Proven Phase-Change Technology

45 Patents+
DTM Technology

- Epi Diode: $4F^2$ Cell Size, Density
- Efficient Memory Cell: Very Low iReset
- Streamlined Architecture: Reduced CapEx
- Now Debugging 4Gb Component

Contour PCM Architecture – Big Leap Forward

<table>
<thead>
<tr>
<th></th>
<th>Contour Semi</th>
<th>Micron</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Node</td>
<td>45/52nm</td>
<td>45/52nm</td>
</tr>
<tr>
<td># of Masks</td>
<td>16→14</td>
<td>&gt;35??</td>
</tr>
<tr>
<td>Select Device</td>
<td>Epi Diode</td>
<td>BJT</td>
</tr>
<tr>
<td>Ireset</td>
<td>35-100uA</td>
<td>200-400uA</td>
</tr>
<tr>
<td>Density</td>
<td>4Gb</td>
<td>1Gb</td>
</tr>
<tr>
<td>Die Area/Gb</td>
<td>30mm²/Gb</td>
<td>36mm²/Gb</td>
</tr>
<tr>
<td>Interface</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- NAND
  - Silicon Bitline
  - Epitaxial Diode
  - Confined Cell
  - GST
  - Metallization

- LPDDR
  - Mushroom-type “wall cell” heater
  - Connection to BJT

4x the Density, 3.3x the Area
<¼ Ireset, <½ the Masks
Streamlining Production Drives NVM Economics

- **Masks**
  - 51nm - SS - NAND
  - 52nm - Contour - DTM
  - 48nm - SS - DRAM

- **Process Steps**

![Bar chart showing the comparison between Masks and Process Steps for different processes.]