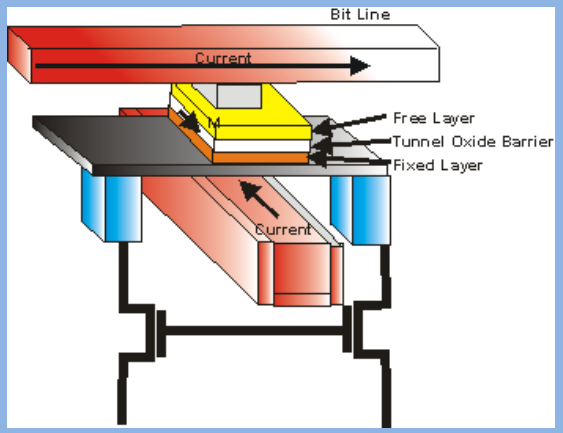
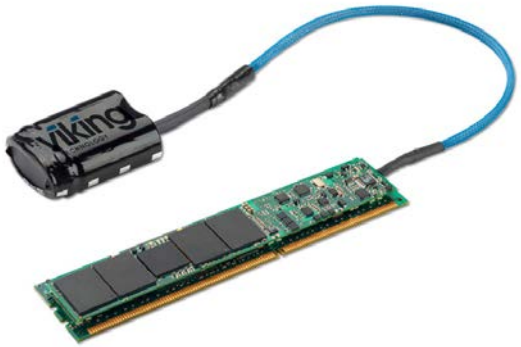
Thanks for the Memories: Emerging Non-Volatile Memory Technologies



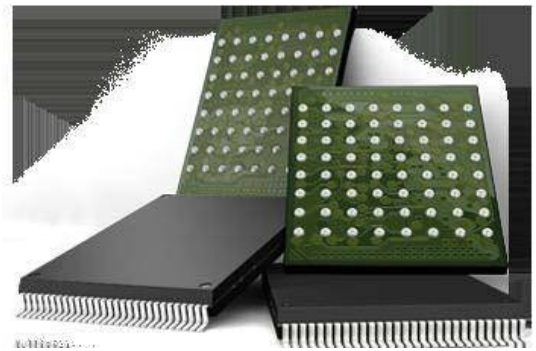
- Tom Coughlin, Coughlin Associates
- Ed Grochowski, Computer Storage Consultant

Outline

- The Promise of Non-Volatile Memory
- Non-Volatile Memory Technology
- MRAM Demand and Capital Equipment
- Conclusions

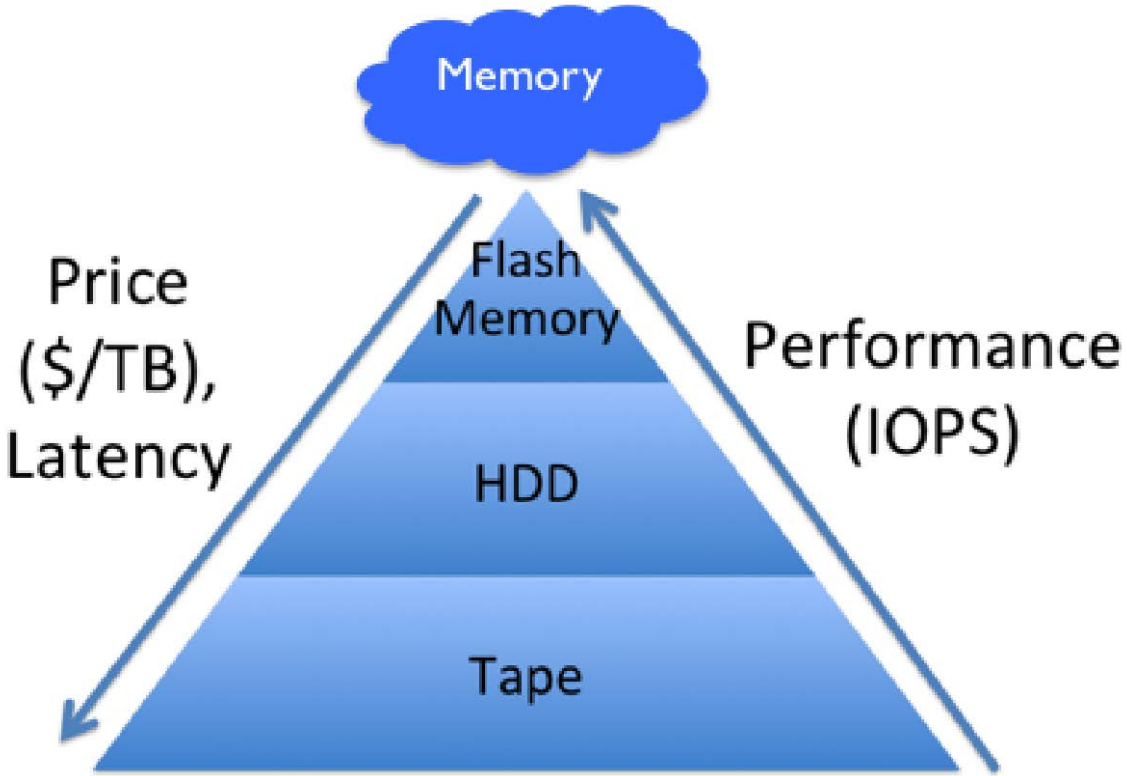


The Promise of Non-Volatile Memory

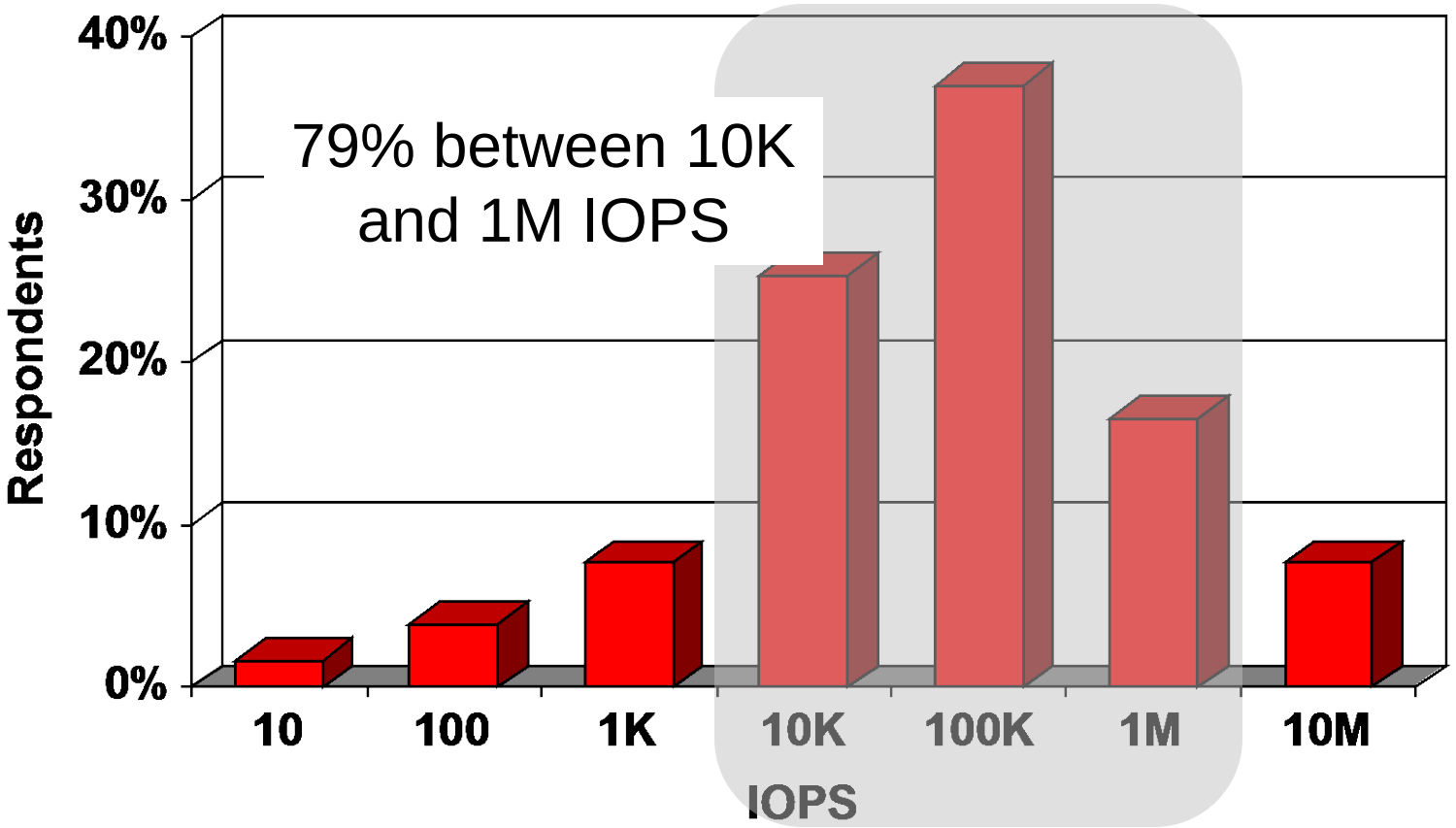


Memory/Storage Hierarchy

- Qualitative trade offs between volatile (and non-volatile) memory and non-volatile storage technology
  - costs to store data ($/TB)
  - performance of the storage technology (IOPS) or data rates).

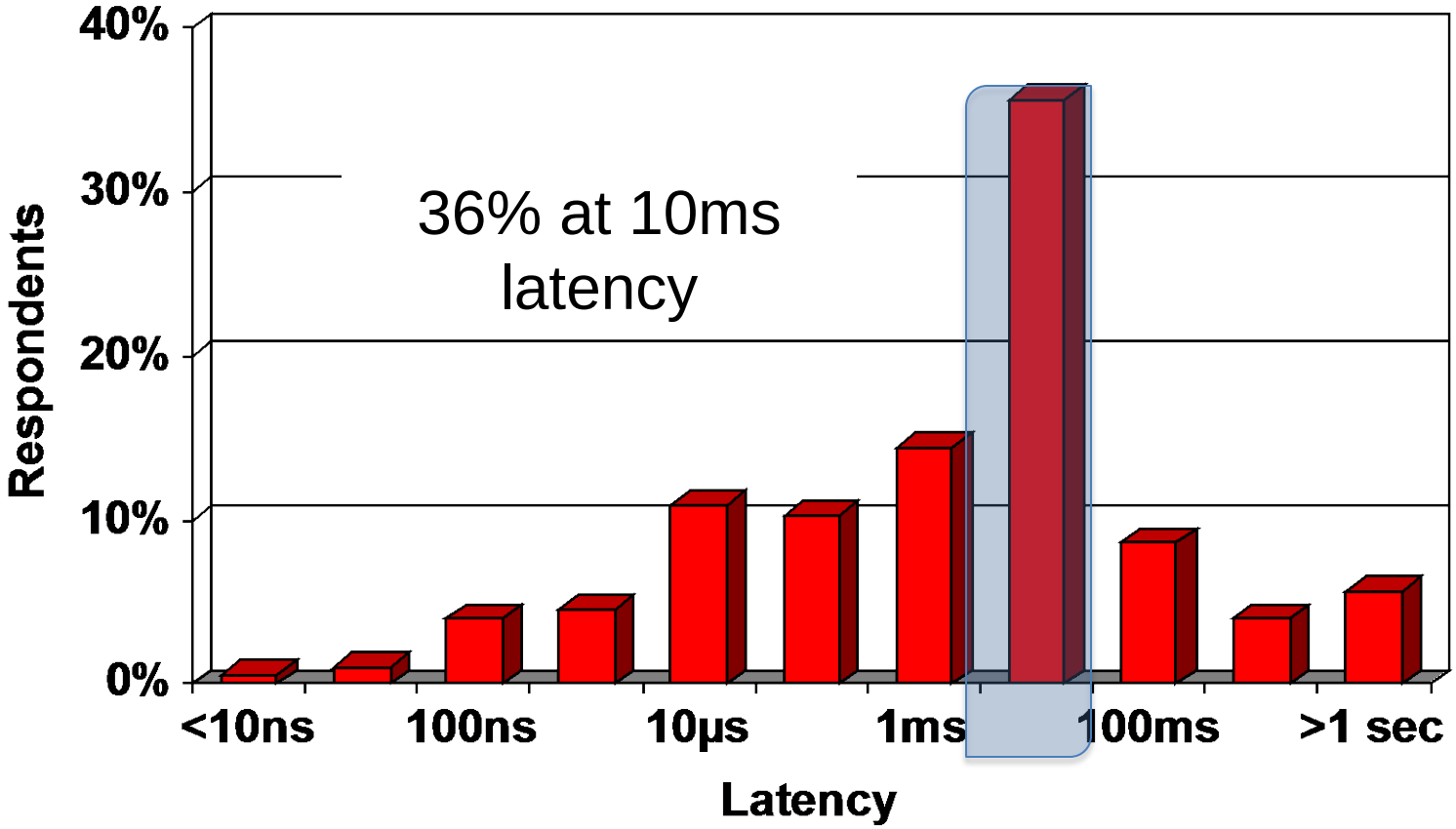


IOPS Required



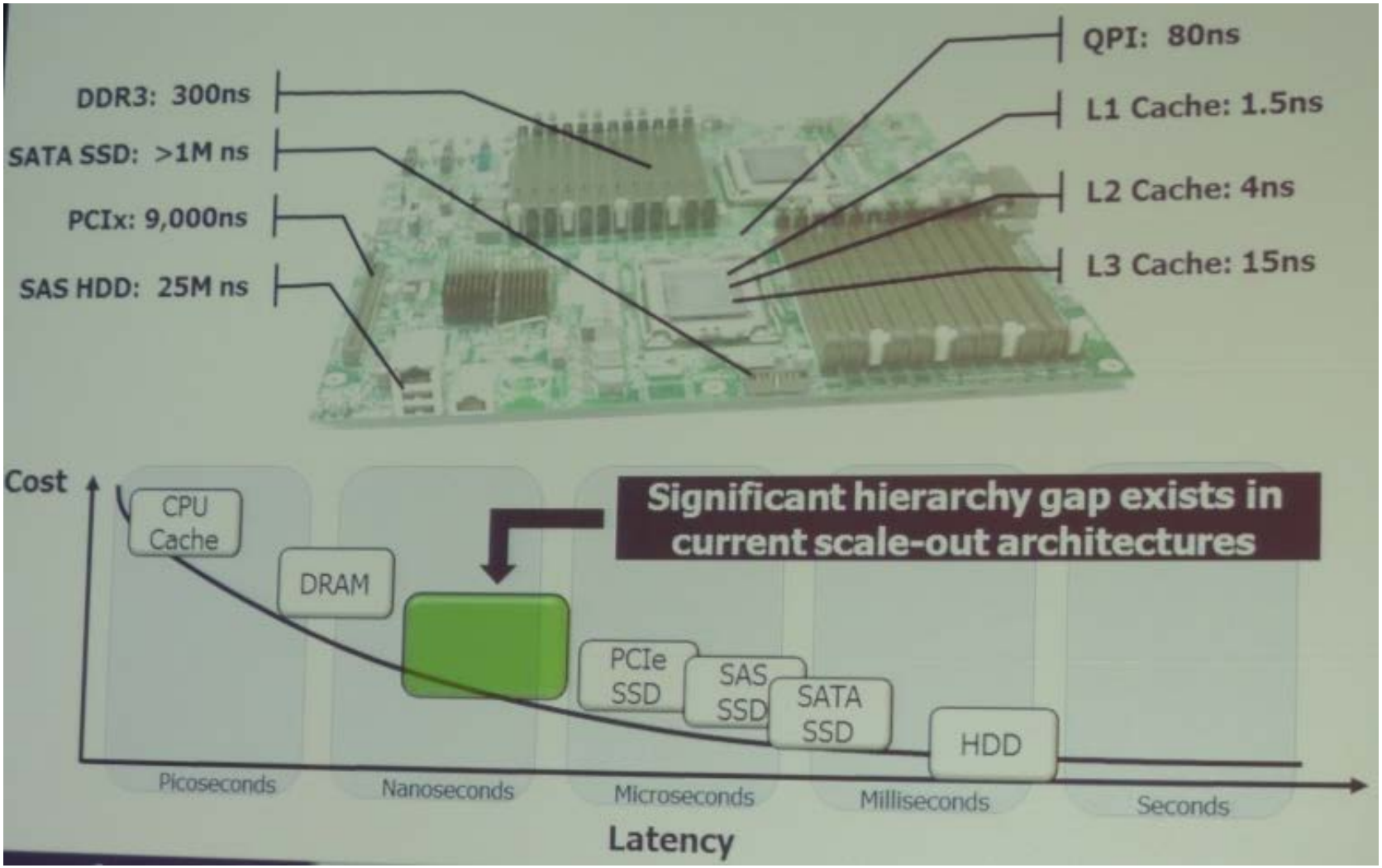
From the 2014 How Many IOPS Do You Really Need Report, Coughlin and Handy, http://www.tomcoughlin.com/techpapers.htm

Minimum Latency Requirement



From the 2014 How Many IOPS Do You Really Need Report, Coughlin and Handy, http://www.tomcoughlin.com/techpapers.htm

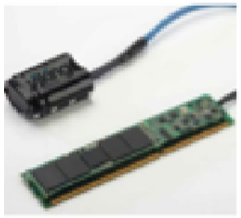
Computer Memory Opportunities
(from SNIA Winter Symposium)



Progression of Storage Technologies with Non-Volatile Solid State Storage

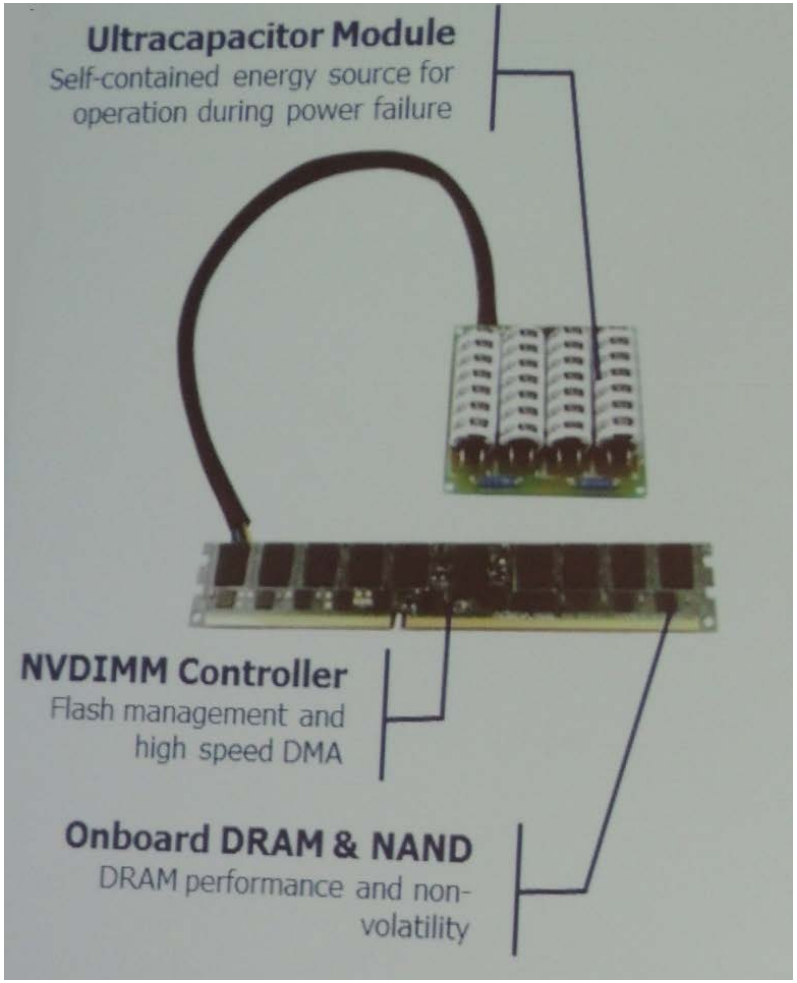
(Presentation by Tony Roug of Intel at a SNIA SSSI meeting in January 2013)

Standard SATA, SAS, FC HDDs	*Standard SATA, SAS, FC SSDs*	*PCIe Proprietary, NVMe, SCSIe Solid State Storage (SSS)*	*Emerging Persistent Memory (PM)*



Best Capacity Per Cost	Higher IOPS Lower Latency Lower Power	Optimized Flash Storage

NVDIMM Activities



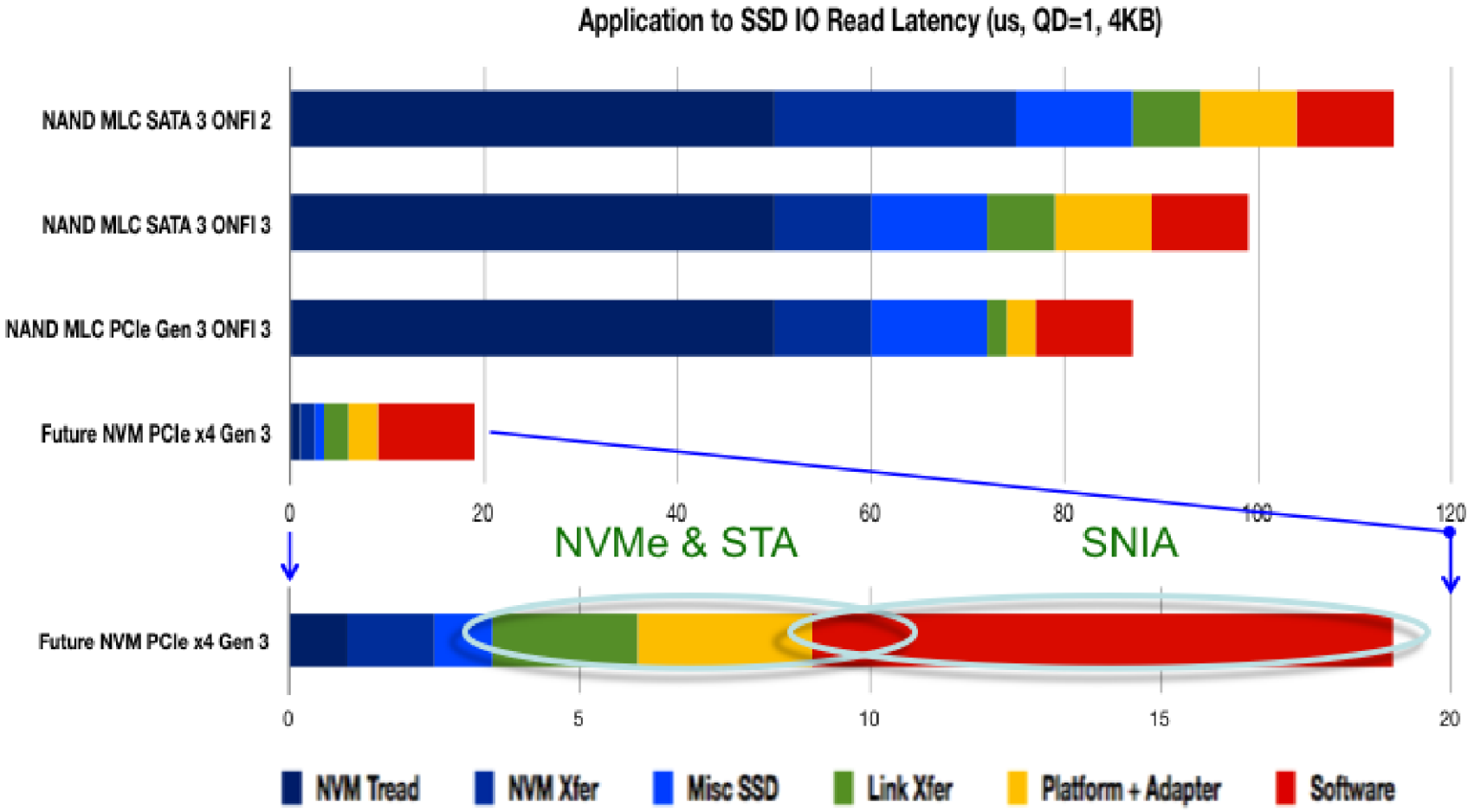
- NVDIMM Activity (image from SNIA Winter Symposium)
- Shows NVDIMM Controller with Ultracapacitors to complete writes if power is lost
- SNIA NVDIMM Working Group

Implications of Persistent Memory

- NV memory retains its data even when power off—thus instant recovery of state before power down is now possible
- NV memory with the right SW changes can provide much better latencies than current systems and SW
- Non-volatile memory will save power since refreshes not needed
- Persistent memory creates new opportunities to share that memory between different computers or computer chips using Remote Direct Memory Access (RDMA)
- Embedded NVM technology can lead to “logic-in-memory architecture” for future SoC—this can lead to new distributed computer architectures

Storage Latency Storage Latency with Current and Future NV Solid State NV Technologies

(from NVMP talk at SNIA Winter Symposium.

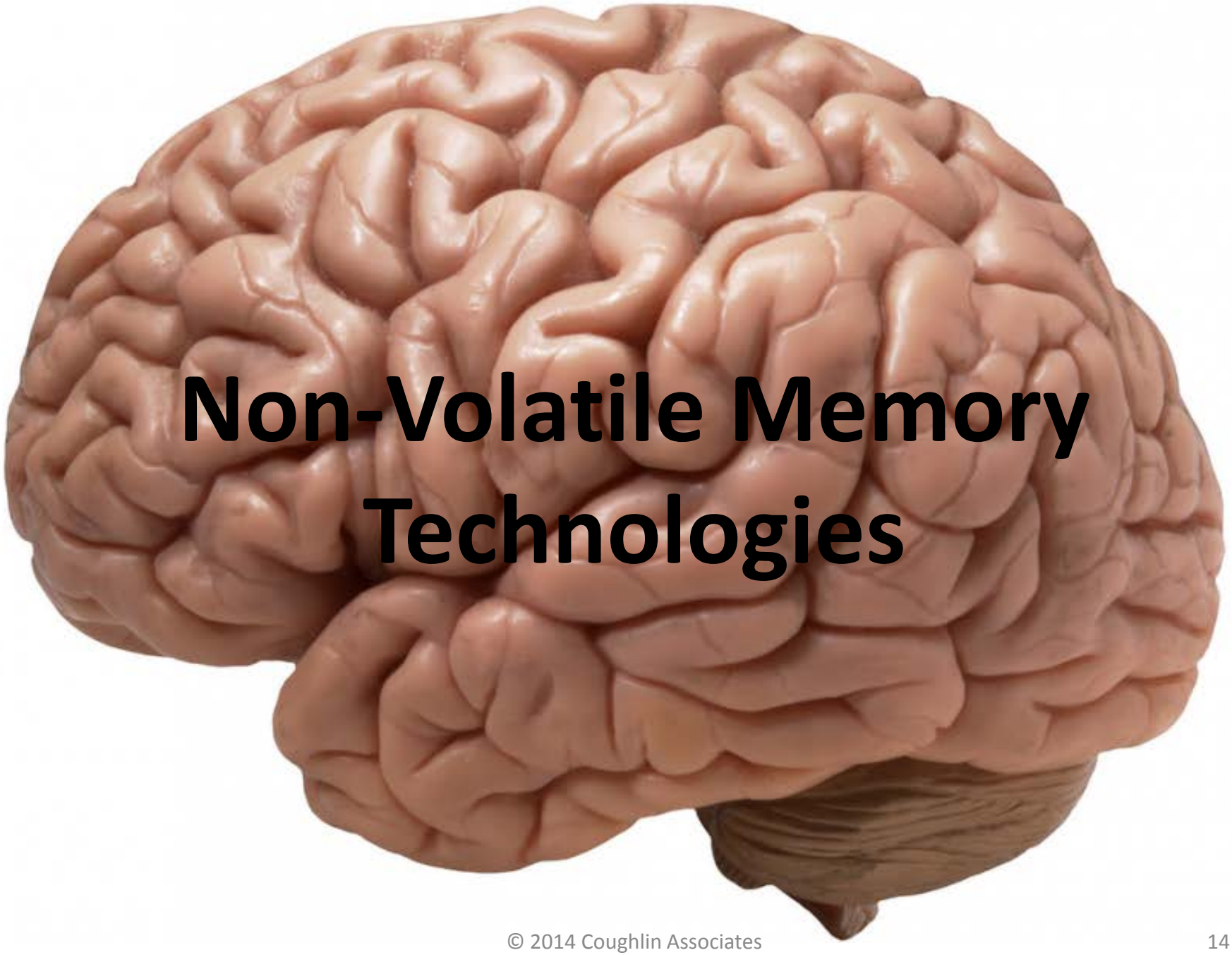


Science Fiction Into Reality

- Enable new industries and applications.
  - The development of an Internet of Things (IoT) that will make social networking extend to the things we own,
  - Improved network connectivity and data transfers,
  - Accelerate the development of self-driving cars,
  - Help users with disabilities be self-reliant,
  - Provide the technology to capture and store life logs,
  - Create an immersive artificial reality,
  - Popularize mobile device tricorders, and
  - Create a host of things that have been the subjects of Science Fiction, and even things we haven't dreamed of yet.

Challenges Of Persistent Memory

- If the memory isn't cleared by rebooting a system, then reboots to recover functionality with corrupted data won't work
- There will need to be a special reboot and clear function that erases and recovers data in memory
- Or, and this may be an even better solution, we need to built devices and software that are self-monitoring and self correcting so we don't need to reboot in order to retain functionality



Non-Volatile Memory Technologies

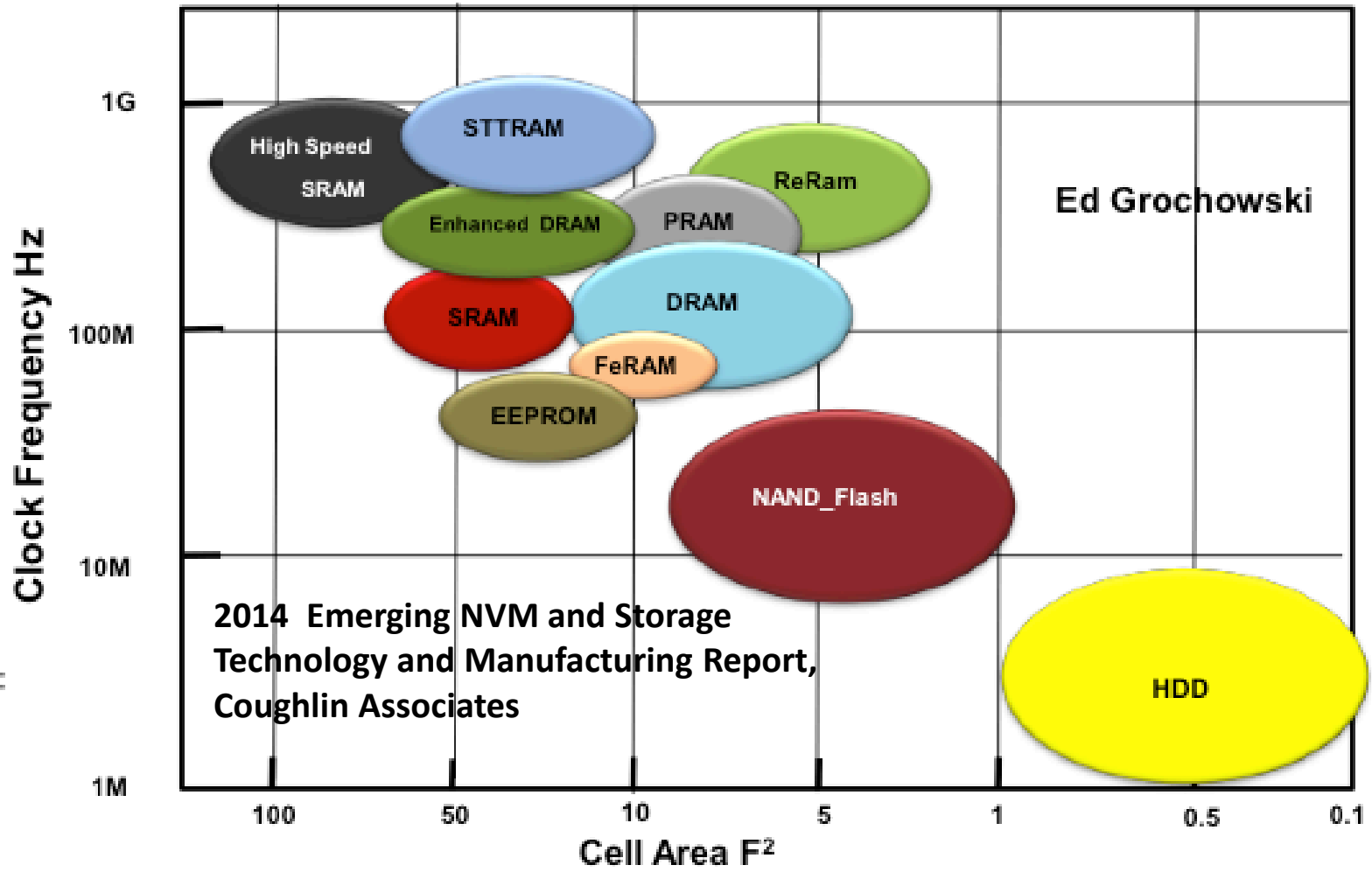
Comparison of Solid-State Memory Technologies (1)

	SRAM	DRAM	NOR Flash	NAND MLC Flash
Non-volatile	N	N	Y	Y
Memory cell factor (F^2)	50-120	6-10	10	4-5
Read time (ns)	1-100	30	10	50
Write/erase time (ns)	1-100	50	$10^5/10^7$	$10^6/10^5$
Number of rewrites	10^{16}	10^{16}	10^5	10^3
Power consumption at write	Low	Low	High	Med
Required input voltage (V)	None	2	6-8	1.8

Comparison of Solid-State Memory Technologies (2)

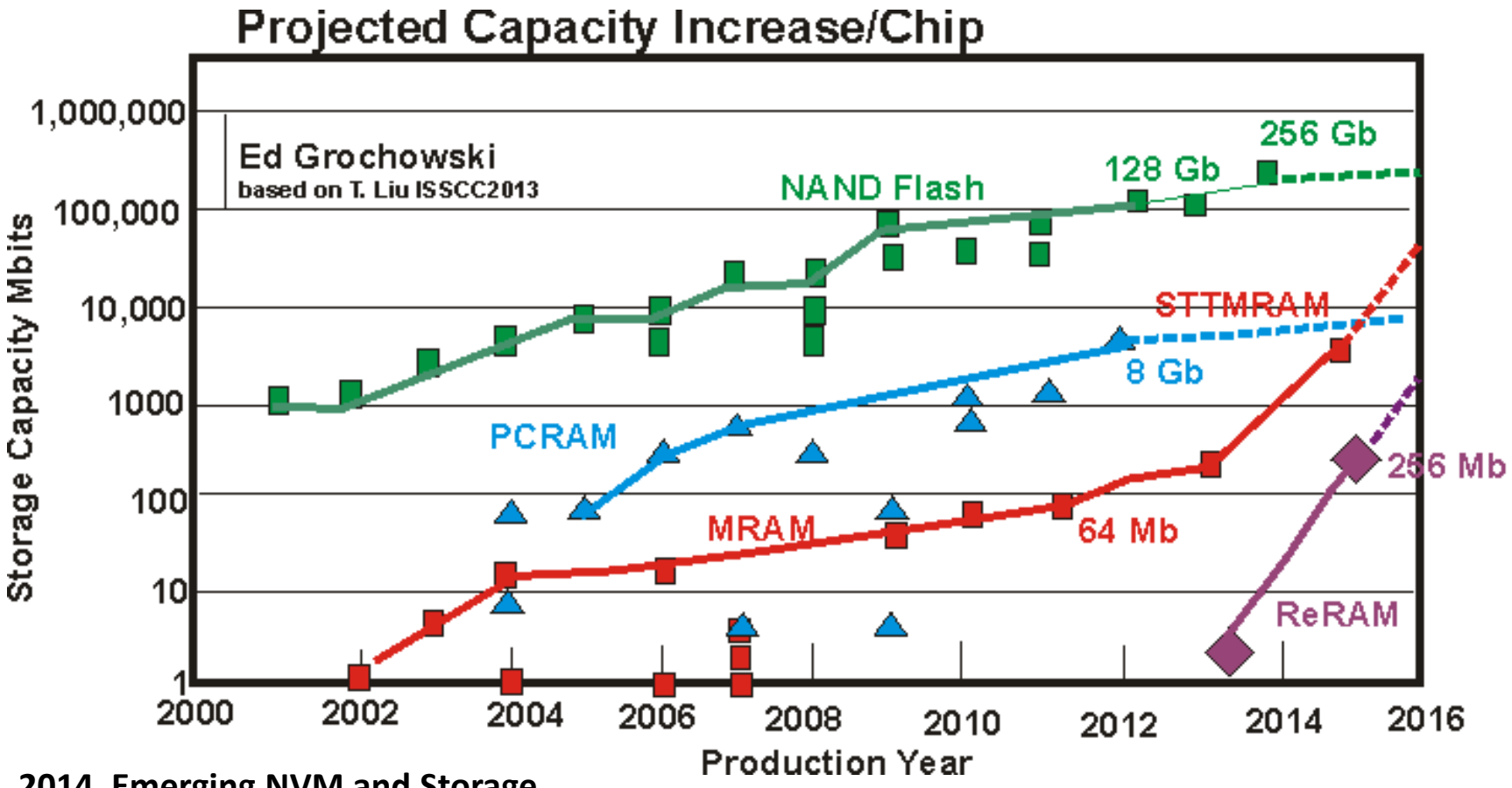
	FeRAM	RRAM	Magnetic field write MRAM	PRAM	STT MRAM
Non-volatile	Y	Y	Y	Y	Y
Memory cell factor (F^2)	16-32	4-6	16-32	5-8	5-7
Read time (ns)	20-50	10-20	3-20	5-20	3-15
Write/erase time (ns)	50	20	10-20	>30	3-15
Number of rewrites	10^{12}	10^{5}	10^{15} min	10^{12}	10^{15} min
Power consumption at write	Low	Low	Somewhat high	Low	Low
Required input voltage (V)	2-3	1.2	3	1.5-3	1.5

Performance and Density Roadmap for Memory and Storage Technologies



PerfDens2014.ppt

Chip Capacity Projections for Various Memory Technologies



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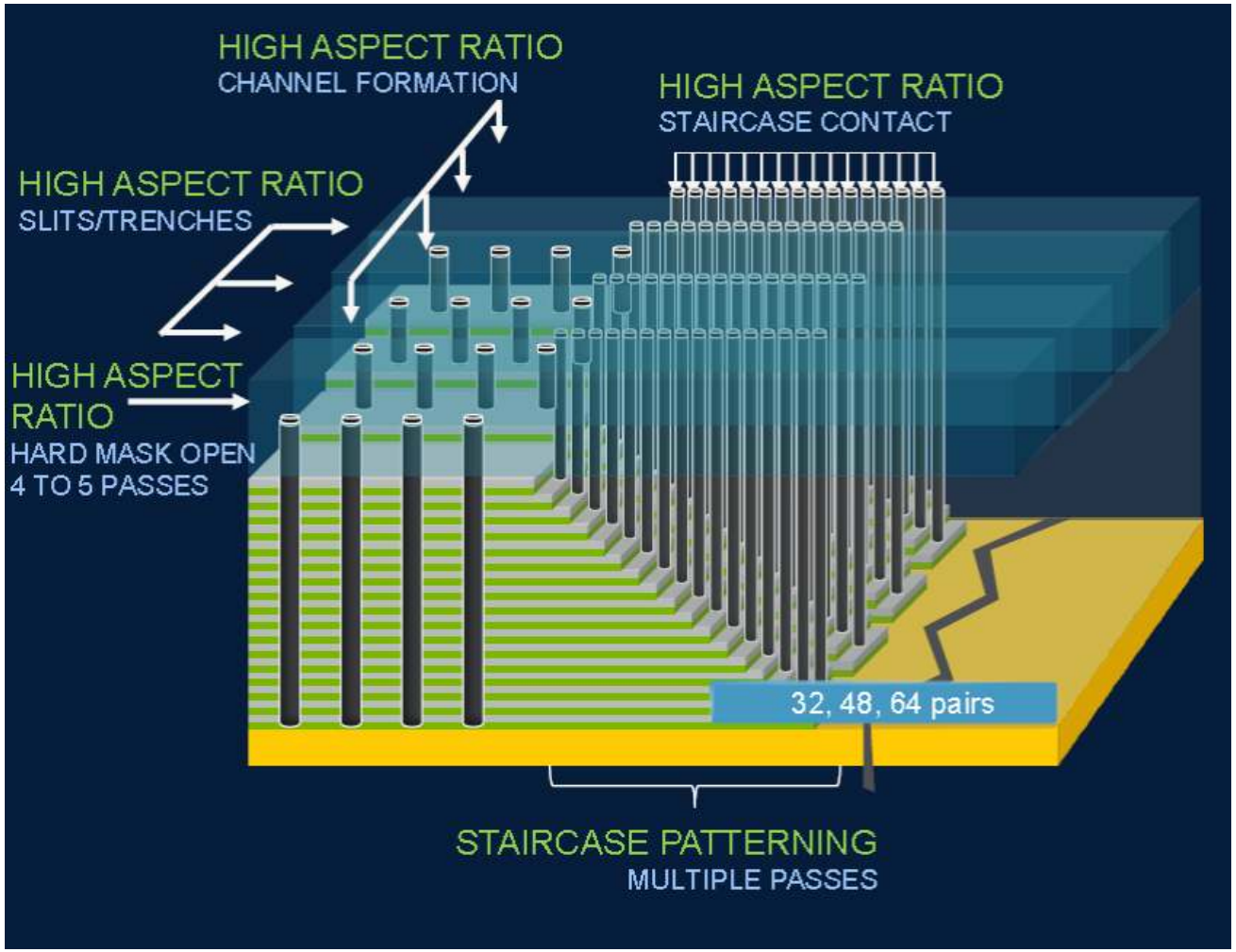
NV Cap 2014.cdr

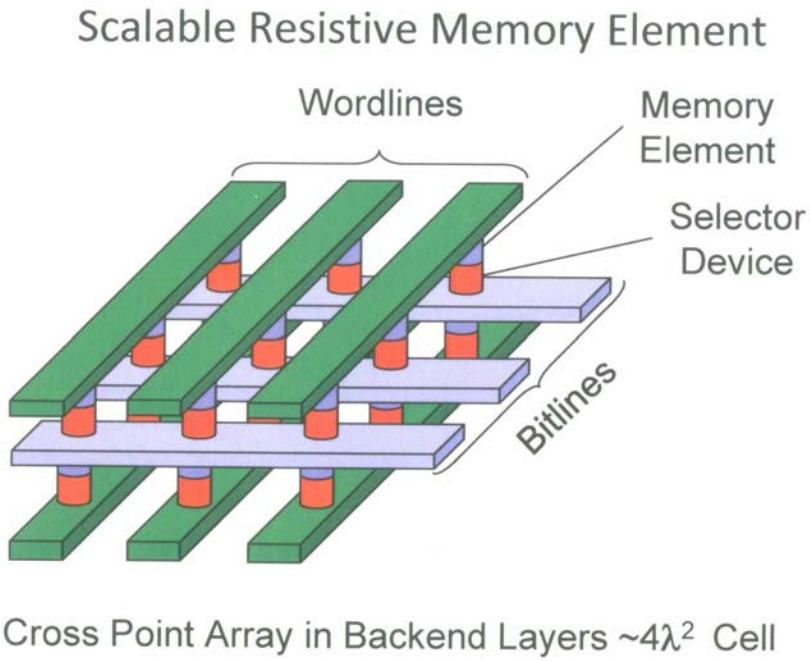
3D NAND Technology



Ref: Applied Materials/Samsung

Ed Grochowski

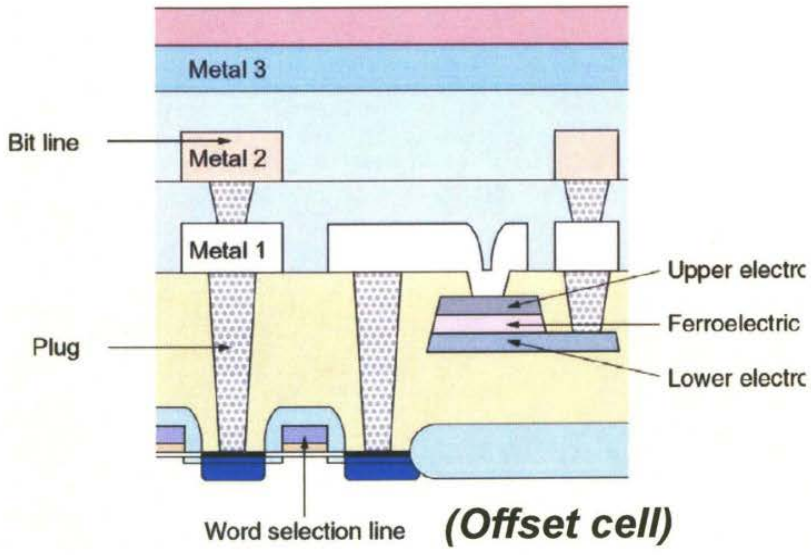
ReRAM or RRAM Cross Point Array



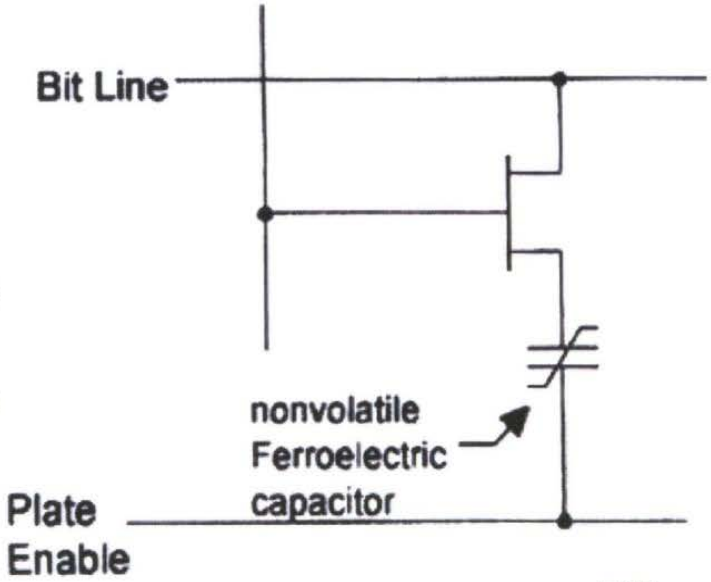
From 2013 Flash Memory Summit

- This technology prehaps shows the most promise as a NAND Flash replacement
- The most promising RRAM structures involve multi-film diodes using compatible materials as an integral part of the unit cell to eliminate the requirement for a larger CMOS device

Ferroelectric RAM (FeRAM)



Source:Fujitsu

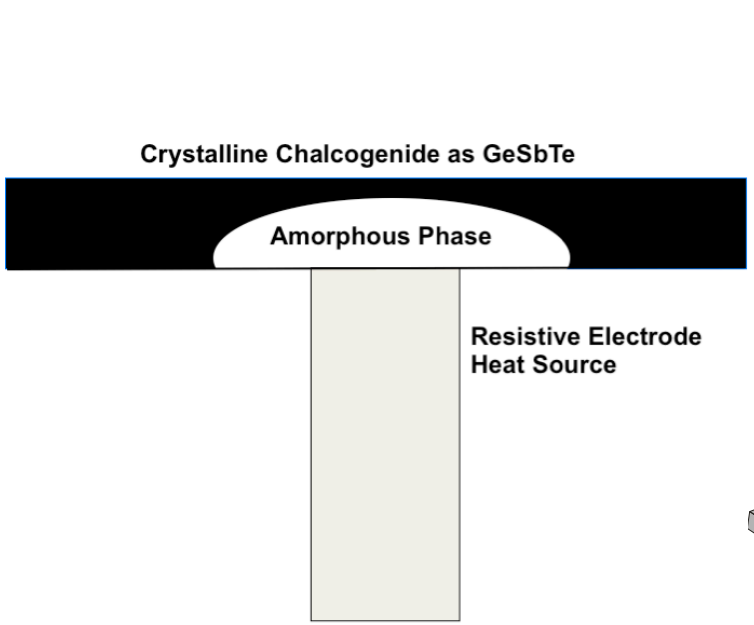


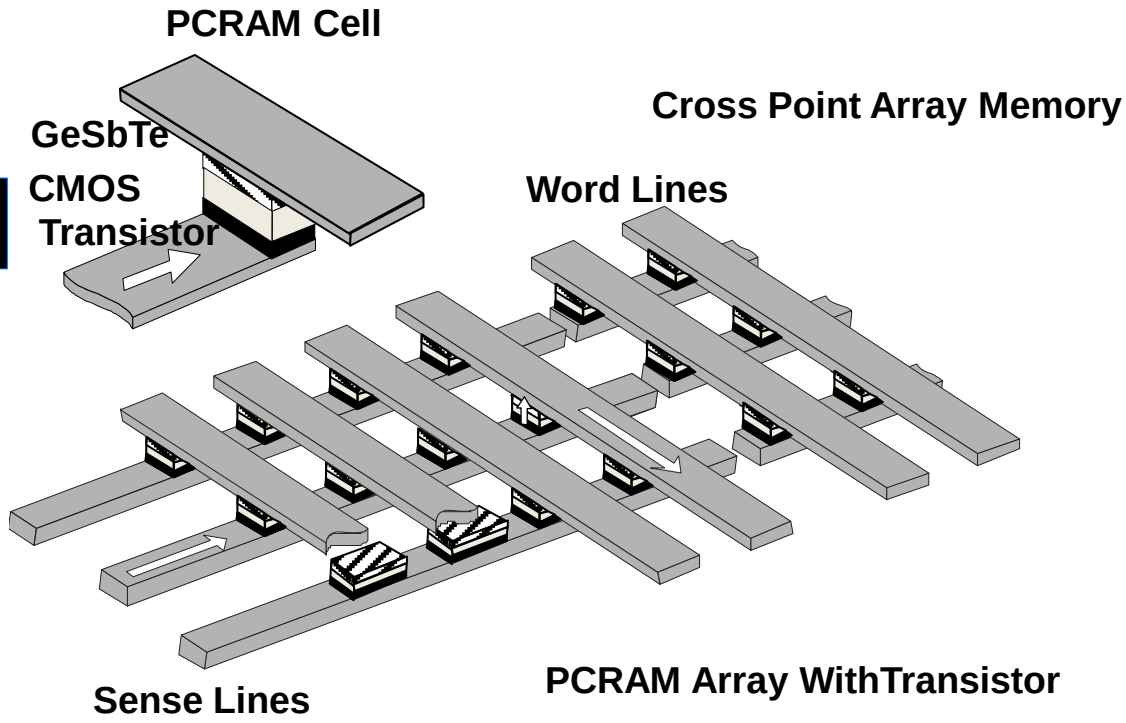
[1]

- This family of devices consists of a CMOS transistor and a variable capacitor, and therefore is a 1T/1C type NV storage cell
- FeRAM devices exhibit remarkable insensitivity to radiation, compared with FLASH and DRAM so that these NV storage devices are in demand for military applications l

Phase Change Memory (PCRAM)

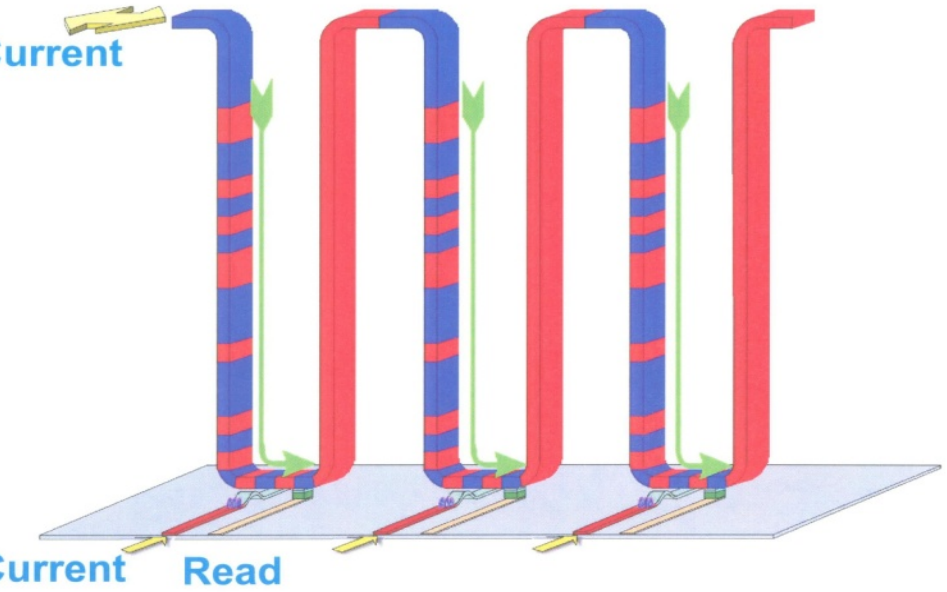
- PCRAM cells are bit addressable, are true NVRAM's, and yield high-density arrays.
- The phase change is accompanied by a resistance change, i.e. the crystalline phase has low resistance and the amorphous phase has higher resistance.





Magnetic Race Track

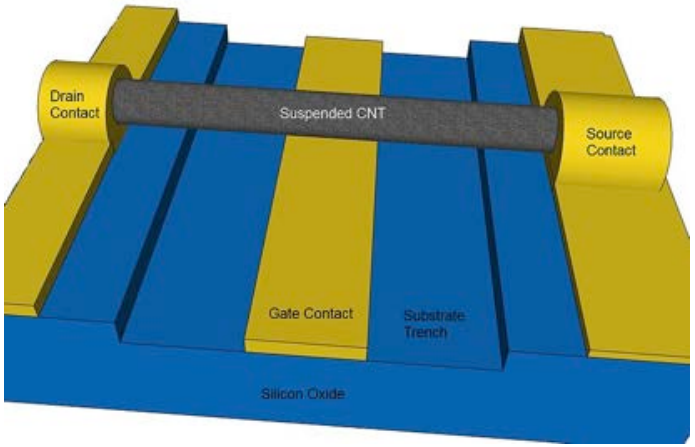
Magnetic Race Track Memory Configured as Shift Register (Stuart Parkin, IBM)

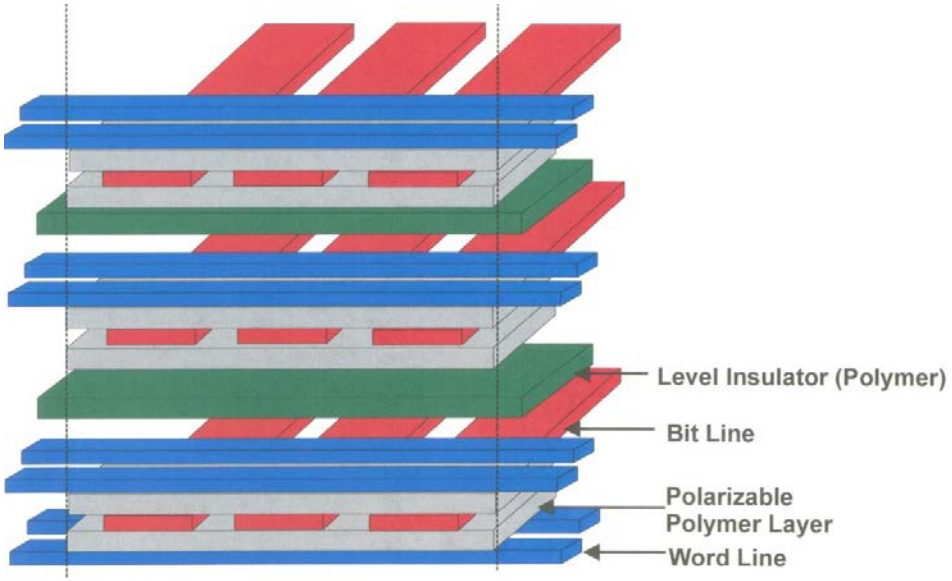


- The MRT employs the motion of domains through a vertically oriented magnetic material such as a permalloy wire (a NiFe alloy)
- By connecting a series of MRT nano-wires, a type of magnetic shift register may be configured.
- A single read and write head positioned at one location of the column determines the polarity of these domains records them accordingly.

Other Memory Technologies

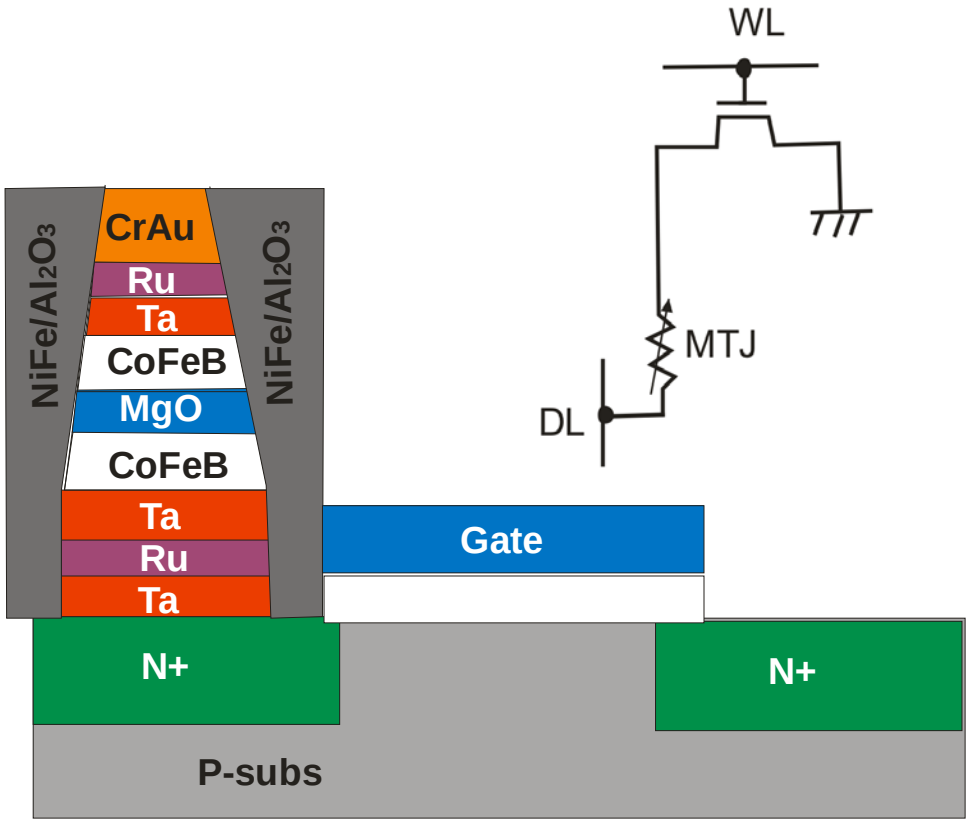
- Carbon Nanotubes
- Polymeric Ferroelectric RAM (PFRAM)
- Ferroelectric Field Effect Transistor RAM (FeFET RAM)





Magnetic RAM (MRAM)

- Three Major MRAM memory architectures
  - Toggle Mode (field driven)
  - Spin Torque Transfer (STT)
  - Magnetothermal MRAM (Heat Assisted)



STT MRAM Stack on Single CMOS Transistor

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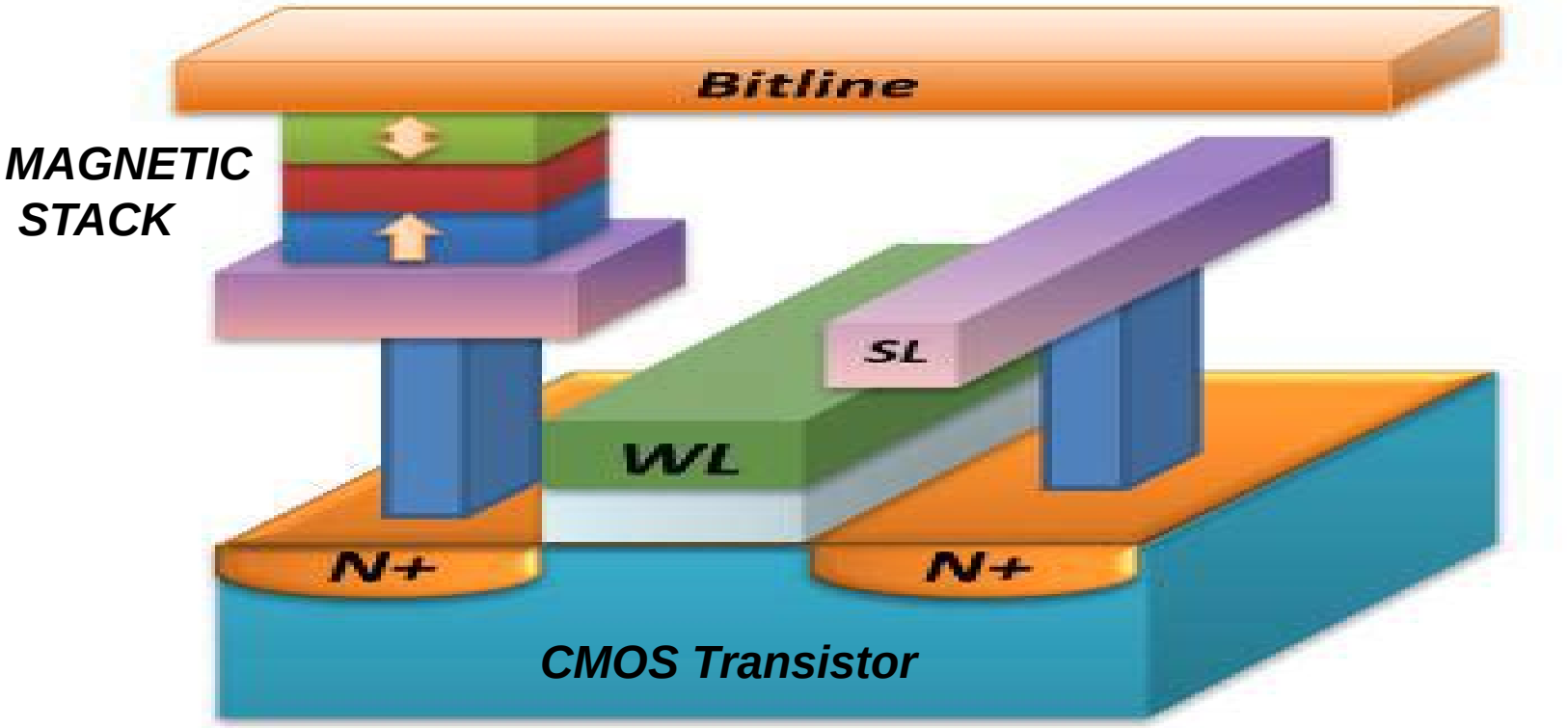
STT RAM CELL SCHEMATIC



Cell Requires Magnetic Stack Deposited and Ion Etched Directly on Underlying CMOS Transistor

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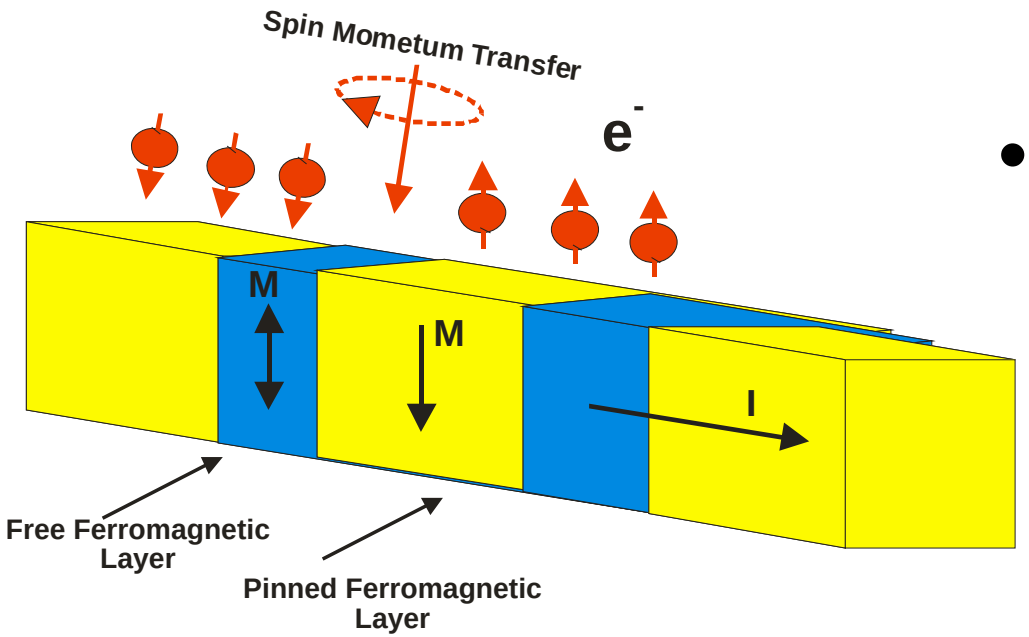
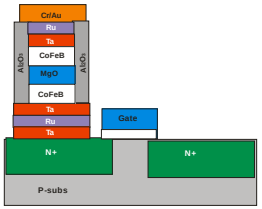
Spin Momentum Transfer



- STT MRAM uses the electron spin to create a memory element

	STT MRAM	DRAM	SRAM
Read Time (ns)	3-	30	1-100
Write Time (ns)	3-15	50	1-100
# Rewrites	$>10^{15}$	10^{16}	10^{16}
Input Voltage	1.5	2	None



STT RAM AS A DRAM REPLACEMENT

Based on Spin Transfer Technologies FMS 2014

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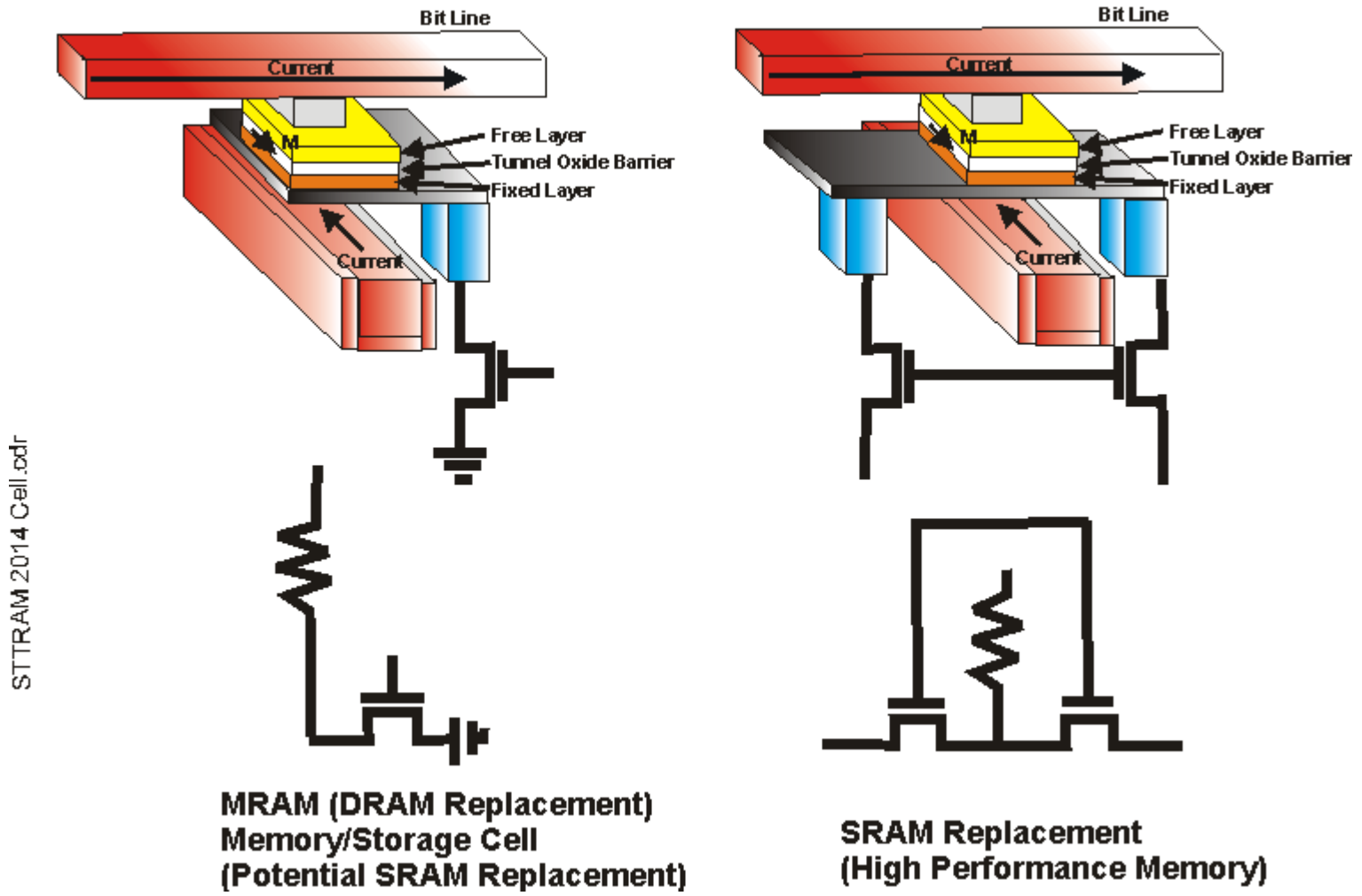
Possible STT MRAM Device Cell Architectures



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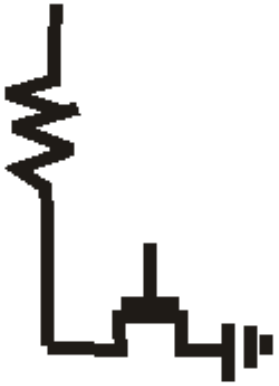
Comparison of DRAM and STT MRAM

DRAM
(Memory Cell)

STT RAM
(DRAM Replacement)
(Potential SRAM Replacement)



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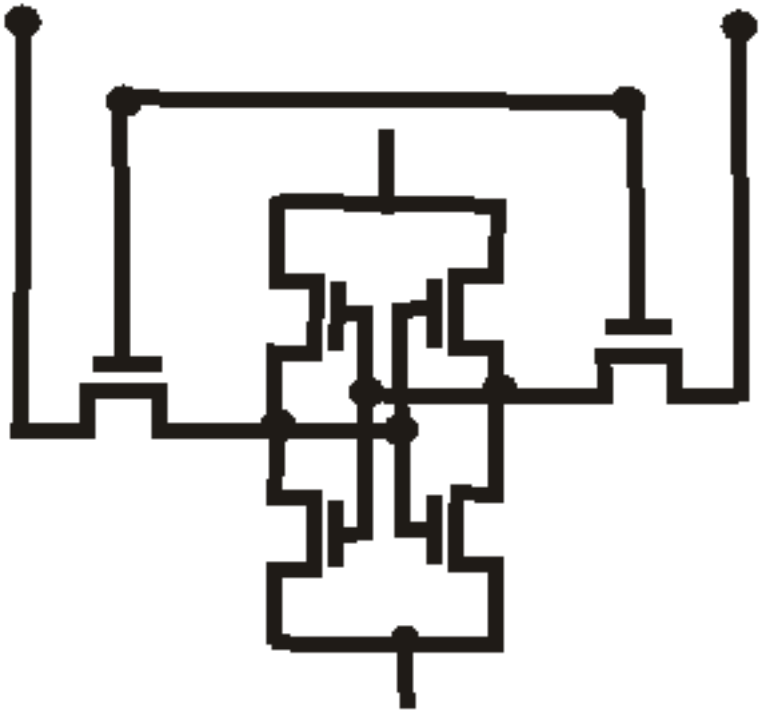
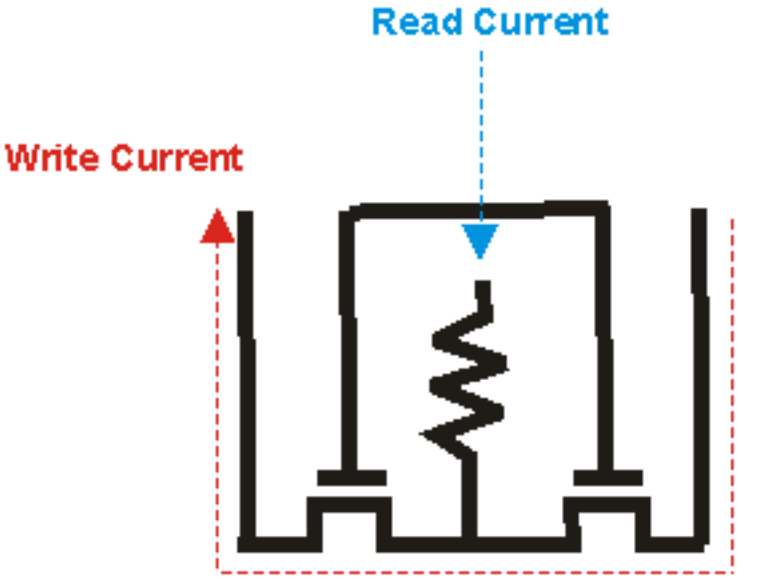
- STT MRAM Replaces DRAM capacitive element with a resistive element
- STT MRAM performance is close to DRAM and near SRAM
- STT MRAM is Non-volatile, DRAM requires refresh

Future STT MRAM Replacement for SRAM



6T SRAM (Memory Cell)



STT RAM
(Performance Memory)

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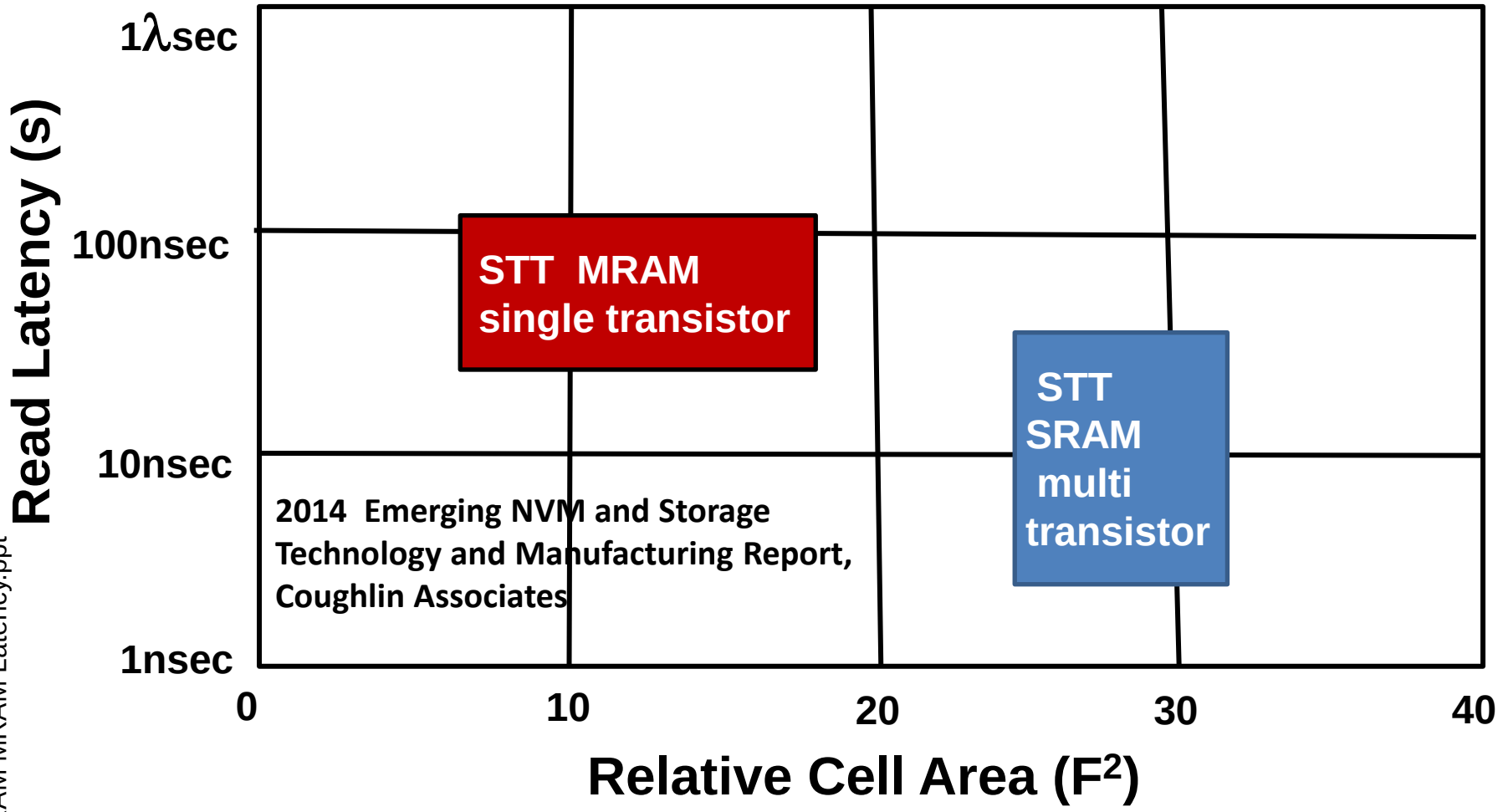
Estimated STT MRAM DRAM and SRAM Replacement



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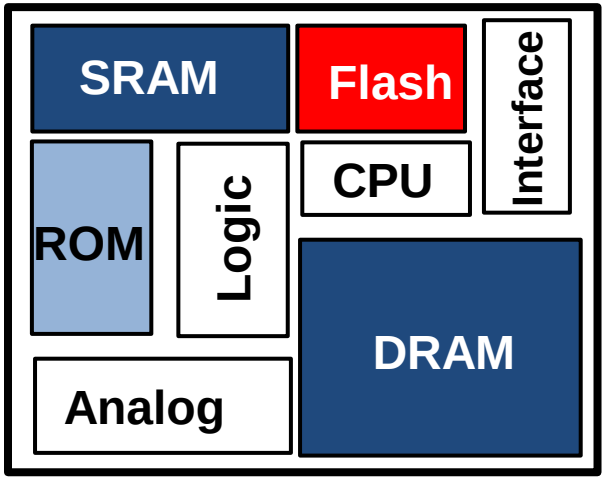
STTRAM MRAM Latency.ppt

Everspin 64 Mbit STT MRAM Chip Used for Caching

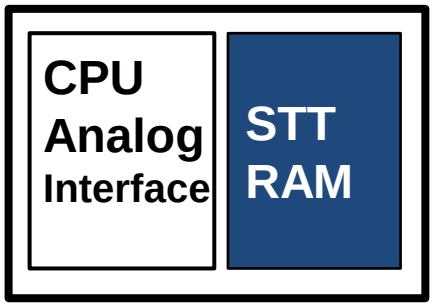
STT RAM Embedded Memory

SOC With Multiple Memories



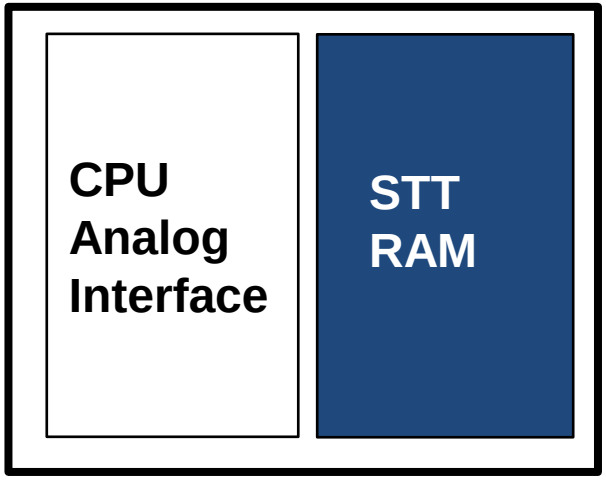
1.0 X

45% Chip Size Saving



0.55X

1.5-2.0 X Functionality



1.0 X

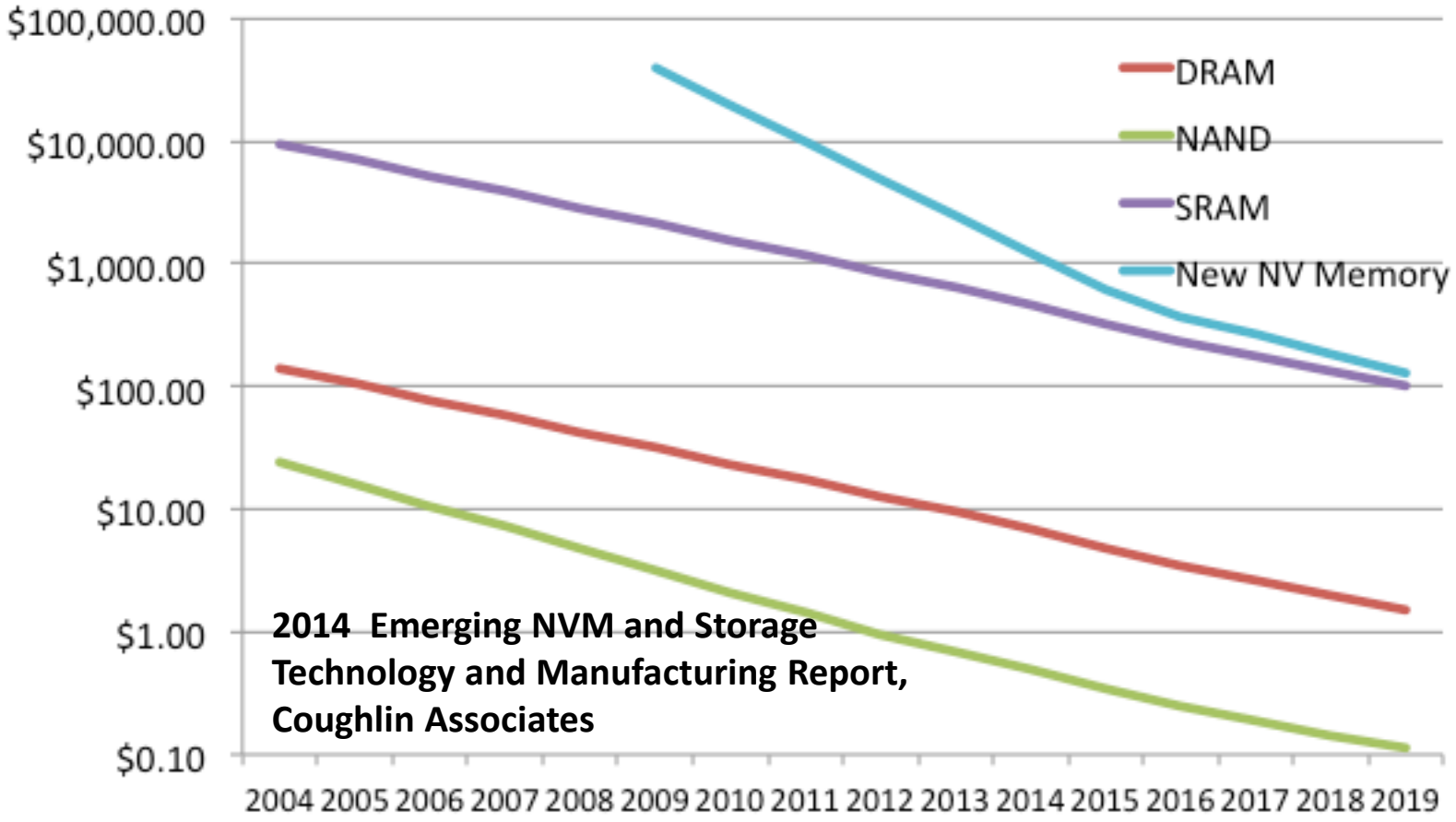
Based On Rajiv Ranjan (Avalanche Technology)

Ed Grochowski

MRAM Demand and Capital Investment

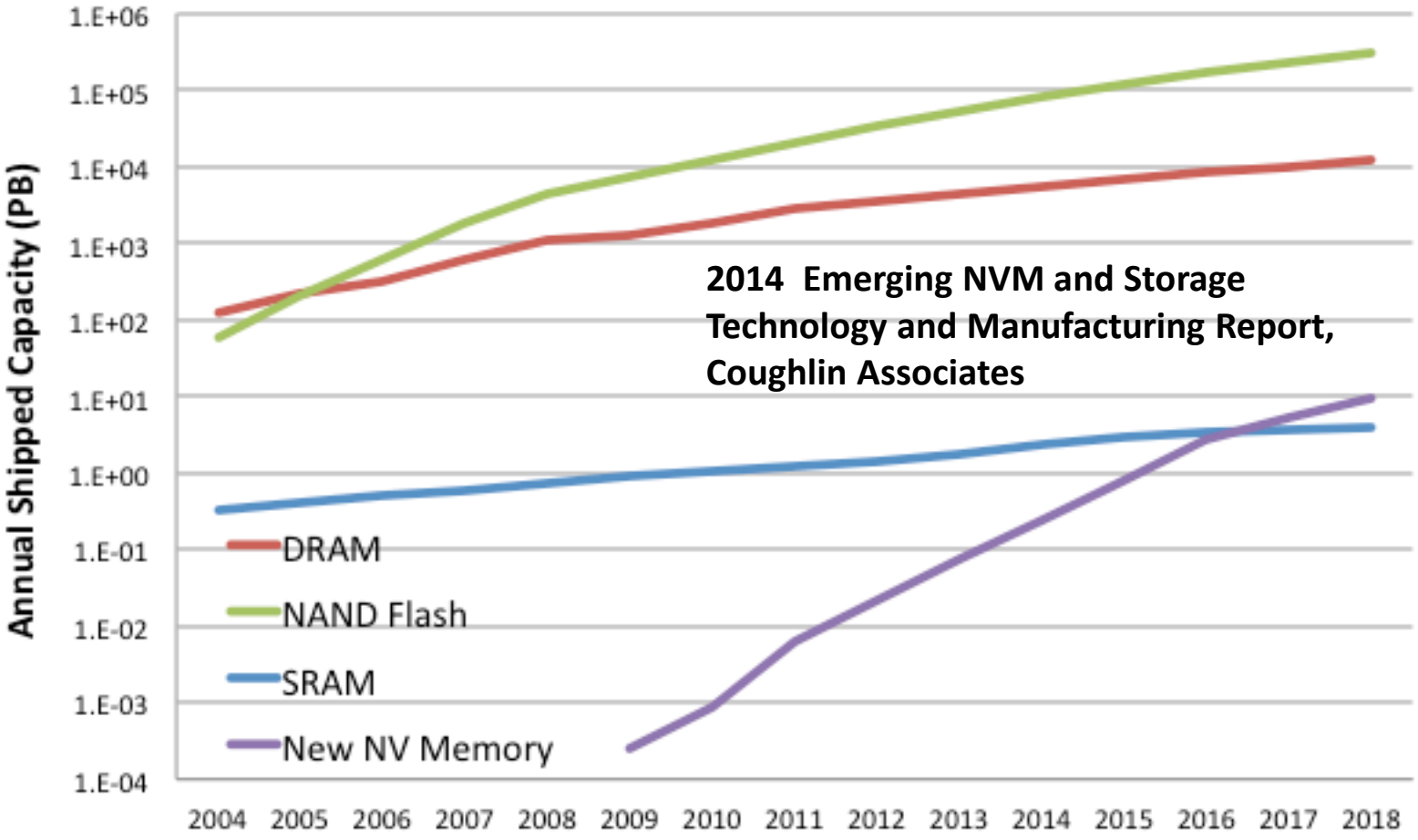
$/GB for Memory Technologies

(includes data from Jim Handy, Objective Analysis)

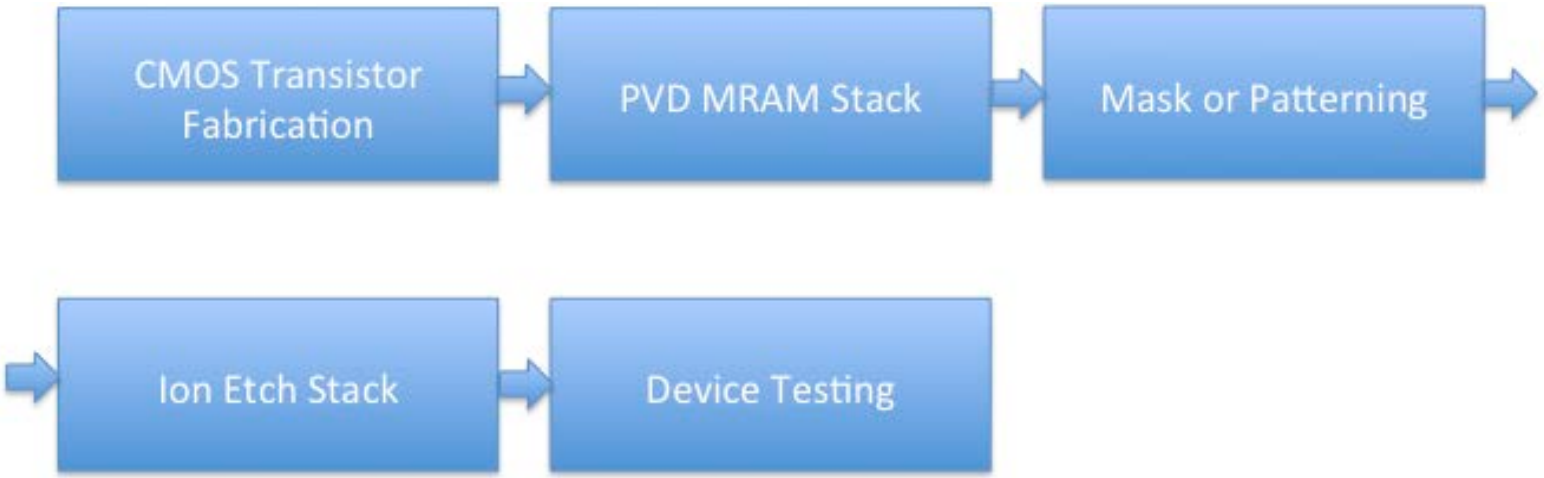


Annual Memory Capacity Shipments

(includes data from Jim Handy, Objective Analysis)



MRAM Manufacturing Process Flow



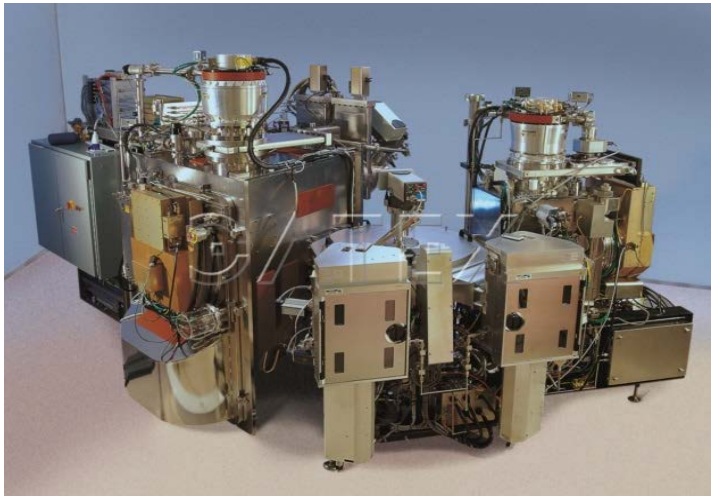
- First comes CMOS transistor production after which the MRAM layers must be deposited using a physical vapor deposition technology.
- After depositing this stack the basic pattern, MRAM Manufacturing Process Flow must be defined on the surface of the MRAM stack.
- This pattern is then used to control etching of the MRAM device.
- Following the construction of MRAM devices connected to their CMOS transistors the devices go through testing and mapping out the bad memory cells.

Equipment for MRAM Production

Singulus Timaris PVD Cluster Tool Platform

Canon I-Line Stepper

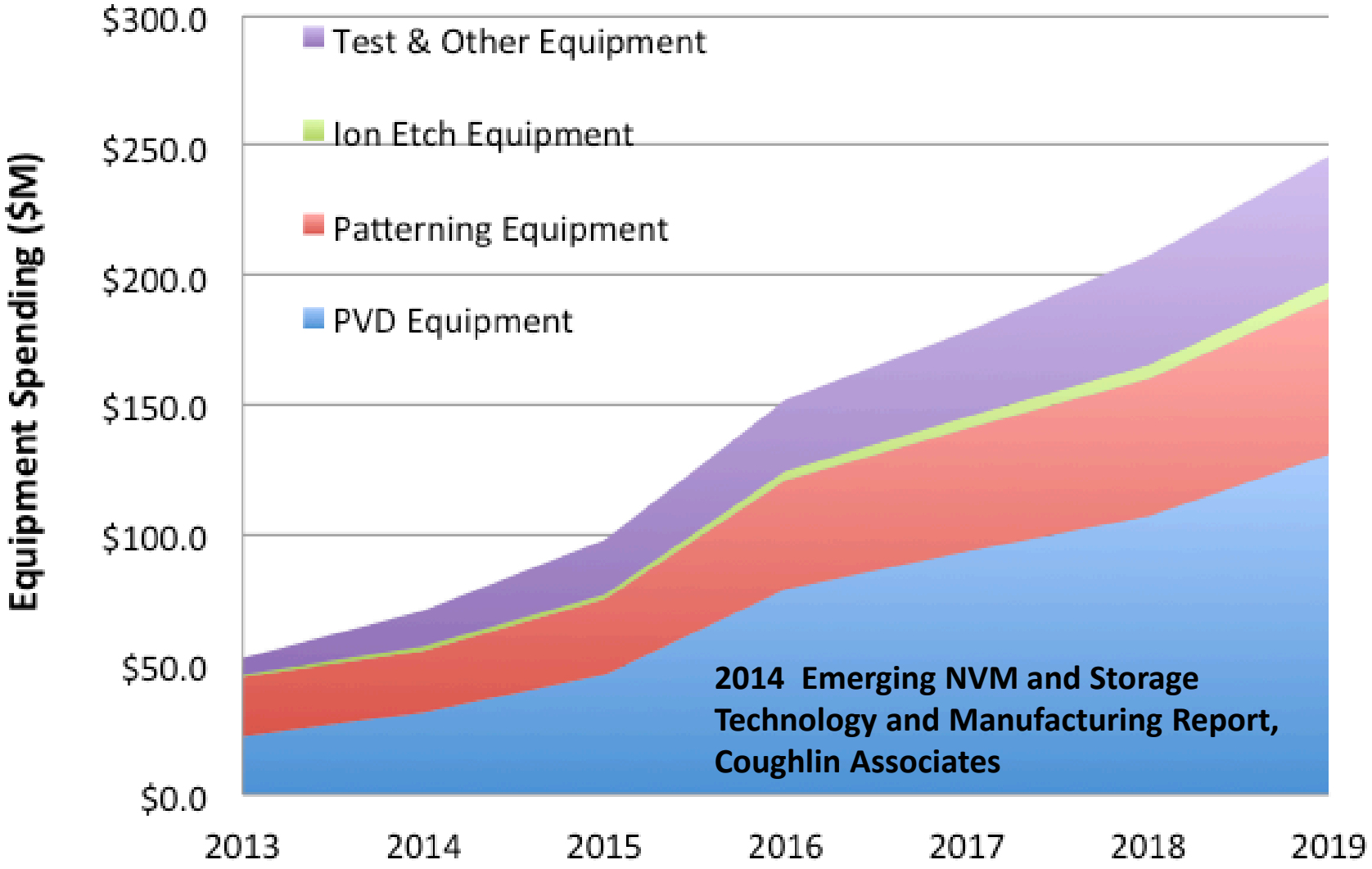
ISI WLA 3000 Quasi-Static Tester



Veeco Nexus Ion Beam System

Tokyo Electron Magnetic Annealing Tool

Revenue Estimates for MRAM Equipment



Conclusions

- Many Candidates for NV memory/storage – RRAM, STT MRAM, PRAM, FRAM, each with specific trade-offs
- Advantages: Power Savings, Scalability, Density
- Architectural System Evolution—new applications, use spin versus current
- RRAM replacement for flash after 2020
- STT-MRAM, RRAM Replacement for SRAM and DRAM
- STT-MRAM Very Compatible With current CMOS Processing
- MRAM Production drives capital investment