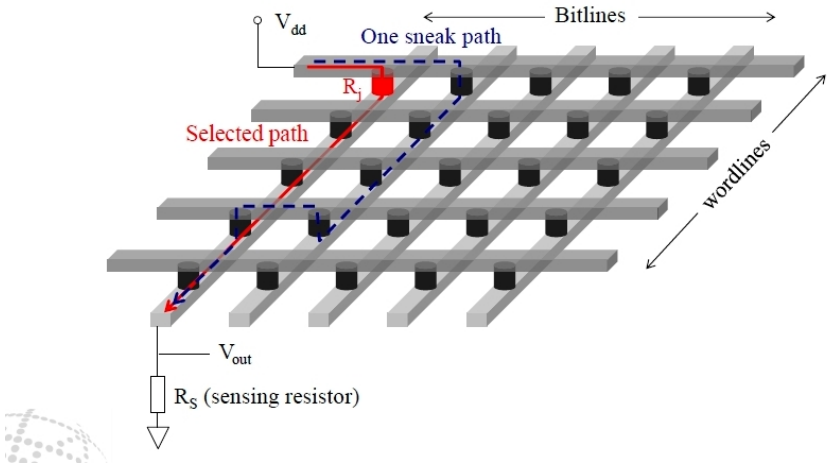
SNIA DSI '16 DATA STORAGE INNOVATION CONFERENCE
Innovation in Storage Products, Services, and Solutions
June 13-15, 2016 | Marriott San Mateo | San Mateo, CA

Emerging Non Volatile Memory And Spin Logic



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Outline

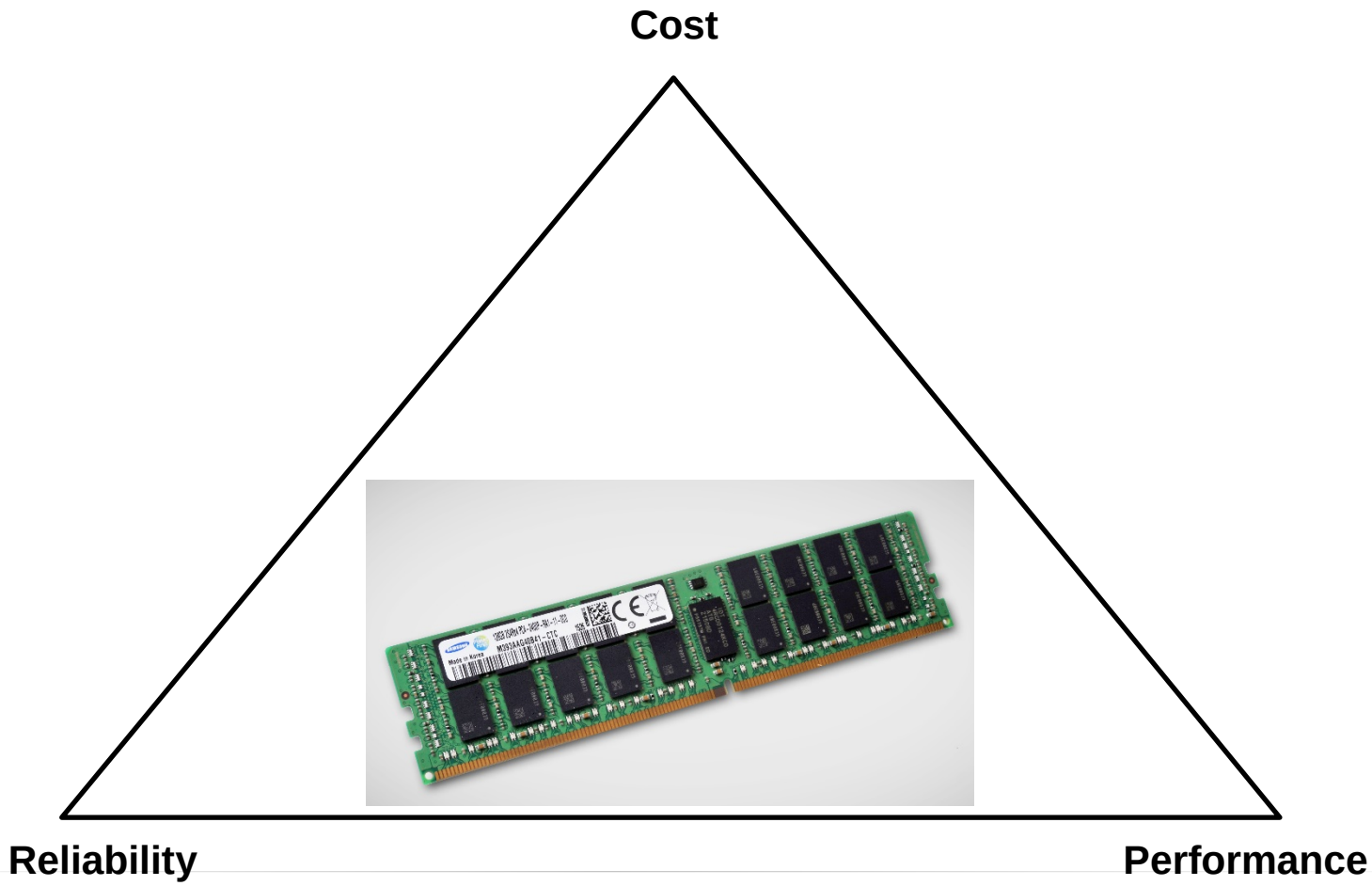
- Power is an issue
- New memories are coming
- Memory and logic can be combined
  - This will drive architectural advancements
- Summary, Q&A

Technical “Ages”

1. The Industrial Age (1800’s)
2. The Age of Electricity
3. The Age of Flight
4. The Age of Communications
5. The Atomic Age
6. The Space Age
7. The ~~Information~~ Age of Data Storage (2000’s)
8. “The Age of Energy Conservation 2020?”

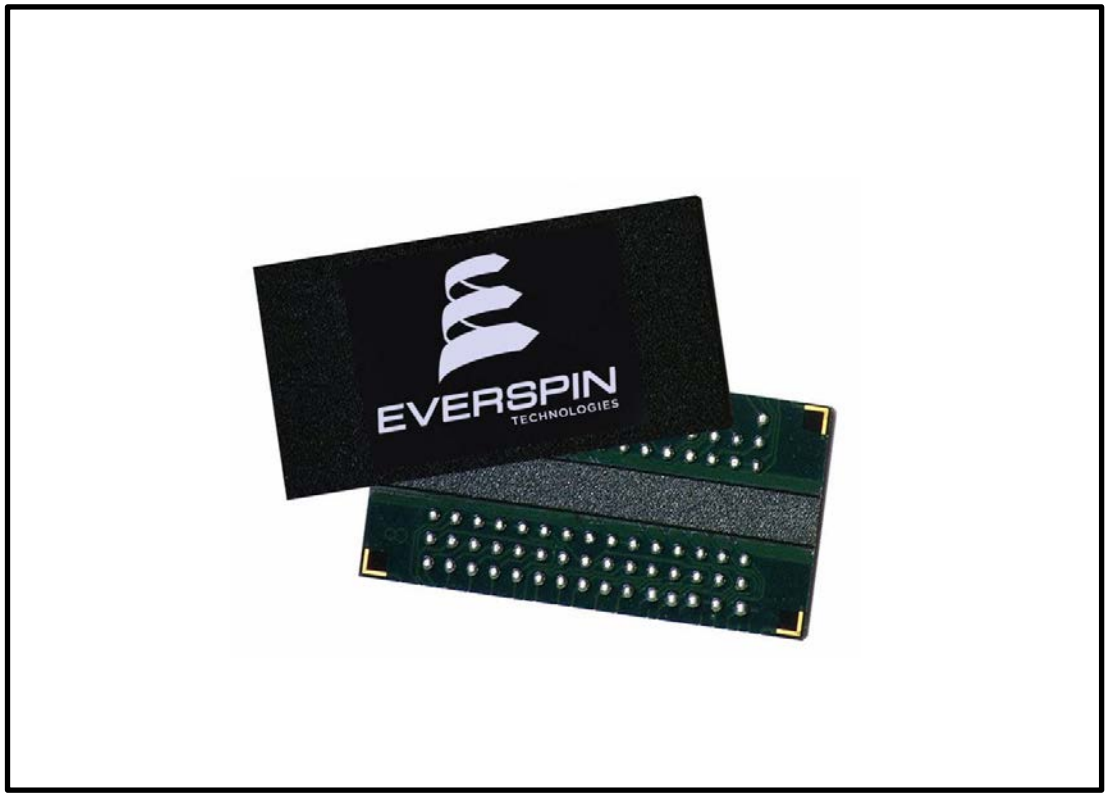
Power Consumption Gains Focus

Today's Memory/Storage Selection Criteria



~~Today's~~ Memory/Storage Selection Criteria Tomorrow's

Cost **Power**



Reliability **Performance**

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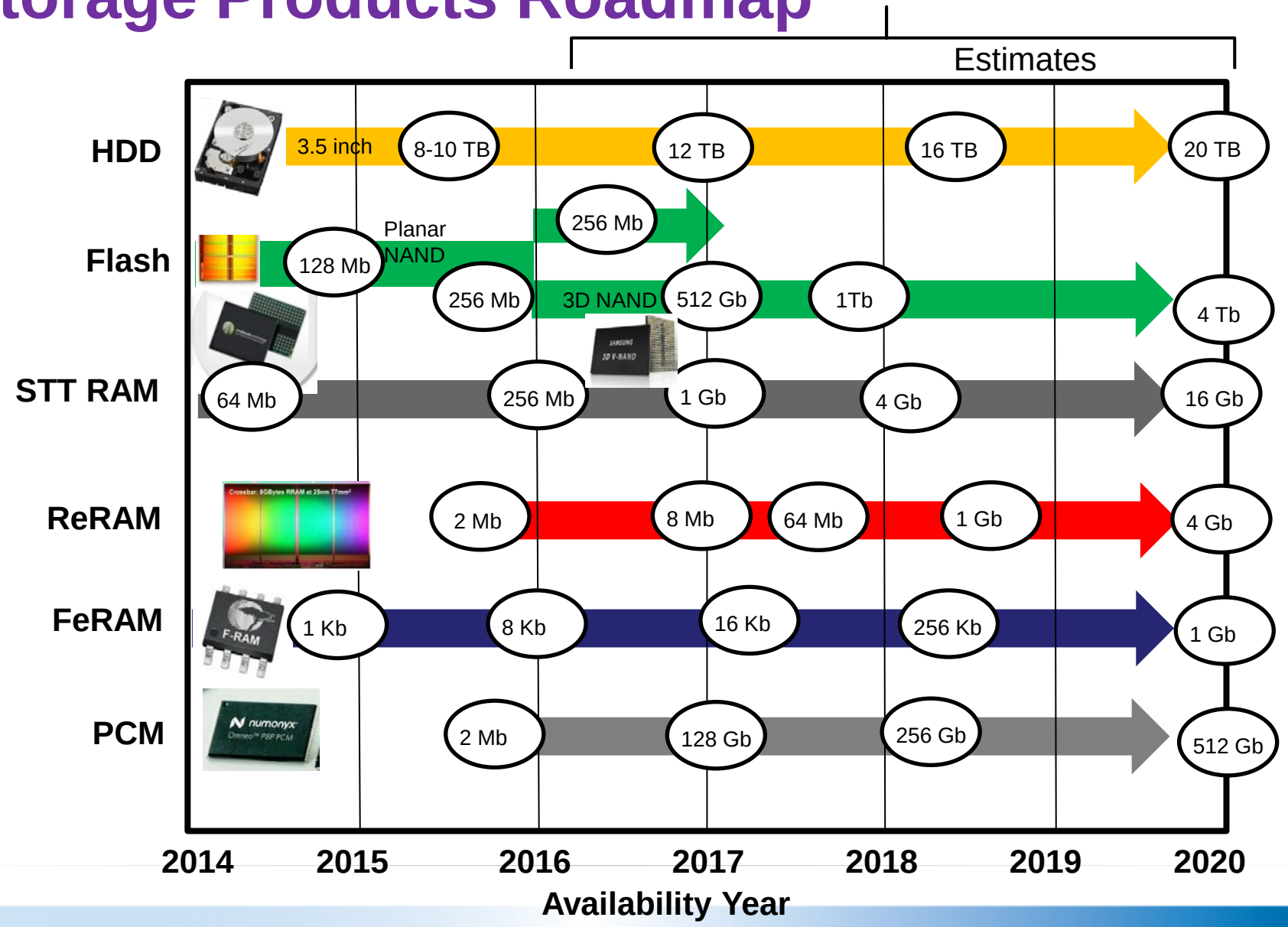
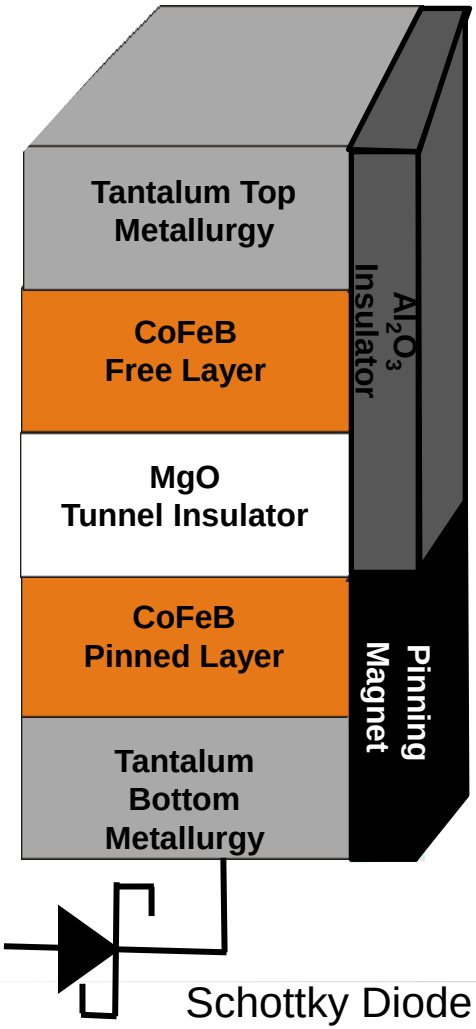
Storage Products Roadmap

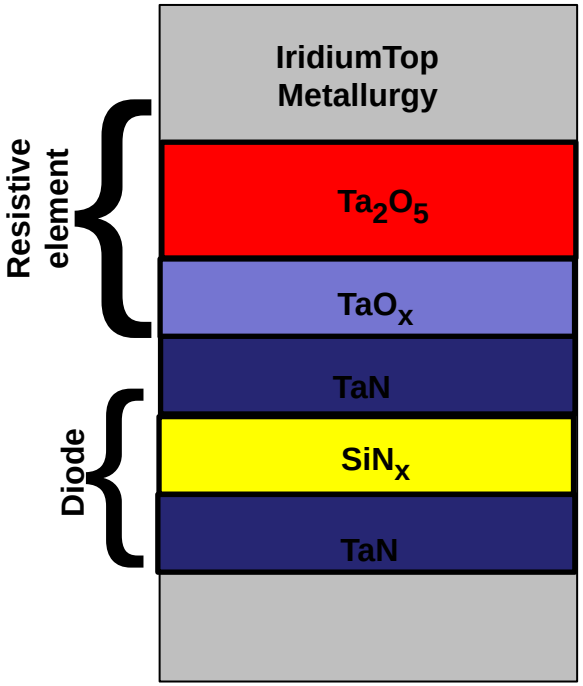


NVM Cell Designs

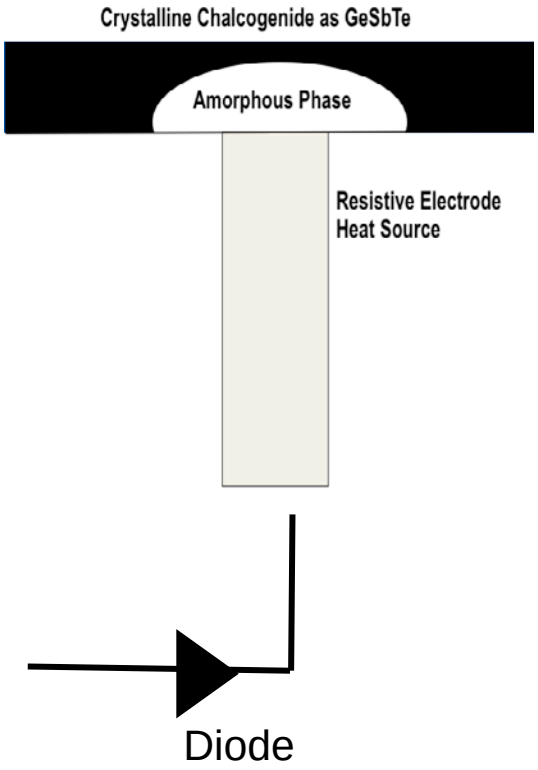
STTRAM Cell



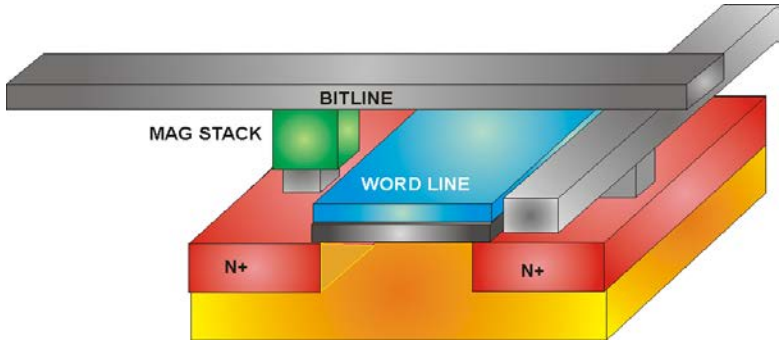
ReRAM Cell



PCRAM Cell



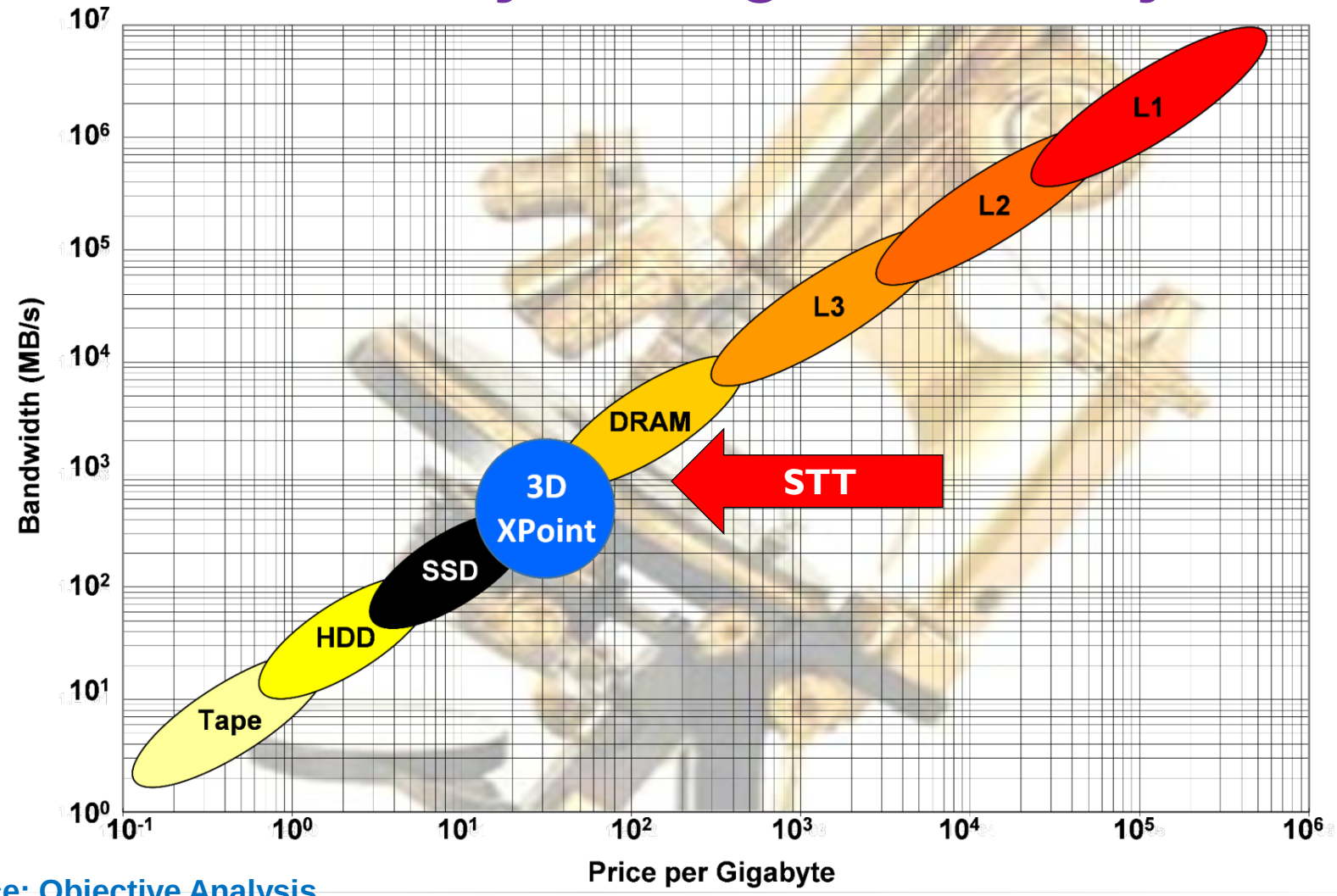
Spin Torque Tunneling Mechanism



Dr. Edward Grochowski
Computer Memory/Storage Consultant

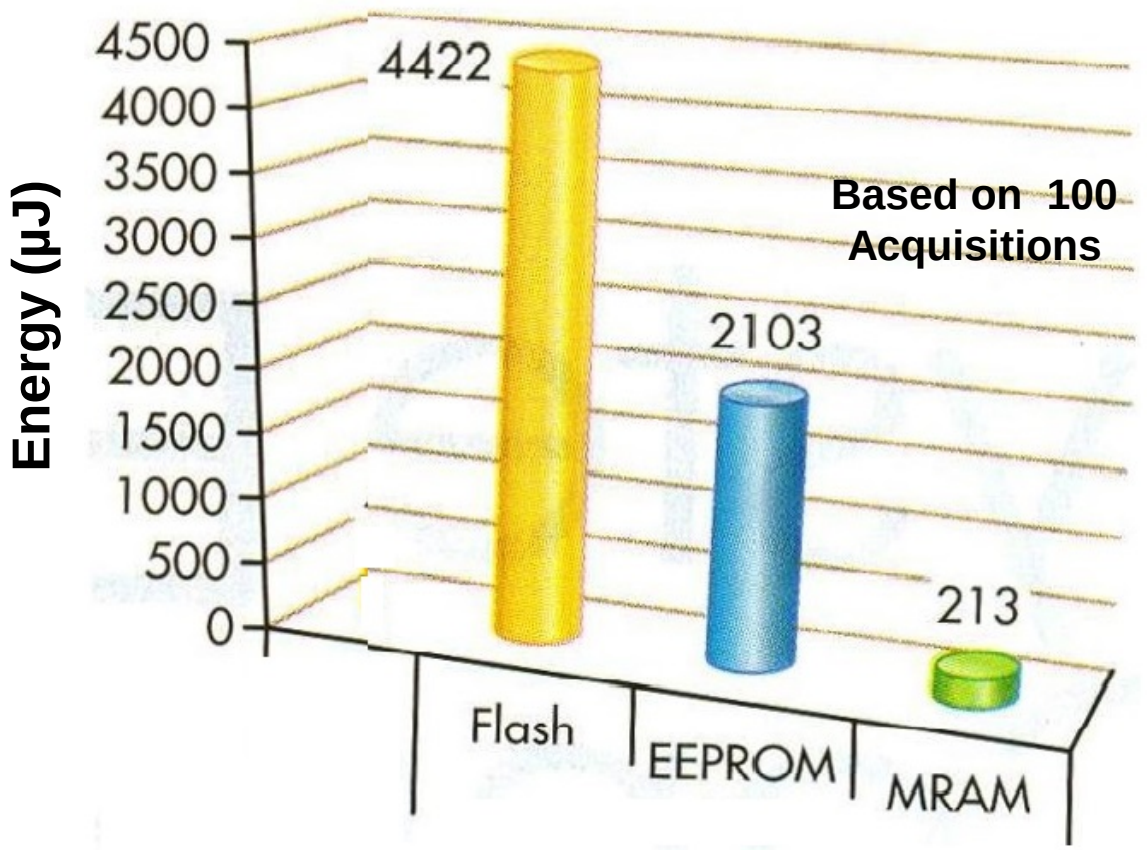
Animation by Casey Straka

STT in the Memory/Storage Hierarchy



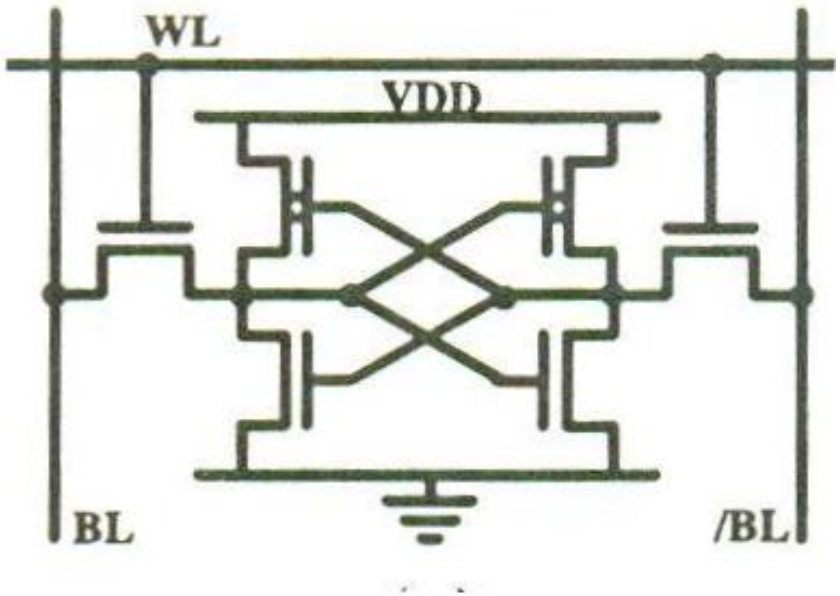
Source: Objective Analysis

MRAM Beats Flash & EEPROM Energy Consumption

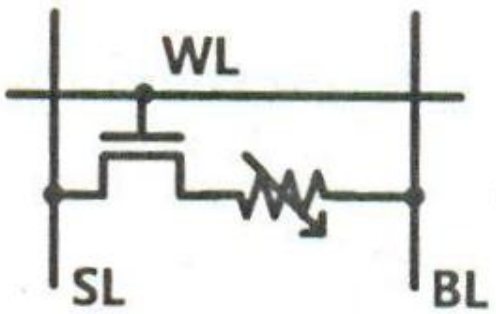


Ref: D. Bennett and A. Pockson, ED April 2016

6T SRAM vs. 1T STT



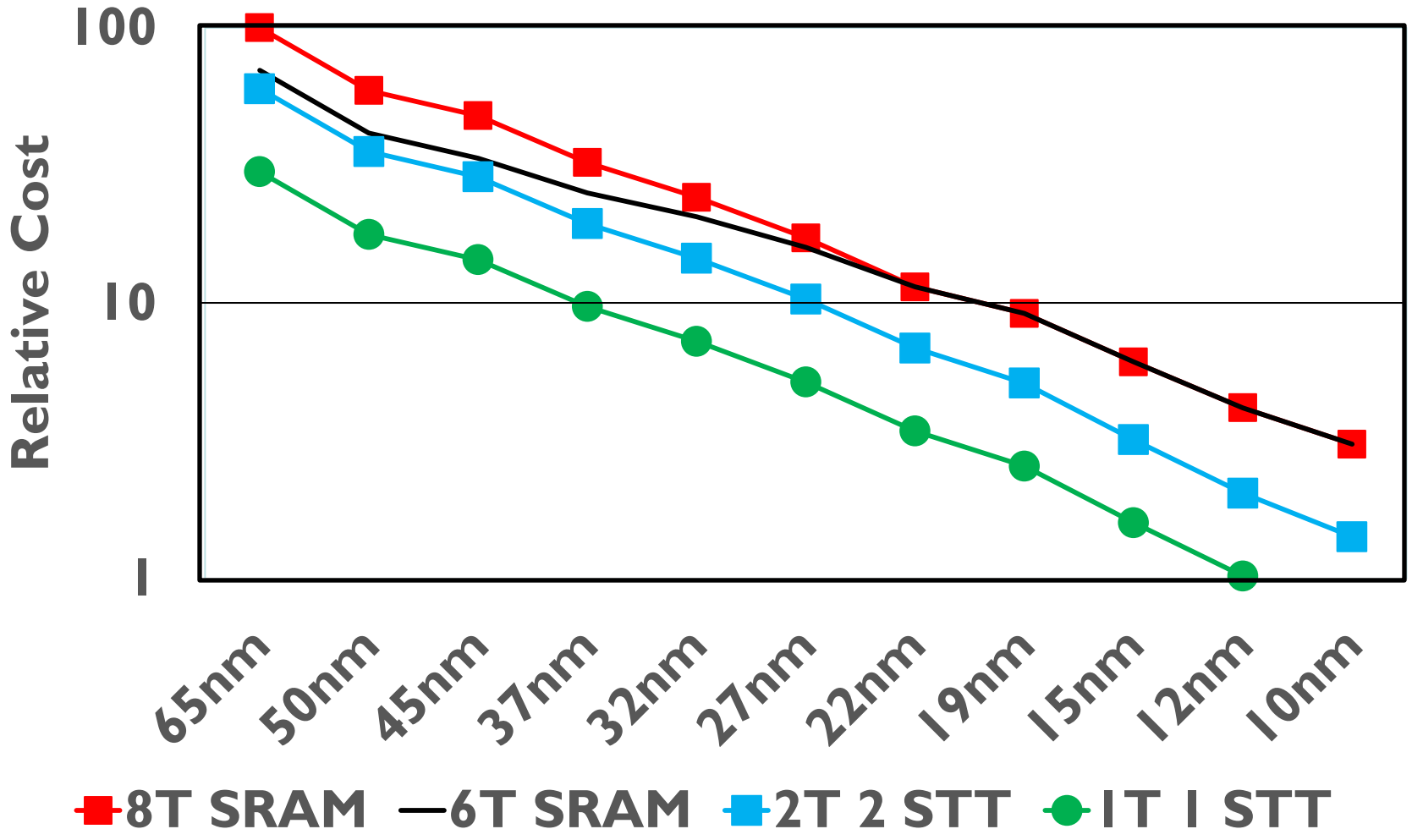
6 CMOS Transistor SRAM Circuit



1 CMOS Transistor + 1 STTRAM Circuit

Ref" J. Ryu etal. IEEE Trans. Magn. 52, 4, April 2016

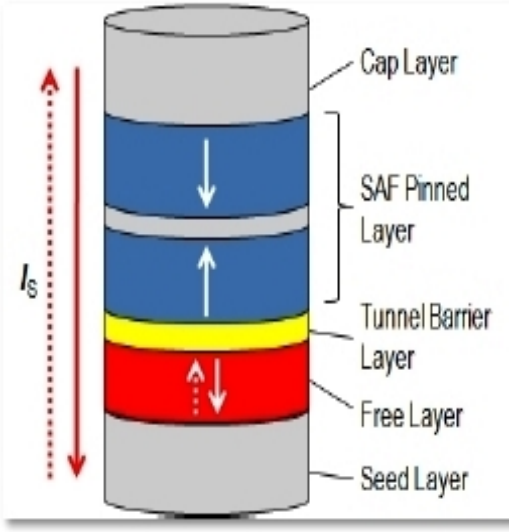
Result: MRAM Beats SRAM Cost



Based on Jang-Woo Ryu etal. IEEE Trans. Magn. 52, 4, April 2016

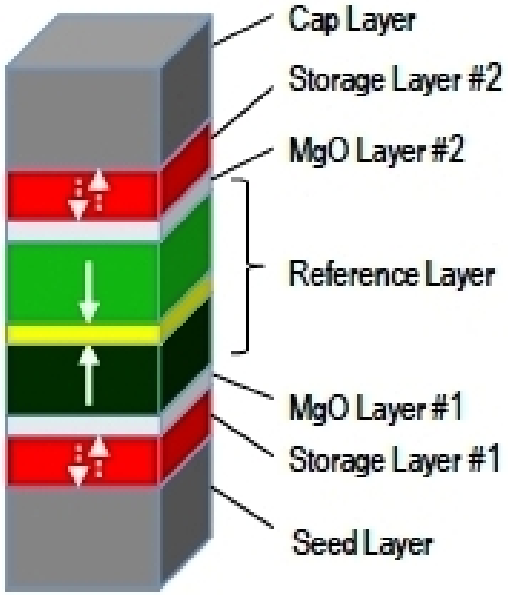
MRAM Can Be Stacked

Single-bit STT RAM Stack



Multi-bit STT RAM Stack

Multi-bit MTJ (MBJ)



Ref: A. Shukh NVMTS 8/2013

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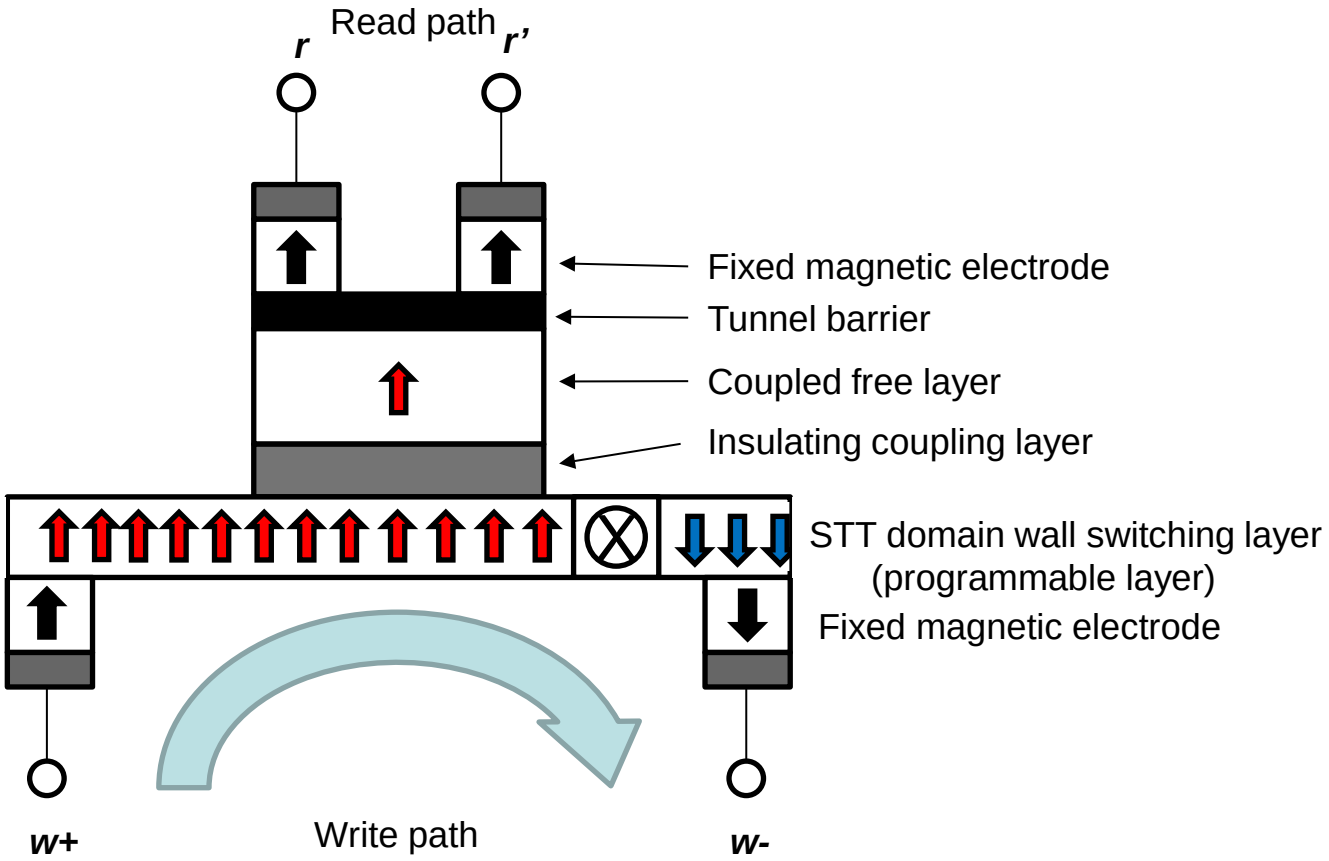
The cMem Cell: Logic + NVM



http://repository.cmu.edu/cgi/viewcontent.cgi?article=1418&context=dissertations

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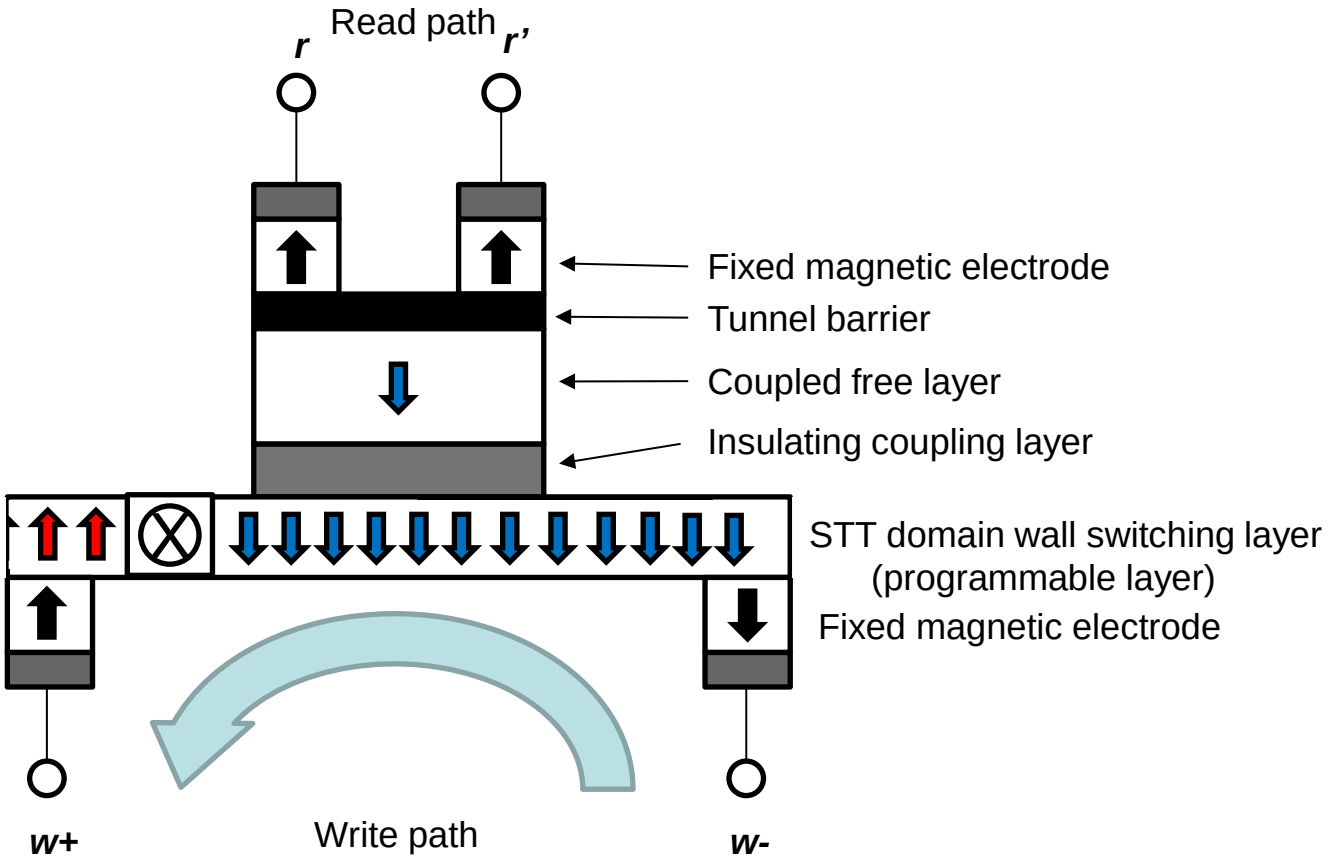

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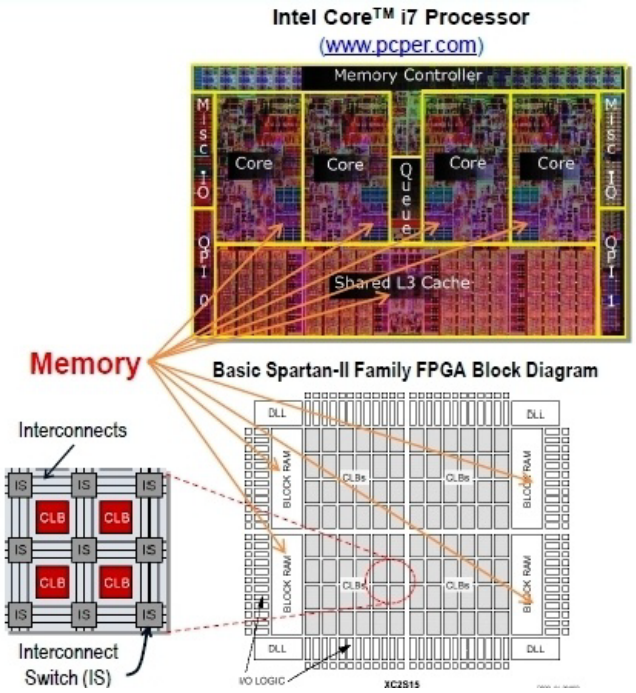
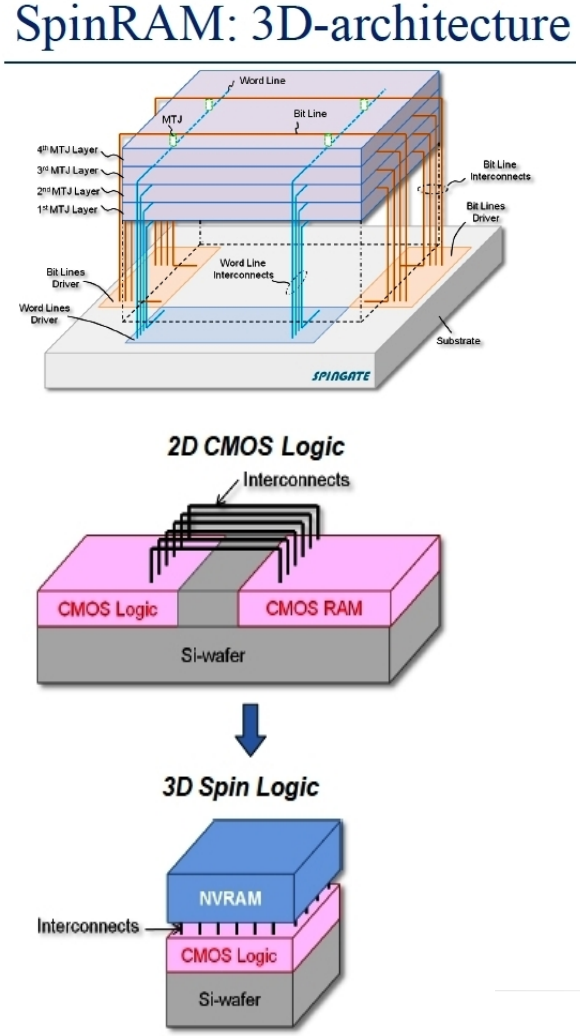
Packaging and Performance





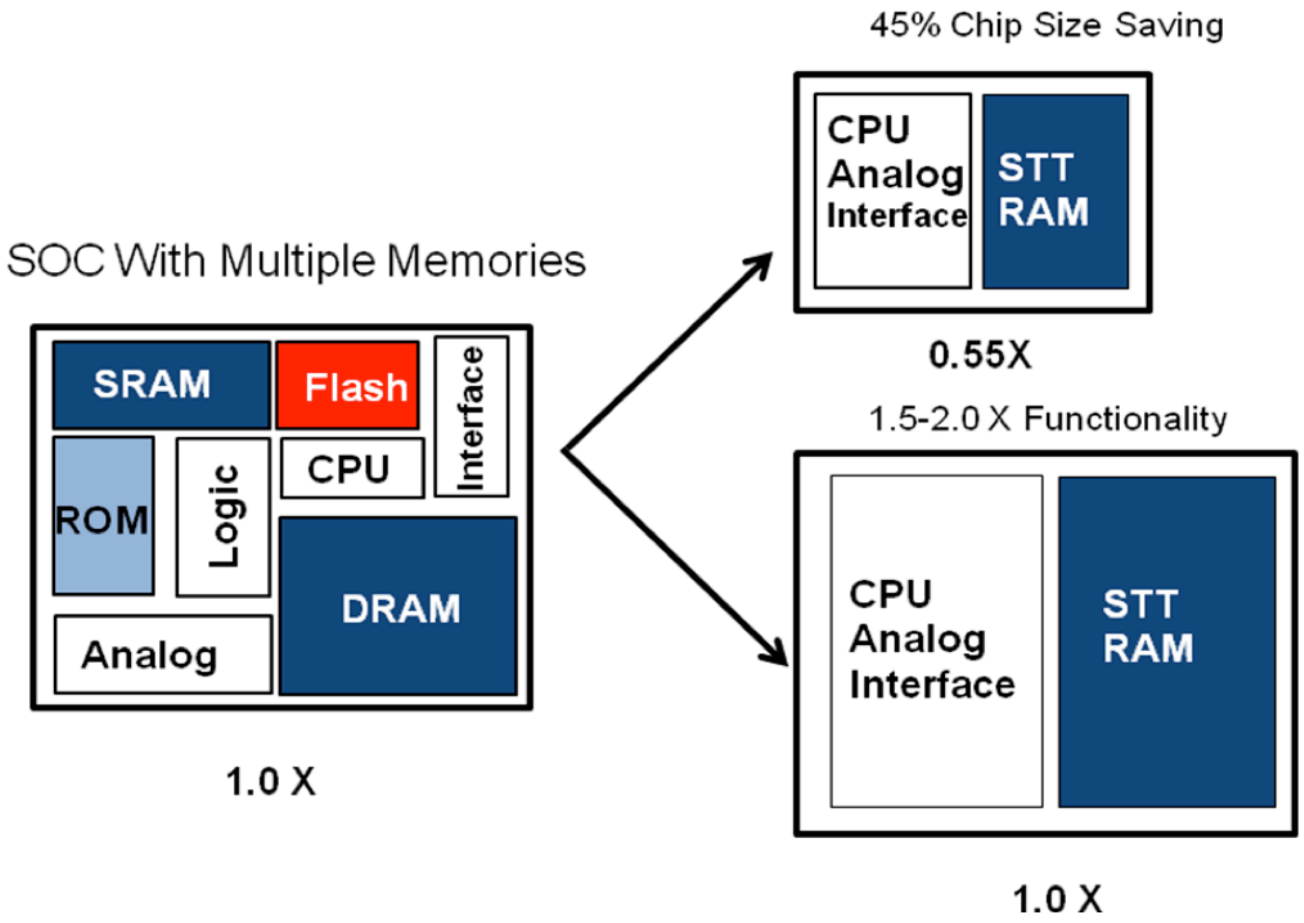
Total Interconnect length

- Chip level :10's mm
- Board level:10's inches

i.e. Circuit Delay+ Power

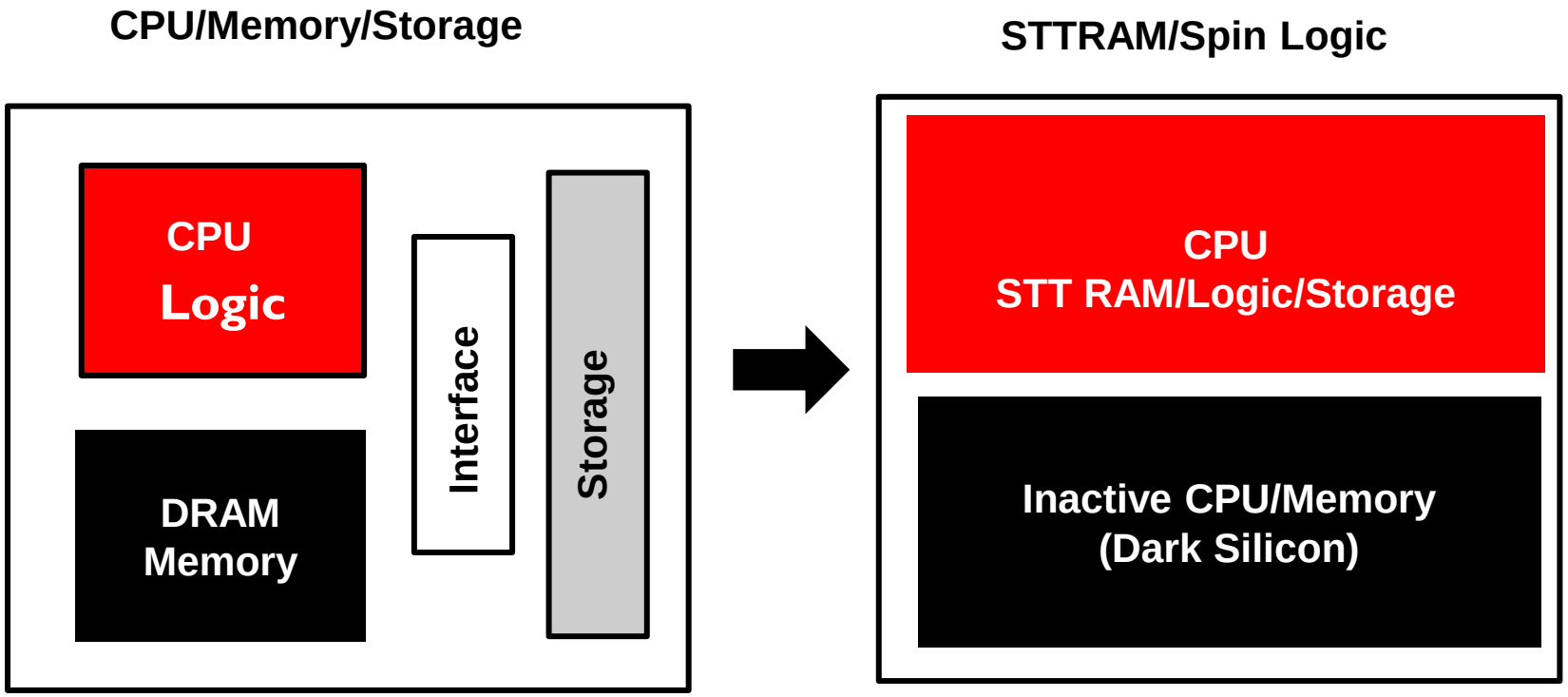
Ref: A. Shukh NVMTS 8/2013

STT Advantage: Smaller Chip or More Functionality



Based On Rajiv Ranjan (Avalanche Technology)

Changing Von Neuman's Computer Architecture Concept



Summary

- Power issues can be solved
  - NVM is a big contributor
- New memories are coming
  - STT is a promising candidate
- Memory and logic can be combined
  - This will drive architectural advancements

Questions?