

Future Memories and Today's Opportunities

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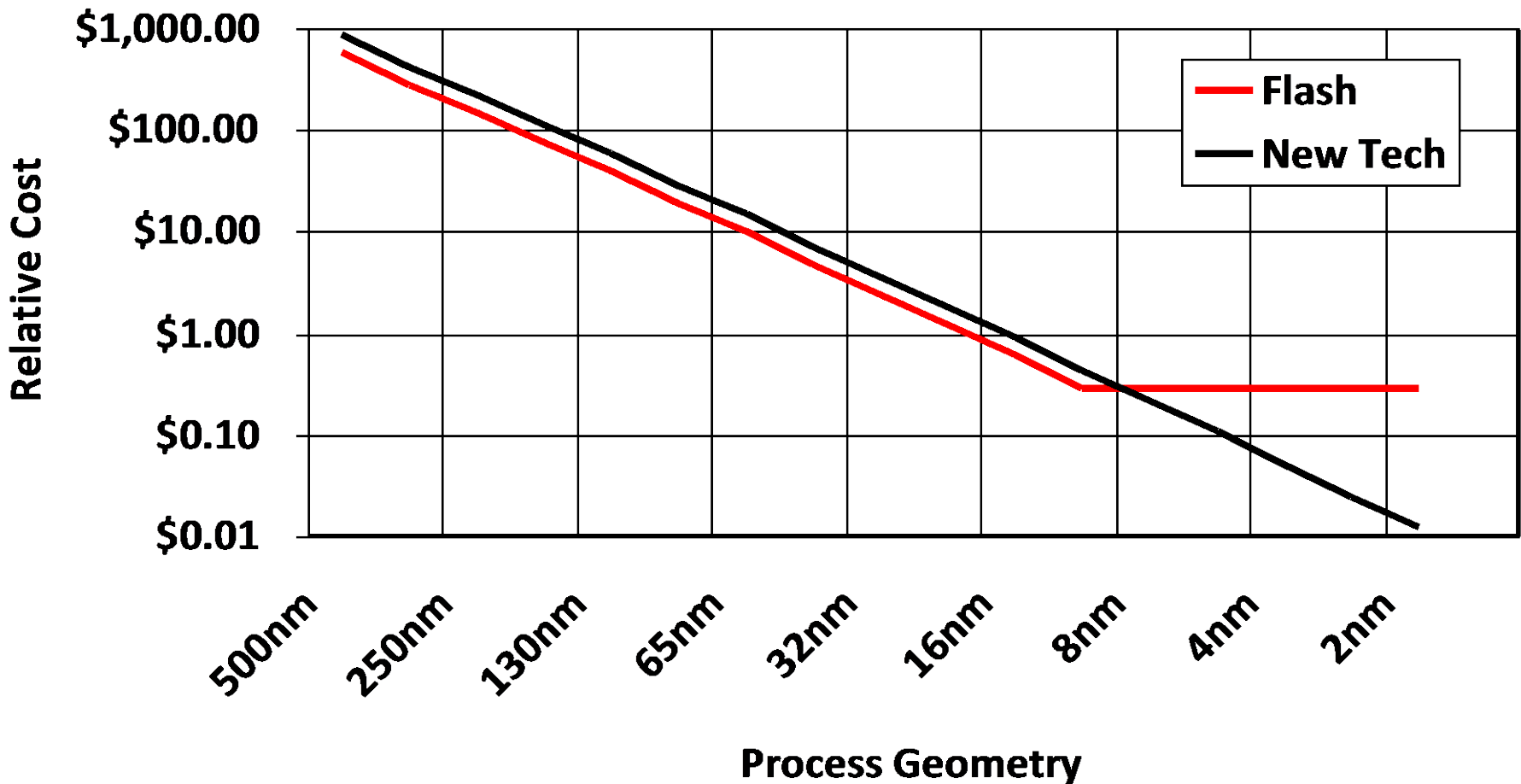
Cataclysmic Changes Coming Soon

- Scaling Limits
 - We can't make transistors any smaller
- New Storage Hierarchies
 - You think SSDs were disruptive? Just wait!
- More Layers Will Be Added
 - It's all about touch rates and response time
- Processors Must Adapt

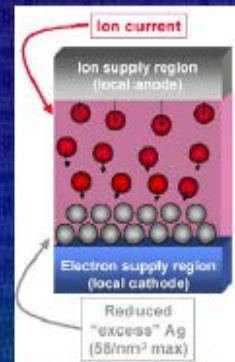
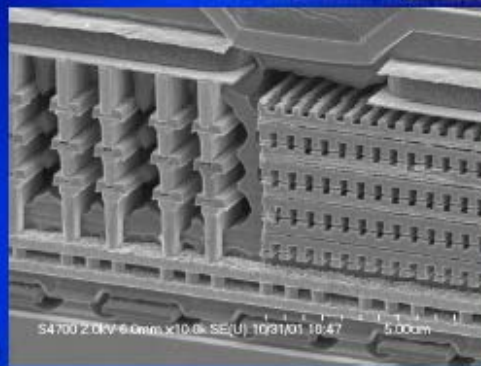
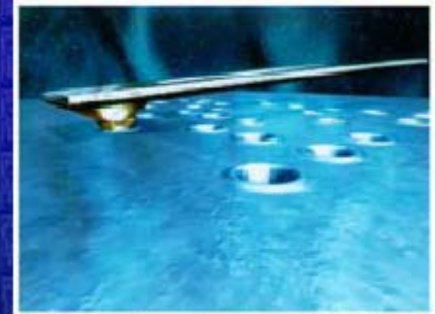
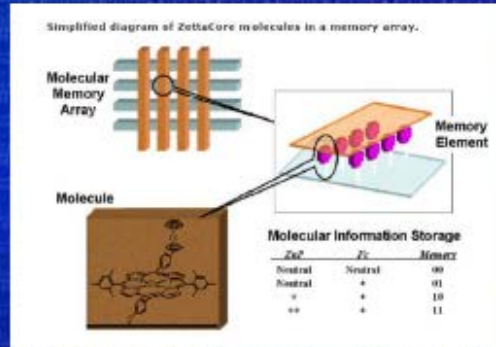
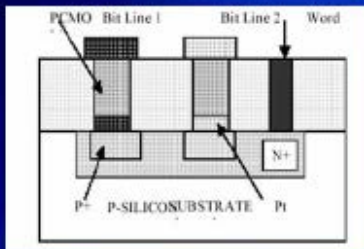
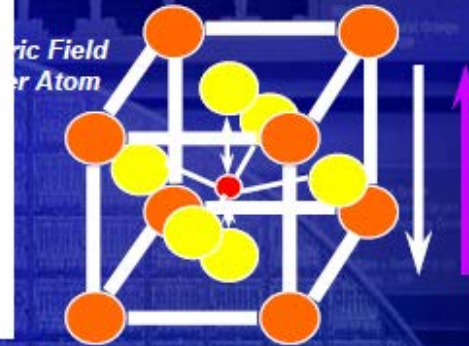
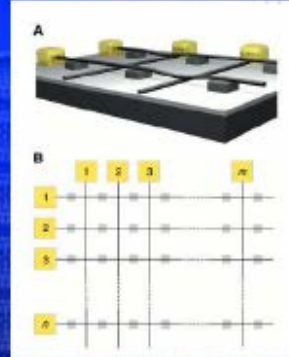
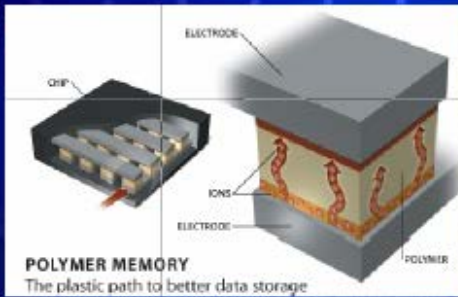
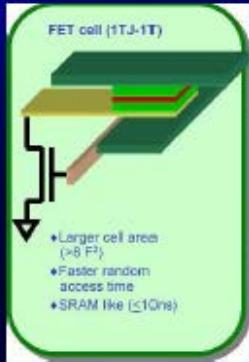
A photograph of a traditional Chinese roof with ornate sculptures and a row of mythical creatures. The roof is dark, possibly black, with a row of golden-brown sculptures along the ridge. From left to right, the sculptures include a large dragon-like creature with horns, followed by several smaller mythical creatures, including what appear to be lions and horses. The roof is covered in snow, and the background is a plain, light-colored sky. The text "SCALING LIMITS" is overlaid in white, bold, sans-serif font across the center of the image.

SCALING LIMITS

Scaling Limits Create Opportunities for New Memories



No Shortage of Options



intel

Today's Memories Are Limited

	SRAM	DRAM	ROM	EEPROM	NOR	NAND
Nonvolatile	No	No	Yes	Yes	Yes	Yes
Erasable	Yes	Yes	No	Yes	Yes	Yes
Programmable	Yes	Yes	Factory	Yes	Yes	Yes
Smallest Write	Byte	Byte	N/A	Byte	Byte	Page
Smallest Read	Byte	Page	Byte	Byte	Byte	Page
Read Speed	V Fast	Fast	Fast	Fast	Fast	Slow
Write Speed	V Fast	Fast	N/A	Slow	Slow	Slow
Active Power	High	Med	Med	Med	Med	Med
Sleep Power	V Low	High	Zero	Zero	Zero	Zero
Price/GB	High	Low	Low	High	Med	V Low
Applications	Small Fast	Main Memory	Stable Code Volume	Serial #, Trim	Code	Data

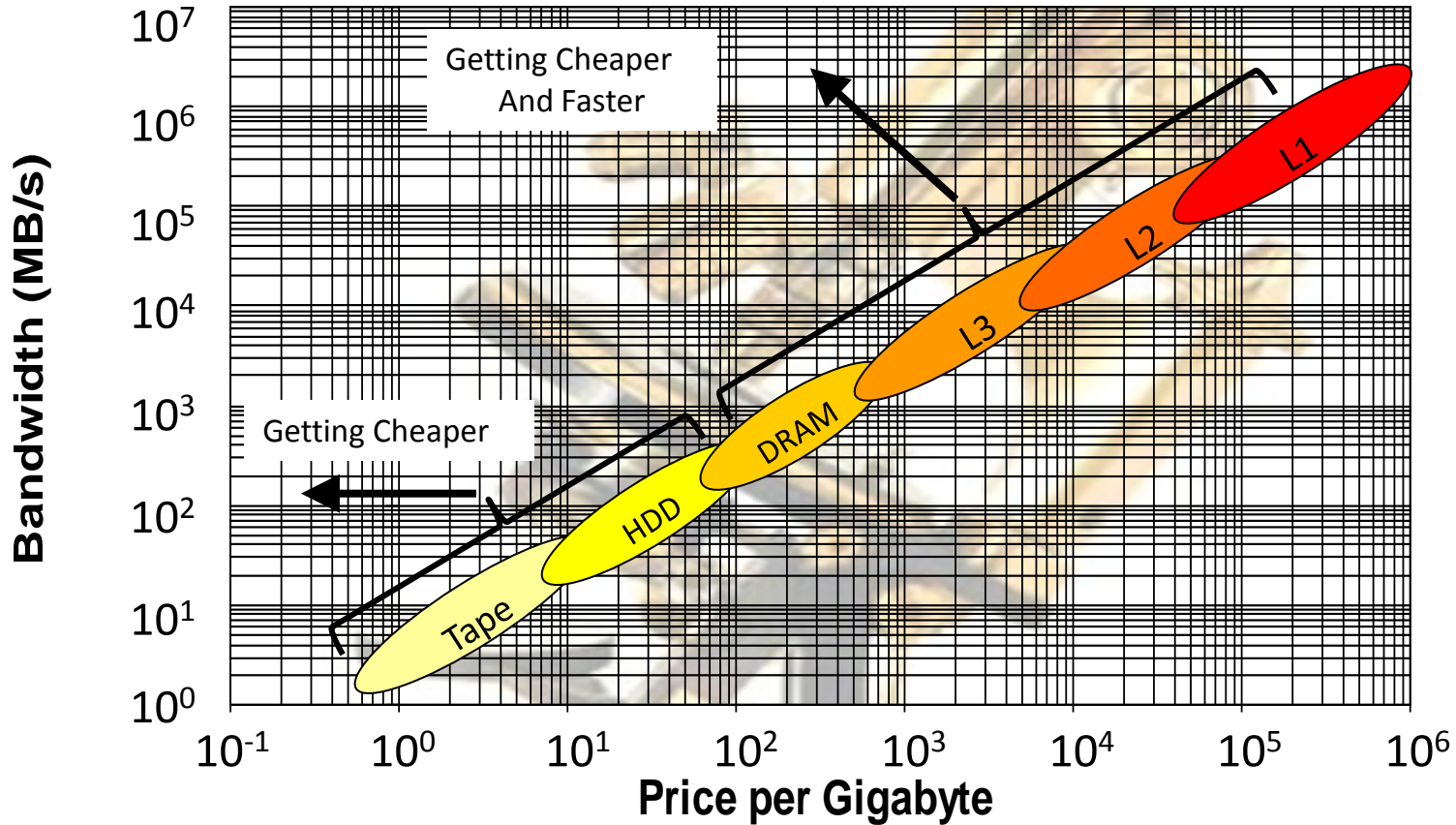
Emerging Memories Perform Better

	MRAM	ReRAM	FRAM	PCM	XPoint
Nonvolatile	Yes	Yes	Yes	Yes	Yes
Erasable	Yes	Yes	Yes	Yes	Yes
Programmable	Yes	Yes	Yes	Yes	Yes
Smallest Write	Byte	Byte	Byte	Byte	Byte
Smallest Read	Byte	Byte	Byte	Byte	Byte
Read Speed	Fast	Fast	Fast	Fast	Fast
Write Speed	Fast	Fast	Fast	Fast	Fast
Active Power	Low	Med	Low	High	High?
Sleep Power	Low	Low	Low	Low	Low
Price/GB	High	High	High	High	High?
Applications	Niche	TBD	Low Power	Obsolete	Main Memory



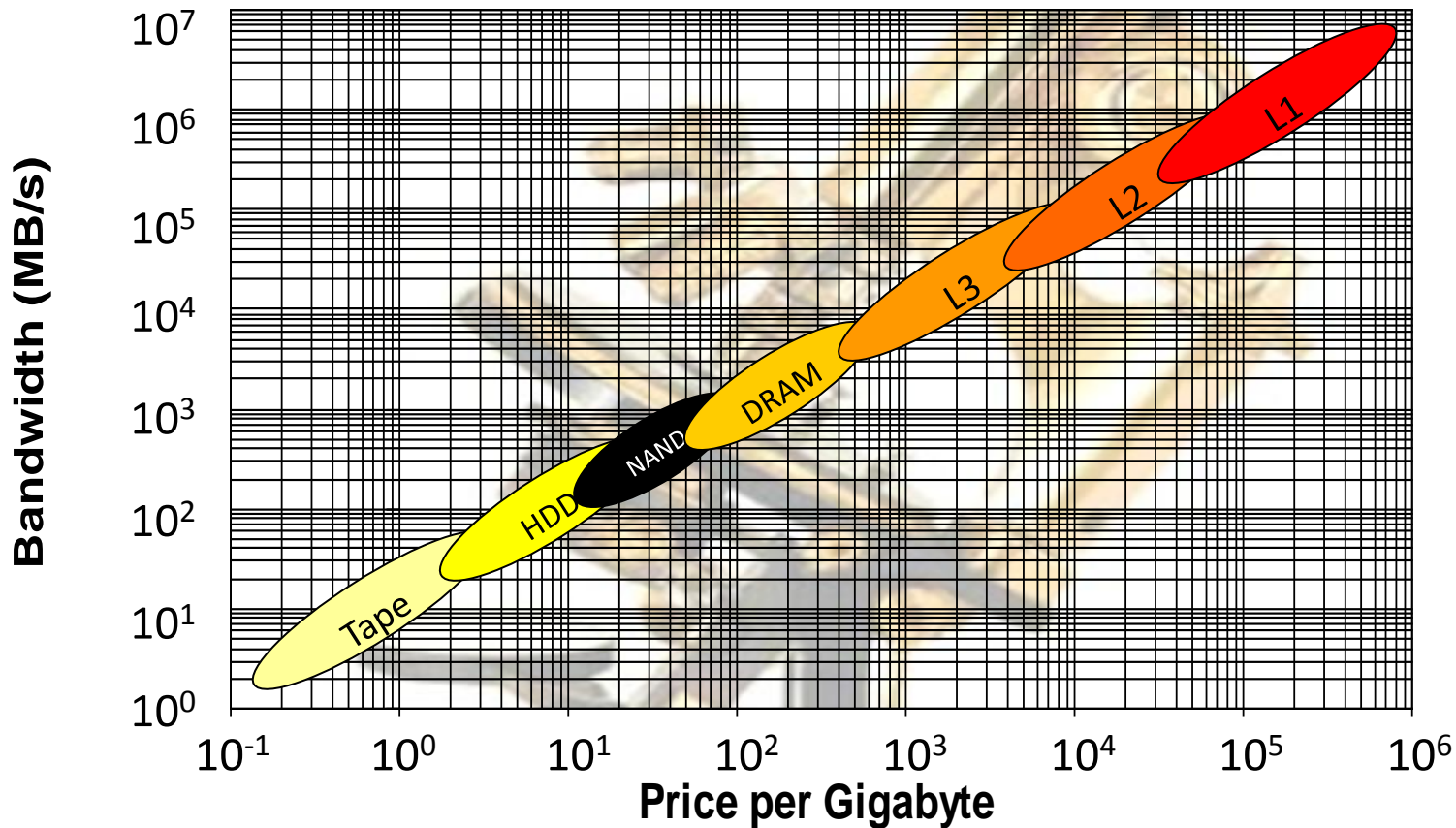
NEW STORAGE HIERARCHIES

Memory/Storage Hierarchy 2000



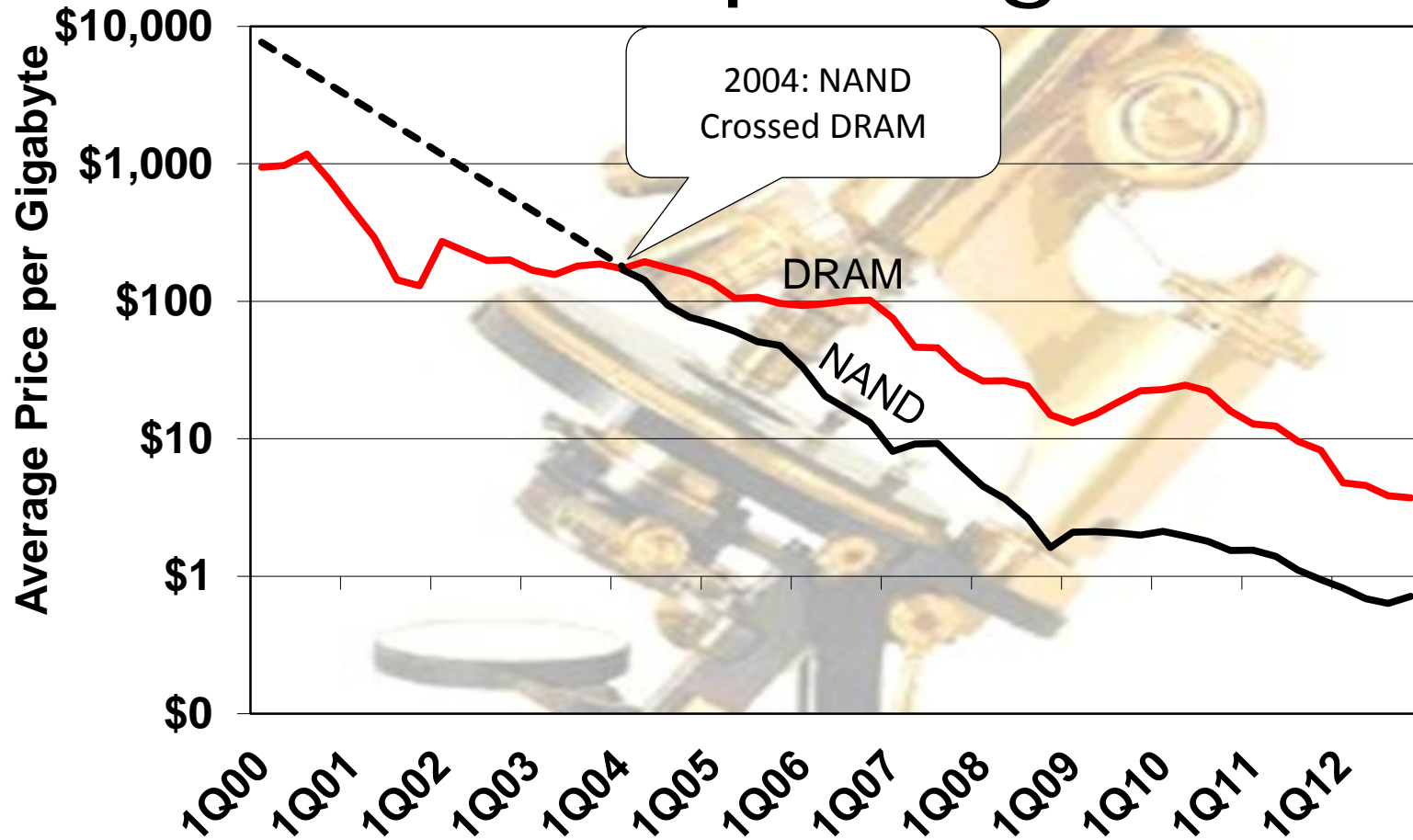
From: Objective Analysis: Solid State Drives in the Enterprise

NAND Flash SSDs Today Make Sense



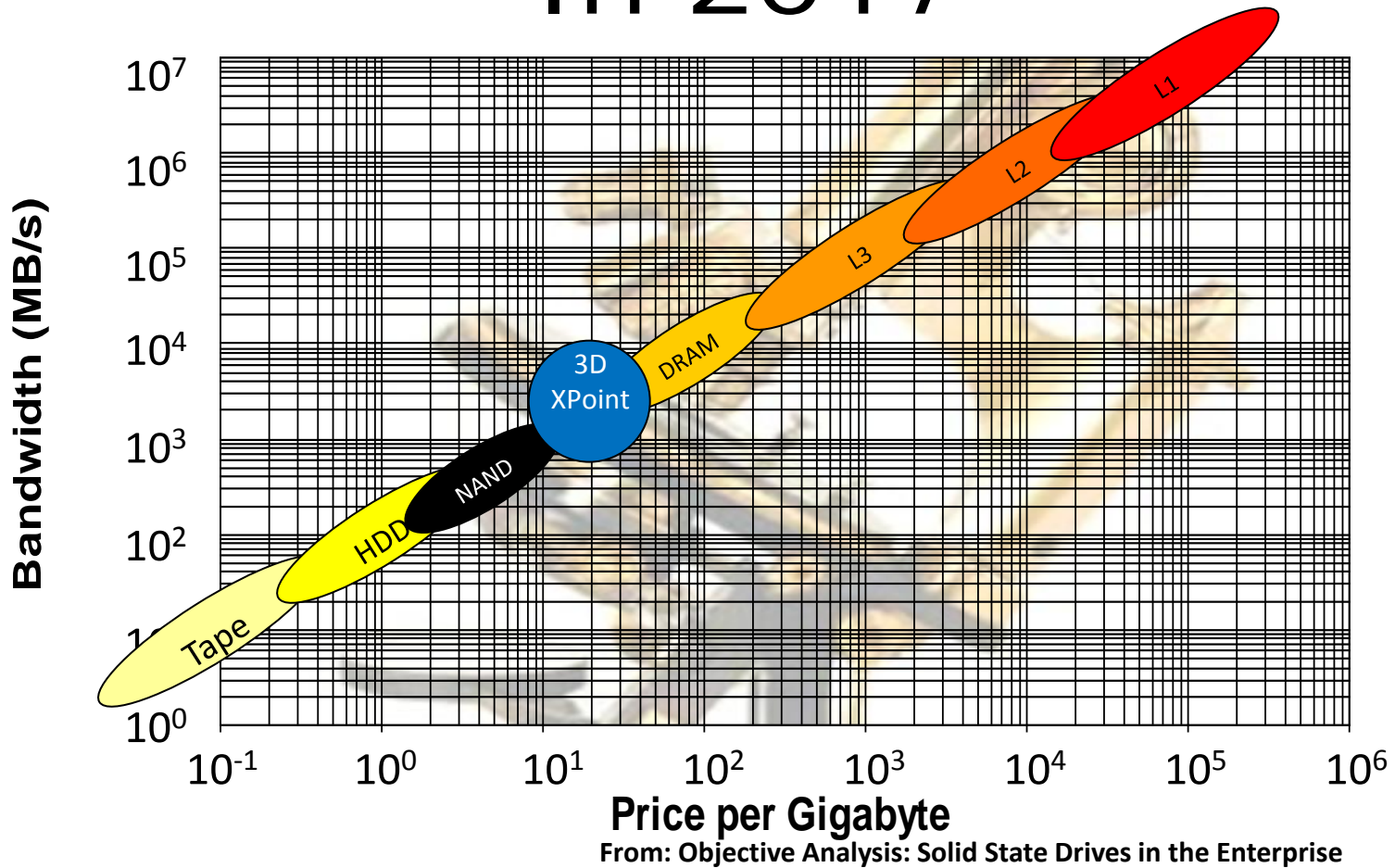
From: Objective Analysis: Solid State Drives in the Enterprise

Cost Brought Flash Into Computing



From: Objective analysis: Hybrid Drives: How, Why, & When?

3D XPoint Will Do The Same In 2017



Intel's & Micron's 3D XPoint Intro

3D XPoint™ Technology: An Innovative, High-Density Design

Cross Point Structure

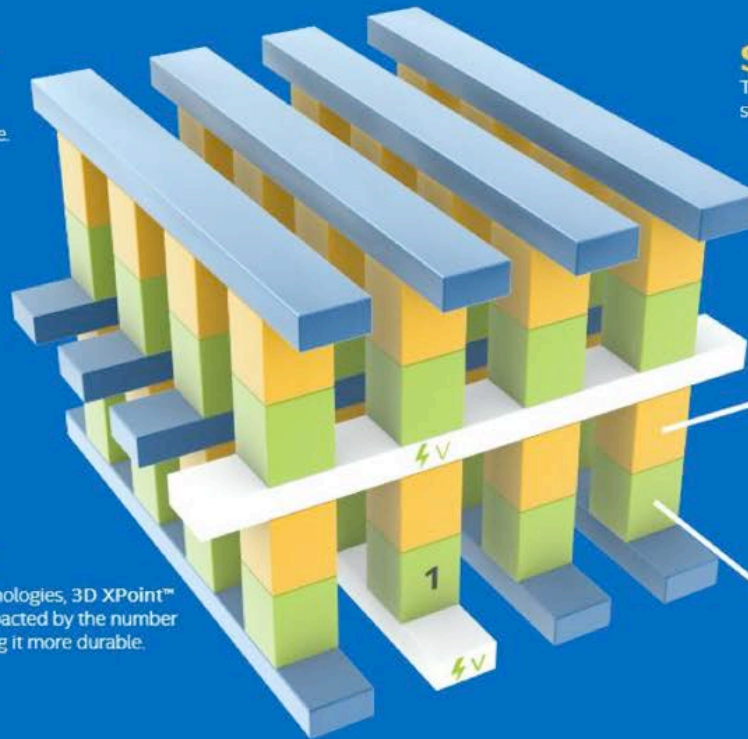
Perpendicular wires connect submicroscopic columns. An individual memory cell can be addressed by selecting its top and bottom wire.

Non-Volatile

3D XPoint™ Technology is non-volatile—which means your data doesn't go away when your power goes away—making it a great choice for storage.

High Endurance

Unlike other storage memory technologies, 3D XPoint™ Technology is not significantly impacted by the number of write cycles it can endure, making it more durable.



Stackable

These thin layers of memory can be stacked to further boost density.

Selector

Whereas DRAM requires a transistor at each memory cell—making it big and expensive—the amount of voltage sent to each 3D XPoint™ Technology selector enables its memory cell to be written to or read without requiring a transistor.

Memory Cell

Each memory cell can store a single bit of data.

Transforming the Memory Hierarchy

For the first time, there is a fast, inexpensive and non-volatile memory technology that can serve as system memory and storage.

~8x to 10x Greater Density than DRAM¹

3D XPoint™ Technology's simple, stackable, transistor-less design packs more memory into less space, which is critical to reducing cost.



3D XPoint™ Technology

Processor

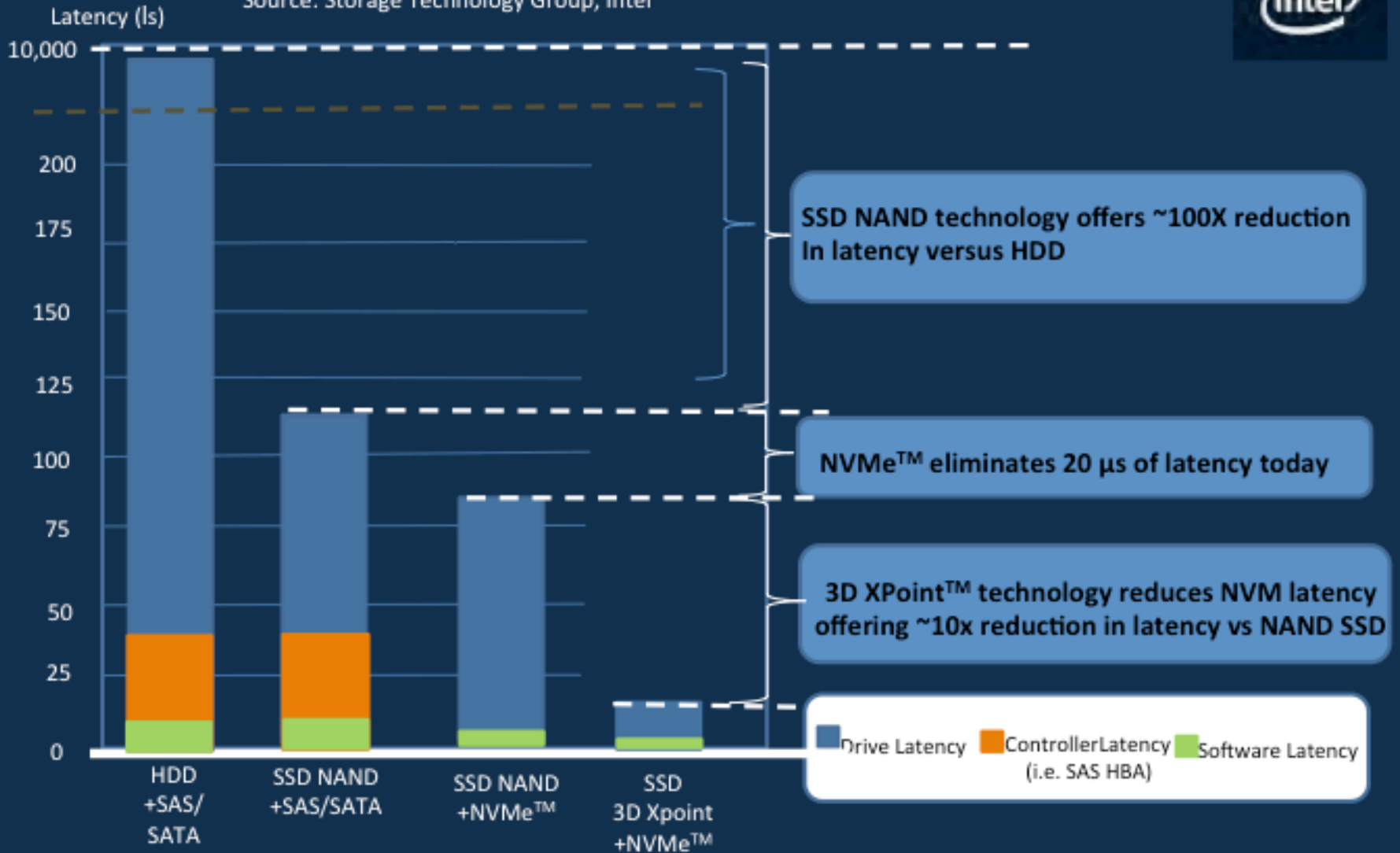
DRAM

3D XPoint™ Technology

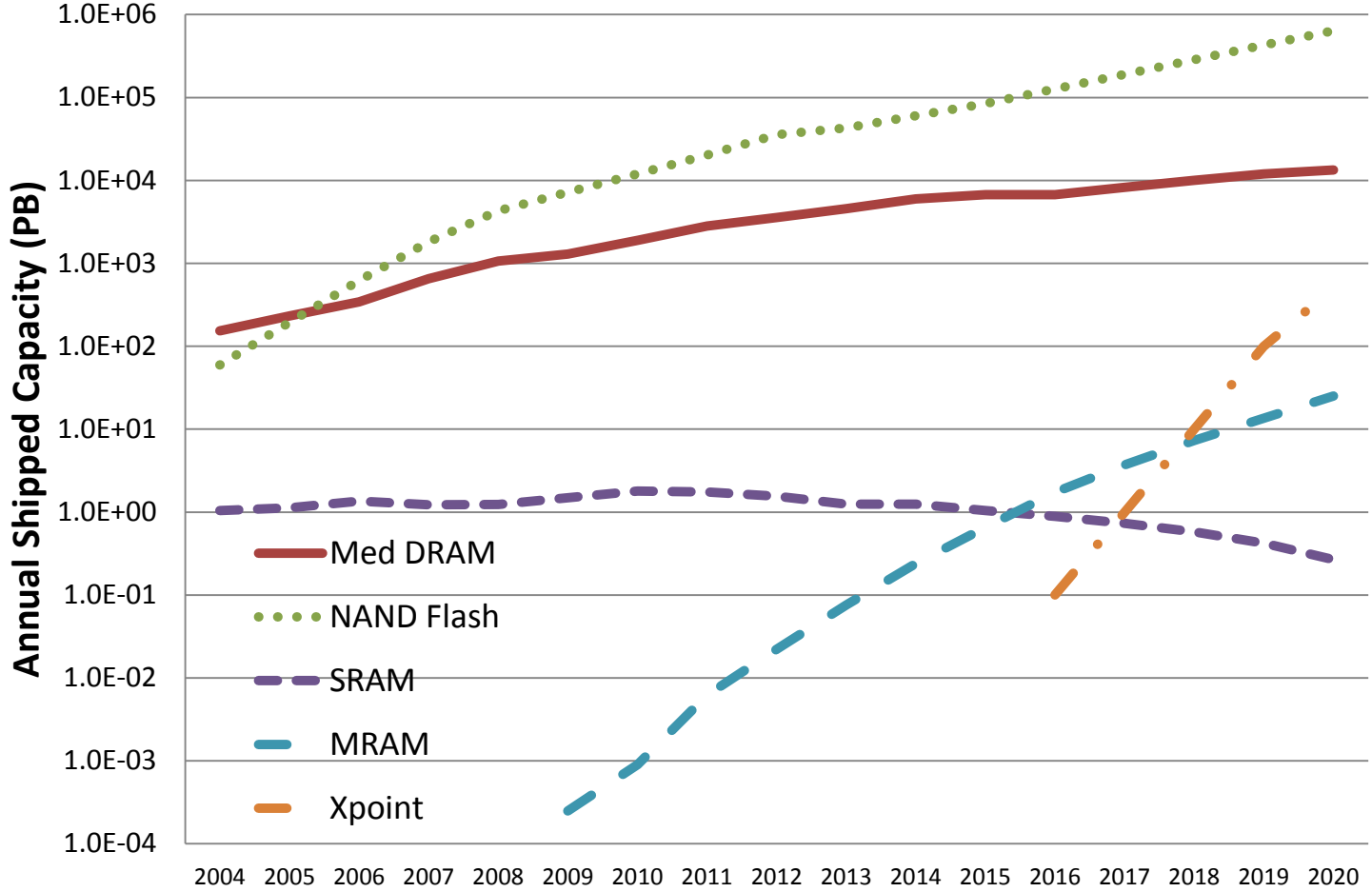
3D XPoint Slashes Latency



Source: Storage Technology Group, Intel



ANNUAL SHIPPED CAPACITY (PB) FOR DRAM, NAND FLASH, SRAM, MRAM AND 3D XPOINT

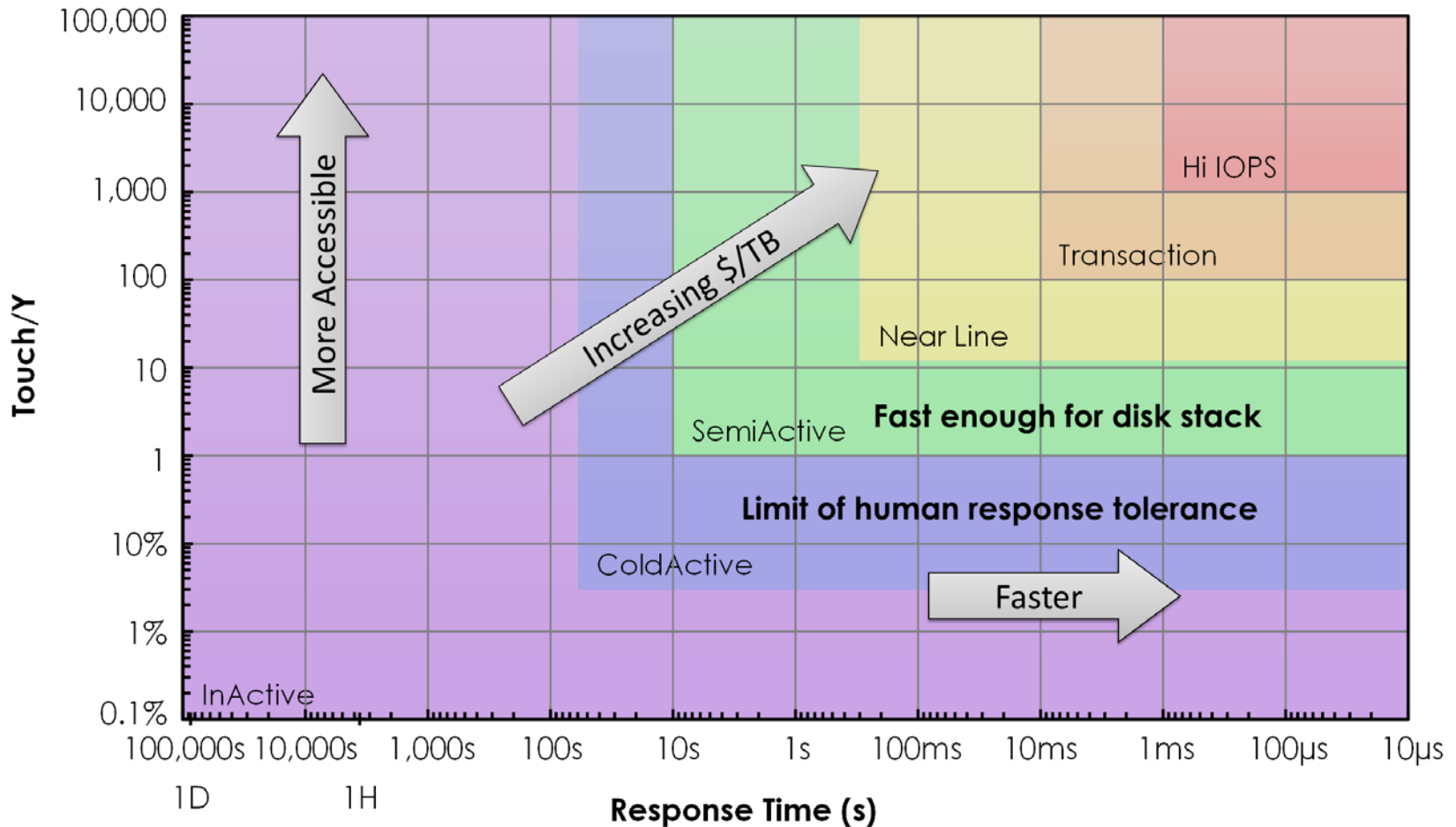


2015 EMERGING NON-VOLATILE MEMORY & SPIN LOGIC TECHNOLOGY AND MANUFACTURING REPORT, Coughlin Associates, 2015, <http://www.tomcoughlin.com/techpapers.htm>

A tall stack of sandwiches, approximately 10-12 layers high, made with whole-grain bread. The fillings include slices of meat (possibly ham or turkey), melted cheese, lettuce, tomato slices, and other vegetables. The sandwiches are stacked vertically, creating a dense, multi-layered structure.

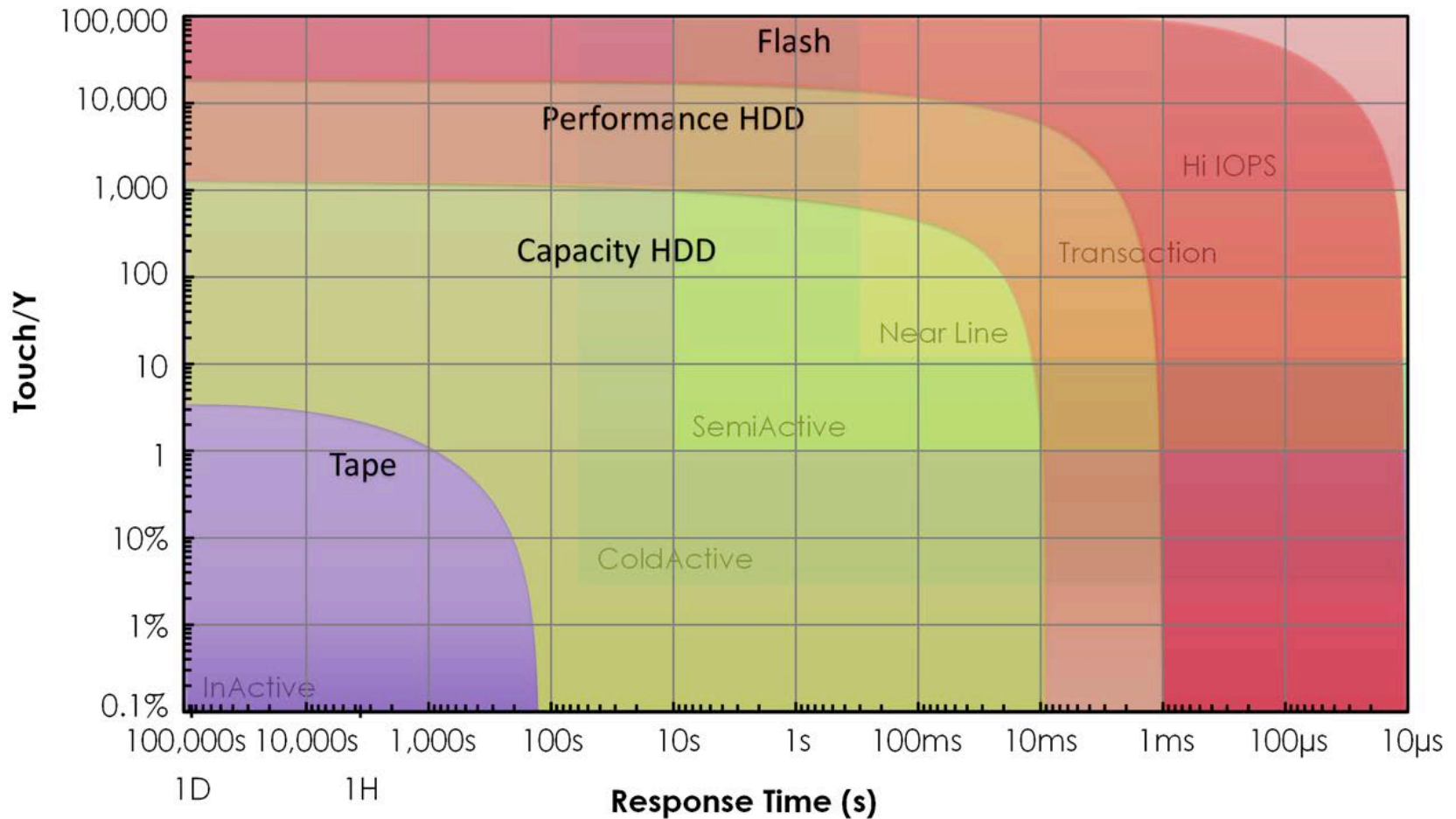
WHY MORE STORAGE LAYERS

“Touch Rates” vs. Response Time By Application



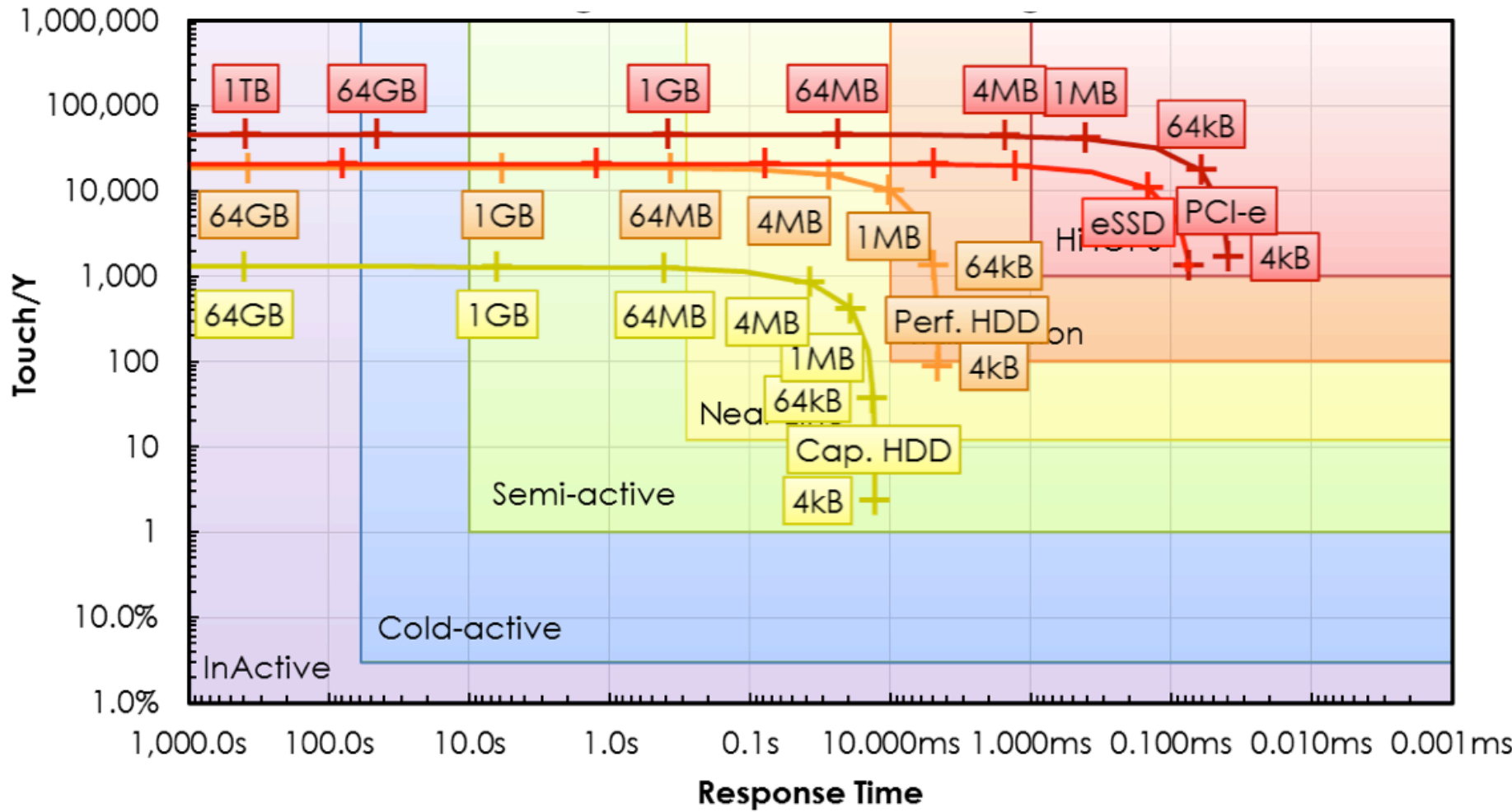
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Mapping This To Storage Technologies



2015 EMERGING NON-VOLATILE MEMORY & SPIN LOGIC TECHNOLOGY AND MANUFACTURING REPORT, Coughlin Associates, 2015, <http://www.tomcoughlin.com/techpapers.htm>

Real Products Mapped

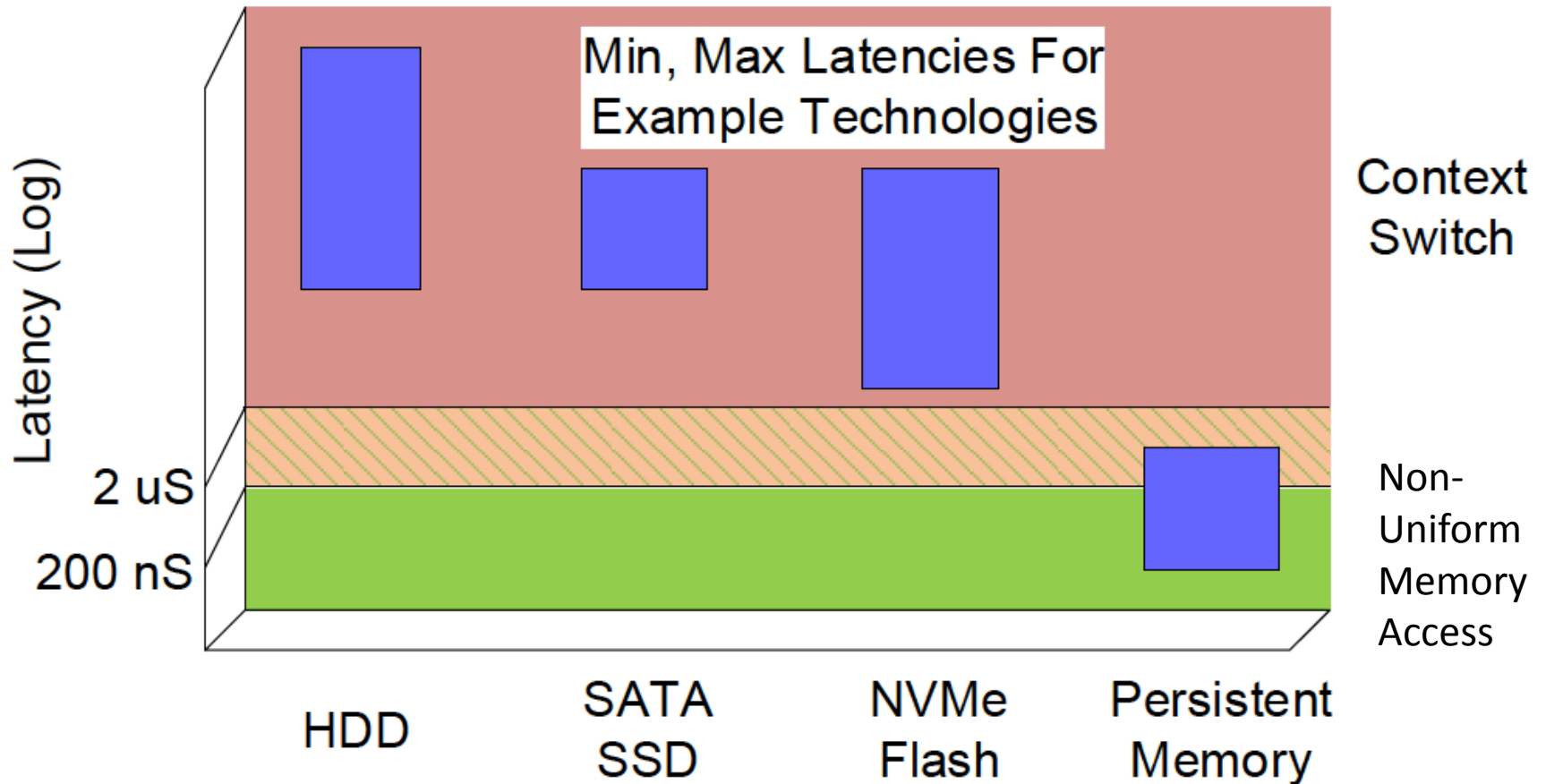


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PROCESSORS MUST ADAPT

Context Switches Become The Issue



Doug Voigt, HP, 2015 FMS

Persistent Memory Implications

- Retains data during a power loss
 - Instant recovery of state before power down
- Lower latencies than disk
- Lower power than DRAM
- Allows persistent states for Remote Direct Memory Access (RDMA)
- Supports “logic-in-memory architecture”
 - Could lead to new distributed computer architectures

Summary

- Scaling limits open doors to new memories
 - New architectures will create other opportunities
- NAND is NOW
 - 3D XPoint is coming soon
- Performance drives need for new layers
- New layers will drive new processor architectures
 - Application programs will also adapt



Thank You!

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Jim Handy, Objective Analysis