Realizing the Next Generation of Exabyte-scale Persistent Memory-Centric Architectures and Memory Fabrics

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Agenda

- Rapid growth in the data ecosystem
  - Importance of purpose-built technologies and architectures
- Current distributed systems architecture
  - Where should we attach persistent memory?
  - RDMA networking: Lowest latency remote memory access
  - Compute state of the art: Compute acceleration
- Persistent memory scale out
  - Memory pool size requirements
  - CPU attached memories access via RDMA networking vs. memory fabrics
  - Memory fabrics latency requirements
- Conclusions
Diverse and connected data types

Tight coupling between Big Data and Fast Data

BIG DATA
- Data Aggregation
- Batch Analytics
- Modeling
- Artificial Intelligence
- Machine Learning
- SMART MACHINES
- REAL-TIME RESULTS
- MOBILITY
- INSIGHT
- PREDICTION
- PRESCRIPTION

FAST DATA
- Performance
- Scale

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From general purpose to purpose built

Architectures designed for Big Data, Fast Data applications

Big Data

Expanding applications and workloads

General purpose compute-centric architecture

Fast Data

- Solutions
- Systems
- Platforms
- Devices
Workload diversity

Demanding diverse technologies and architectures

Big Data → Purpose-built data-centric architectures → Fast Data

Storage-centric architecture

Capacity-centric scale

Storage: HDD, SSD

Memory: NVM, DRAM, SRAM

Interconnect: Storage Semantic Data Flow, Memory Semantic Data Flow

Compute: Storage SOC, General Purpose CPU, GPU, FPGA, ASIC

Memory-centric architecture

Performance-centric scale
### Where should we attach persistent memory?

<table>
<thead>
<tr>
<th>Physical interface</th>
<th>DIMM</th>
<th>DIMM/other</th>
<th>PCIe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logical interface</td>
<td>Non-standard DDR4, NVDIMM-P</td>
<td>DMI for Power 8, CCIX, OpenCAPI 3.1, Rapid-IO, gen-Z</td>
<td>NVMe, DC express*</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pros</th>
<th>Cons</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Low latency</td>
<td>• CPU memory controller has to implement specific logical interface</td>
<td>• Higher latency (~1us)</td>
</tr>
<tr>
<td>• High bandwidth</td>
<td>• Not suited for stochastic latency behavior</td>
<td>• CPU memory controller has to support</td>
</tr>
<tr>
<td>• Power proportional</td>
<td>• Not hot pluggable</td>
<td>• May have higher power consumption</td>
</tr>
<tr>
<td>• Coherent through memory controller</td>
<td>• BIOS needs change</td>
<td></td>
</tr>
</tbody>
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- **Pros:**
  - Low latency
  - High bandwidth
  - Power proportional
  - Coherent through memory controller

- **Cons:**
  - CPU memory controller has to implement specific logical interface
  - Not suited for stochastic latency behavior
  - Not hot pluggable
  - BIOS needs change

- **Logical Interfaces:**
  - DIMM for CPU BUS: PARALLEL
  - DIMM/other for CPU BUS: SERIAL
  - PCIe for SERIAL PERIPHERAL BUS
Memory fabric may mean different things to different people:

- Page fault trap leading to RDMA request (incurs context switch and SW overhead)
- Global address translation management in SW, leading to LD/ST across global memory fabric
- Coherence protocol scaled out, global page management and no context switching
RDMA networking: Latency

- As a direct memory transfer protocol RDMA is already suited to accessing remote byte-addressable persistent memory devices.
- Typical latency for RDMA reads: 1.6-1.8us
  - For PCIe attached RNICs on host and target nodes.
- Simultaneous PCIe tracing reveals as little as 600ns spent actually transferring data over the network.
  - 70% of latency is spent in memory or PCIe-protocol overhead.
- How much can be saved by attaching memory directly to network fabric (i.e., no PCIe overhead).
  - Maximal benefit (~1.0 us) would require integrated RNIC interfaces on both Initiator and Target.

**BREAKDOWN OF A 16-BYTE RDMA_READ REQUEST**

- **T=0 ns**: CPU writes 64B WR to Mellanox “Blue Flame” register (NO DOORBELL?)
- **T=393 ns**: Data read request TLP received on “Remote” side.
- **T=812 ns**: Root Complex replies with 16B completion.
- **T=1064 ns**: RDMA Data written to User Buffer.
  - T+1118 ns: 64B Write TLP (assumedly to Completion Queue?) Followed immediately by mysterious 4B Read.
- **T=1377 ns**: Completion of mysterious 4B Read.
- **T=1815 ns**: CPU issues next RDMA read request.
RDMA to persistent memory latency

Raw RDMA access to remote PCM via PCIe peer2peer is 26% slower than to remote DRAM
Compute accelerators

- **Traditional distributed system:**
  - Memory accessible only via general purpose CPU or via RDMA

- **Distributed system with compute accelerators, with own memory:**
  - FPGA, GP-GPU, ASIC
  - Compute accelerators need large memory bandwidth and may drive need for memory appliances (e.g. NVLink)

- **Data (memory) centric architecture:**
  - Large number of compute devices (Cores, FPGA, GP-GPUs, ASIC) assessing large pool of memory
The emergence of memory fabric

Memory fabric may mean different things to different people:

- Page fault trap leading to RDMA request (incurs context switch and SW overhead)
- Global address translation management in SW, leading to LD/ST across global memory fabric
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Latency requirements

- It is not trivial to determine the threshold latency, for which CPU load operation still makes sense:
  - As opposed to using block IO, which allows more efficient CPU utilization
- Based on slowing down DRAM, and executing large number of benchmarks, we determine soft threshold of approximately:
  - 500 ns – 1 us

NORMALIZED EXECUTION TIME

Impact of latency on execution time
(Intel Xeon, DRAM frequency settings changed in BIOS)
Persistent memory scale-out

- **Exabyte scale memory system requirements:**
  - Assume exabyte scale, or at least many 10’s of Petabytes distributed in large number of nodes
  - Assuming 256 Gb/die, the amount of persistent memory per node can be estimated as 8-16 TB:
    - Limited by total power budget – SoC and media
  - **Number of nodes required is quite large:**
    - For 1 PB: 64 nodes
    - For 64 PB: 4096 nodes
  - Assuming 3D torus, the number of hops (one direction) is:
    - For 1 PB: 64 nodes; 8 hops
    - For 64 PB: 4096 nodes; 48 hops
  - **Path for improvement is:**
    - Increasing dimensionality of the network topology – expensive
    - Improving power-density envelope of the memory technology in order to pack more capacity per node

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<table>
<thead>
<tr>
<th>Topology</th>
<th>Block diagram</th>
<th>#neighbors</th>
<th>throughput</th>
<th>latency</th>
<th>cost</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1D torus</td>
<td></td>
<td>2</td>
<td>O(n)</td>
<td>O(n^(-3))</td>
<td>O(n)</td>
<td></td>
</tr>
<tr>
<td>2D torus</td>
<td></td>
<td>4</td>
<td>O(n)</td>
<td>O(n^(0.33))</td>
<td>O(n)</td>
<td></td>
</tr>
<tr>
<td>3D torus</td>
<td></td>
<td>6</td>
<td>O(n)</td>
<td>O(n^(0.25))</td>
<td>O(n)</td>
<td>Latency is more likely O(n^0.25) due to loading</td>
</tr>
<tr>
<td>Hypercube</td>
<td></td>
<td>nD/2</td>
<td>O(n log n)</td>
<td>O(log n)</td>
<td>O(n log n)</td>
<td>Latency is more likely O(n^0.5) due to loading</td>
</tr>
</tbody>
</table>
End-to-end latency requirements

- Assuming that at least 8 hops across the cluster are required for remote memory access:
  - \( 8 \times \text{switch\_latency} + \text{raw\_memory\_latency} < 500 \text{ ns} - 1000 \text{ ns} \)

- Assuming raw memory latency is 100ns:
  - Switch\_latency < (50 – 100) ns

- Larger clusters and larger number of nodes will lead to significantly tighter latency requirement
Routable and switchable fabric:
- Require uniform fabric from card, to node to cluster level, with uniform switching and routing solutions

25Gb/s IP is available today:
- With a clear roadmap to at least 56Gb with PAM4
- Same fabric can be used on a node level to enable heterogeneous compute

Replace L2 Ethernet with custom protocol on top of 802.3 L1:
- Keep L1 from 802.3
- Rest is programmed with P4 allowing implementation of multiple protocols
- Supports innovation required for RAS
- FPGA or ASIC switch
P4 example: Gen-Z switch prototyping

- **BarefootTofino ASIC (or FPGA):**
  - 256-lane 25 GT/s Ethernet switch, 6 Tbit/s aggregate throughput
  - Supports P4 HDL, successor to OpenFlow enabling protocol innovation
  - Describe Gen-Z packet format in P4
  - Match-Action Pipeline (a.k.a. “flow tables”) enables line-rate performance
Conclusions

- RDMA networking today can be used to build memory fabric solutions
  - Typical measured latency in the 1.6-1.8 us range

- From performance perspective, achieving 500 ns fabric latency across exabyte (~10’s of PB) scale cluster puts significant pressure on persistent memory power and density, and memory fabric switch latency

- Protocol innovations are required to fulfill latency, throughput and RAS requirements
Creating environments for data to thrive

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