Unleashing MRAM as Persistent Memory

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Spin Transfer Technologies

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  - Challenges with the Memory Hierarchy
- What and Where is MRAM ?
- State of the Art pMTJ
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- MRAM Unbound

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The Creaking Pyramid

MRAM restricted to Embedded Nonvolatile

On-chip with CPU

SRAM

SRAM

SRAM

Mind the Gap

Volatile

DRAM

Mind the Gap

NAND

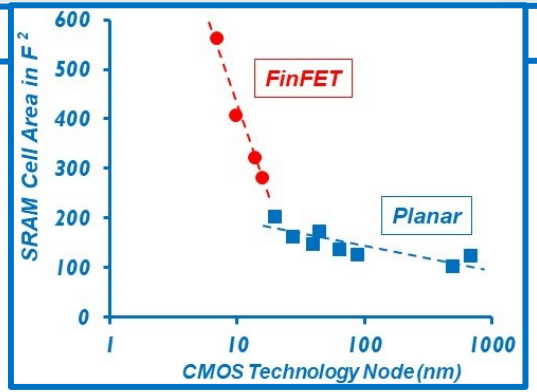
Nonvolatile

DISK

Speed

Capacity

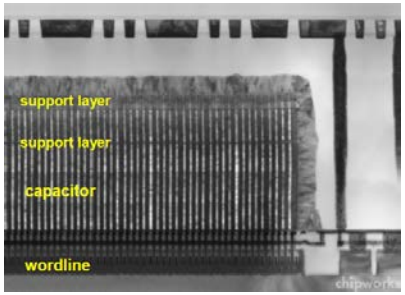
SRAM

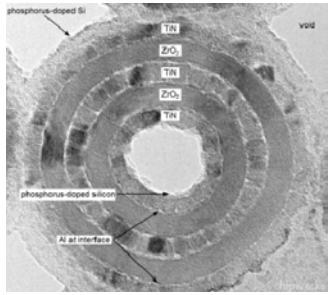


How to deal with leakage, size and inefficient scaling ?

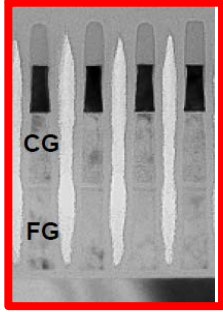
DRAM

What happens after ~30nm pitch ?



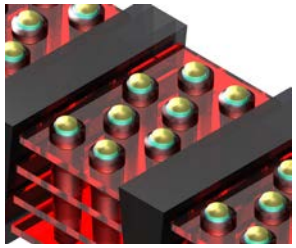


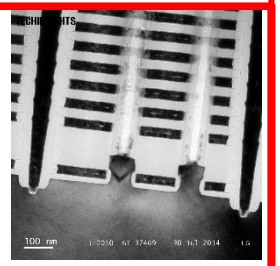
2-D NAND



3-D NAND

How tall can this go ? What is the real cost/bit ?





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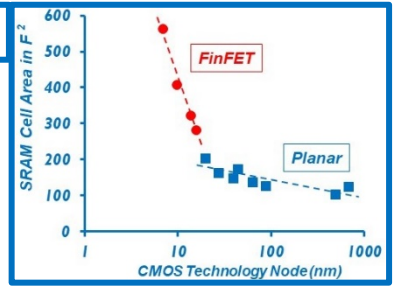
References: S.H. Kang et al., IEDM17., Various IEDMs; D. James, ASMC 2013; Techinsights 2014

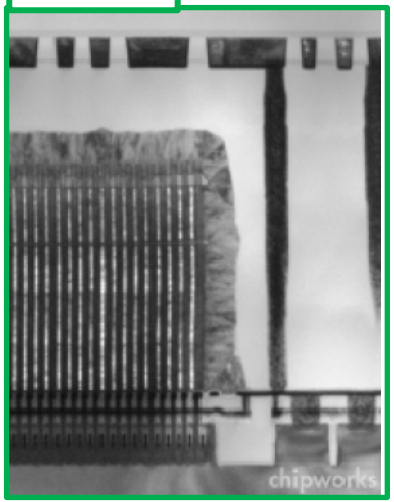
Challenges within the Memory Hierarchy

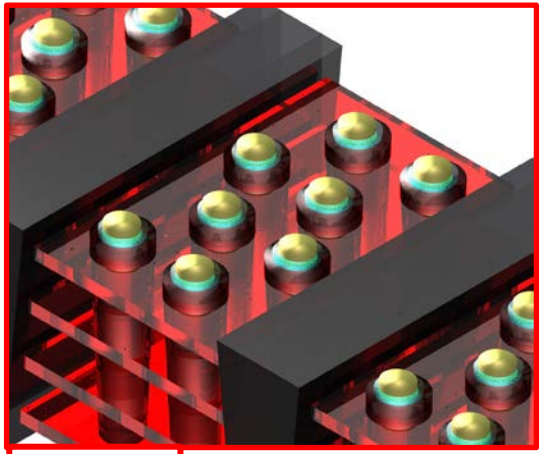
- ***SRAM***
  - Ever larger cache capacities needed
  - Inefficient scaling in FinFET CMOS
  - Large leakage currents dominating power dissipation
- ***DRAM***
  - Scalability reaching fundamental limits close to 30 nm pitch
  - Refresh power dissipation only getting worse
  - Not monolithically 3-D stackable
- ***NAND***
  - 3-D transition made but how tall can it go ?
  - Can it be laterally shrunk ?
  - What is the real cost per bit?
- ***The Gaps***
  - Does 3D XPoint™ fit the bill ?
  - Can ReRAM really be made to work ?
  - What else can fill The Gaps ?

SRAM



DRAM





3-D NAND

References: S.H. Kang et al., IEDM17., D. James, ASMC 2013

3D XPoint is an Intel/Micron Trademark

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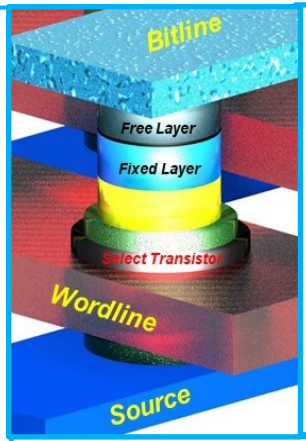
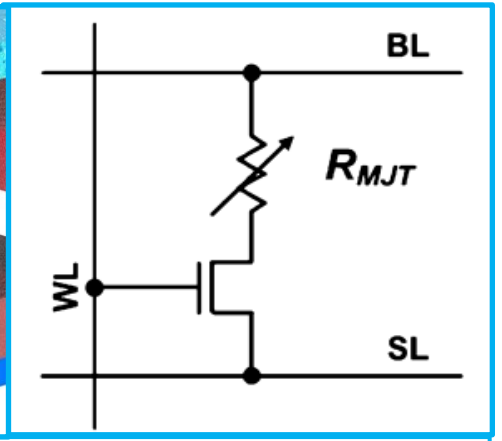
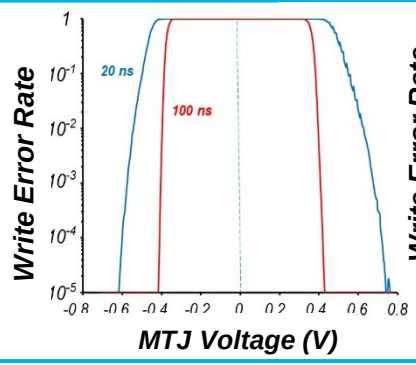
What is MRAM ?

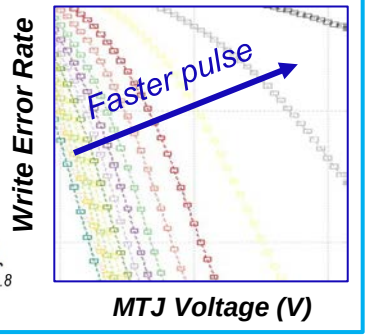
Spin-Transfer Torque Magnetic RAM

- A magnetic ReRAM using a perpendicular Magnetic Tunnel Junction ***(pMTJ)***
- Writing: flip M_{free} vector using electron spin to be parallel or anti-parallel with M_{fixed}
- Writing is ***stochastic*** – highly unusual for solid-state memory with mathematical description
- Reading: monitor current through MTJ
  - M_{fixed} and M_{free} parallel gives low resistance
  - M_{fixed} and M_{free} anti-parallel gives higher resistance
- Physics: the relative directions of M_{fixed} and M_{free} alter the Quantum Mechanical tunneling *transmission probability* through a thin MgO layer resulting in a *resistance change*









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Where is MRAM ?

- Emerging as the embedded NV memory of choice in advanced CMOS
  - Lower voltage and fewer masks than traditional Flash
- But…. Stochastic behavior limiting MRAM to embedded NV
  - Low *Write Error Rates* need *high switching current* and *long write pulses* which cause MgO *wearout* which limits *endurance*
- And…Retention and endurance are strongly inversely linked
  - NV *retention* needs stiff $\boldsymbol{M}_{free}$ which needs *high switching current* which causes MgO *wearout* which limits *endurance*
- Is MRAM confined to the embedded NV "cage" ?

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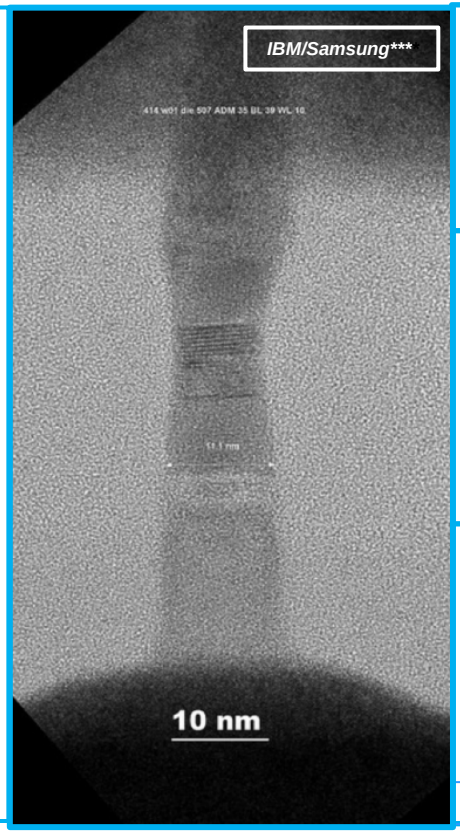
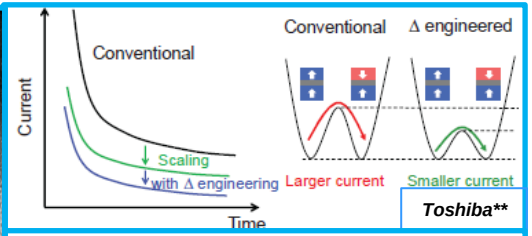
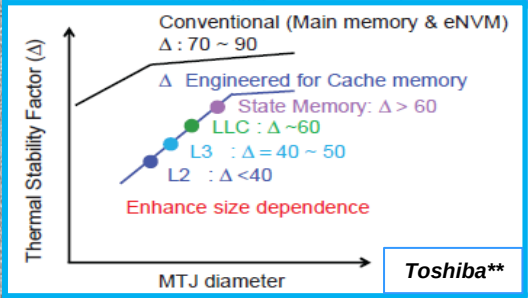
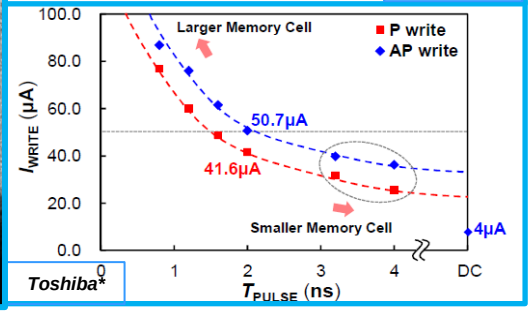
State of the Art pMTJ

- Retention – Endurance – Switching Current engineering through:
  - Scaling
  - Magnetic materials engineering
- Scaled soft magnetic pMTJ allows:
  - Lower switching current
  - Lower write power dissipation
  - High endurance
  - Smaller bitcells
  - Some level of persistence
- "Conservation of Misery"
  - Are R_{low} and R_{high} sufficiently separated ?
  - Manufacturing control and distributions
- Are SRAM/DRAM really replaceable ?
- Are The Gaps Fillable ?
- ***What can be done to help unleash MRAM?***









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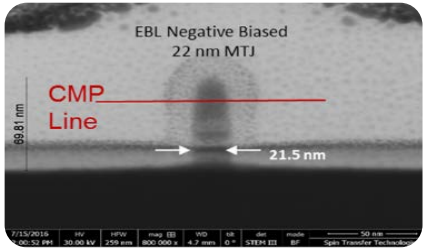
* K. Ikegami et al., VLSI Symp. 2014; ** IEDM 2015; *** http://bit.ly/2CM2C0J

Unleash MRAM with Spin Transfer Technologies

Unique Facility



Smaller pMTJ

10ns R/W times

Sub-20nm pillars

Gb Densities

Advanced process nodes

Partnered w/TEL

Unique Magnetics

Patented pMTJ Enhancement

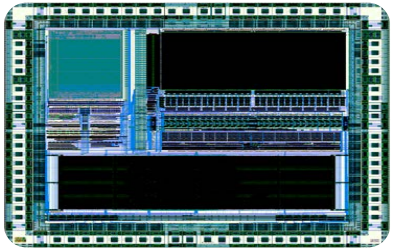
Faster Switching

Lowers R/W current

Critical for smaller geometries

Heavily Patented

Unique Circuits



Endurance Engine

Increases Endurance by up to six orders

Eliminates R/W Errors

Shortens time to high yield.

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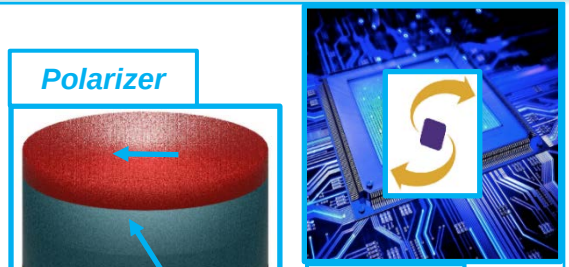
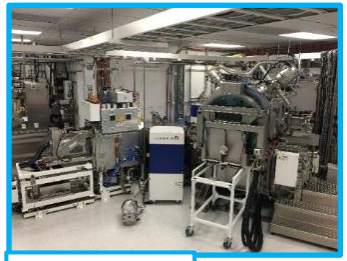
Unleash MRAM with Spin Transfer Technologies

- *STT's **Engine** – The "SanDisk of MRAM" and The Benefit of Synergy*
  - Significantly reduces the switching current requirements
  - Enhances speed to 10ns
  - Boosts endurance by 5 to 6 orders of magnitude with no retention change
  - Allows unique embedded NV and SRAM-like capabilities
  - Tuned to anyone's MRAM
  - Purely circuit-based with no materials or process changes
  - No user-visible errors
- *STT's **Polarizer***
  - Significantly reduces switching current requirements
  - Increased switching efficiency
  - Enhances free layer switching speed
  - Enhances read disturb stability
- *STT's **Magnetics***
  - Local highly flexible/fast MRAM fab – capable of 1x/2x nm pMTJs
  - BEOL MTJ integration
- *STT's **High Density Persistent Memory and Magnetic DRAM***
  - *Selector devices/processes*
  - *High density magnetics*

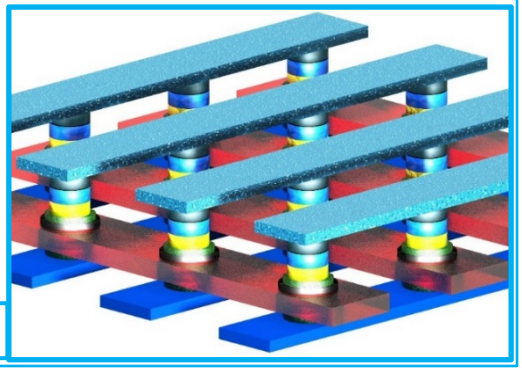


Engine

Polarizer



Magnetics



High Density

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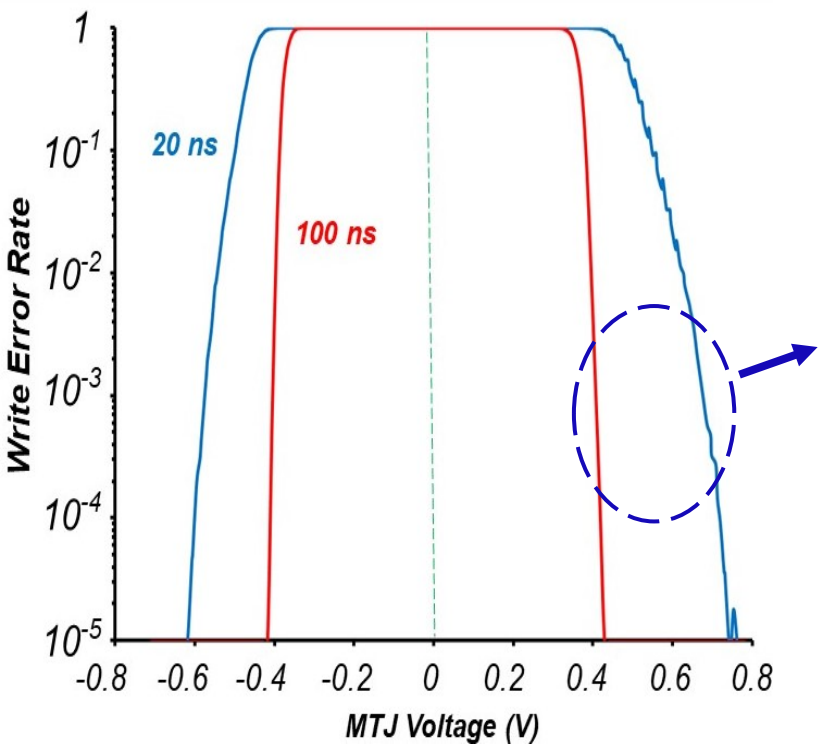
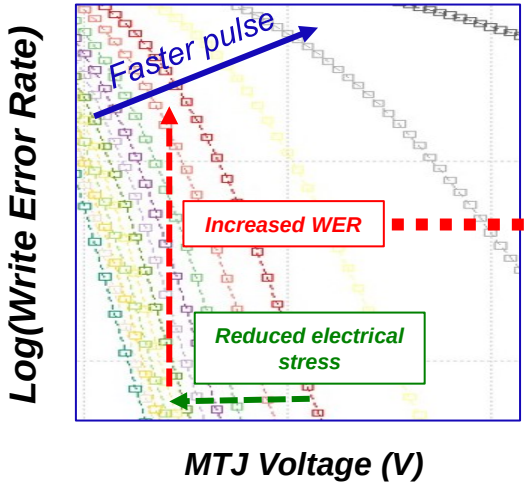
The Physics of The Engine





ENGINE

- ***Engine** allows **reduced electrical stress***
  - *Results in large endurance increase (5 – 6 orders)*
- ***Engine** deals with resultant **WER increase***
  - *Managed transparently to the user*
  - *No change in latency*
  - *Allows for faster pulses at high endurance*

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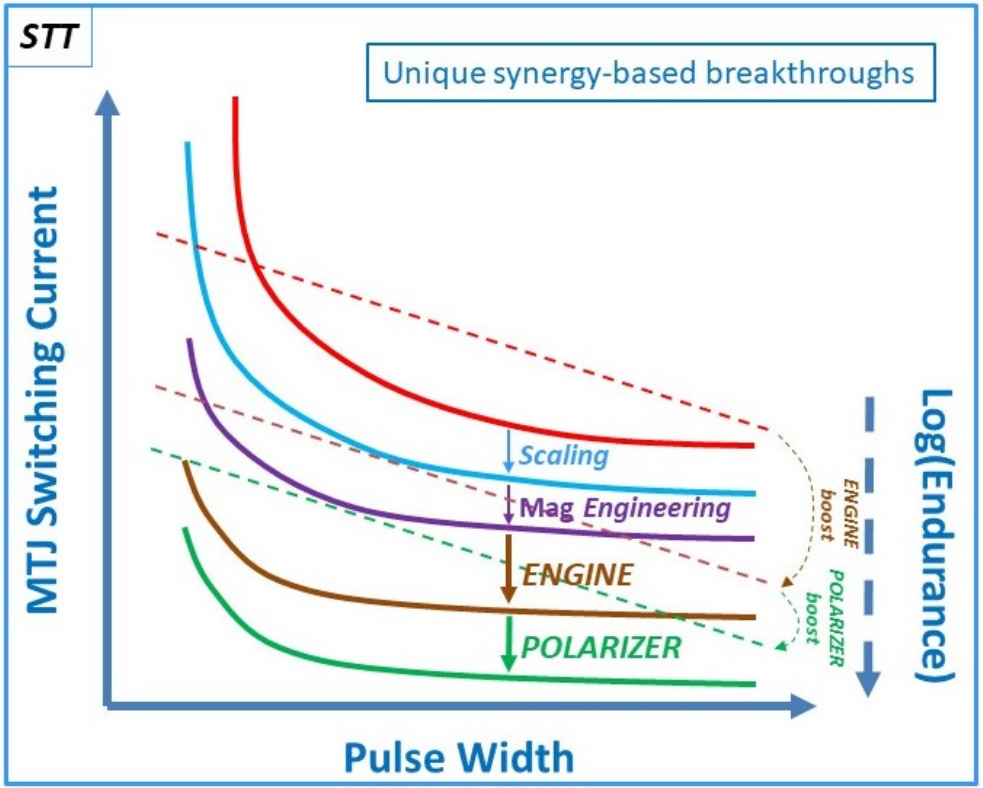
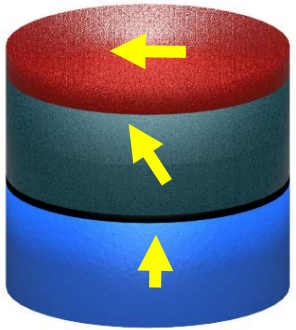
Unleash MRAM with Spin Transfer Technologies



ENGINE

Circuit – based Solution

POLARIZER



Magnetics – based Solution

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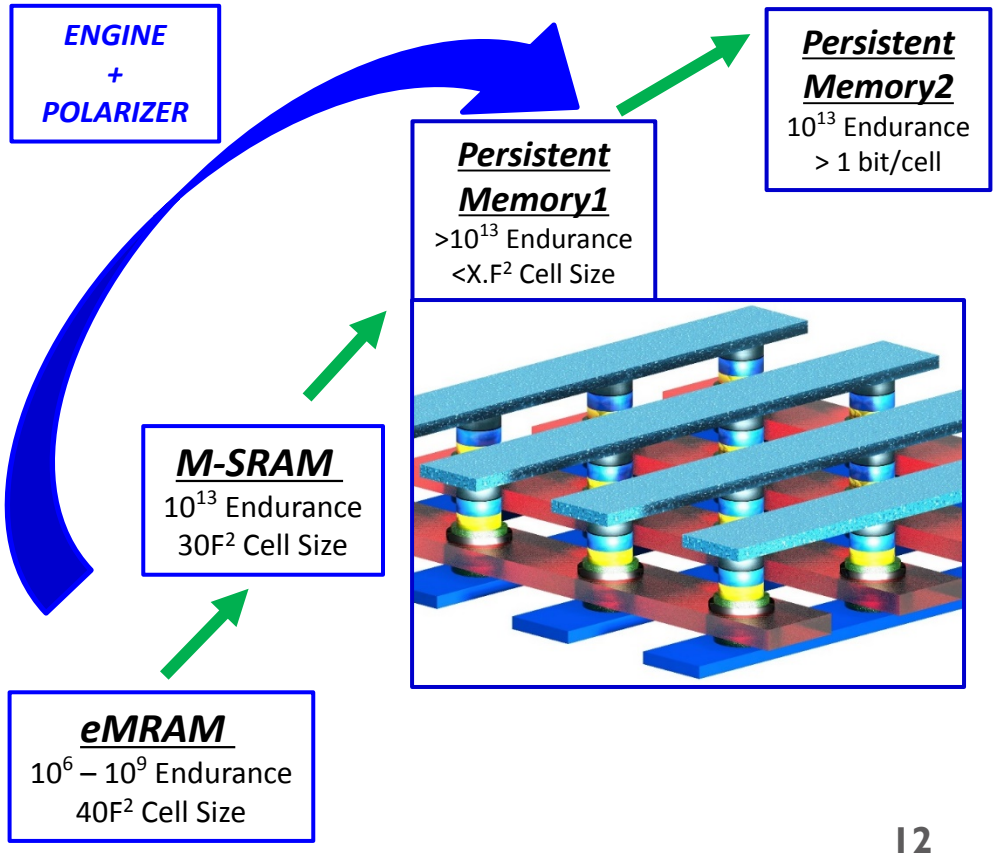
Unleash MRAM with Spin Transfer Technologies

Requirement	Spin's Advantage
Minimize switching currents - *Easier to integrate with selector devices* - *Minimize energy*	- *The **ENGINE** (IP)* - *The **POLARIZER** (IP)* - ***BEOL MTJ Nanofab*** - ***Magnetic materials expertise** (IP)*
***Ultra-small MTJs** for aggressive pitches*	- ***BEOL MTJ Nanofab*** - ***MTJ fabrication expertise** (IP)*
***Selector device** underneath MTJ*	- ***3D memory and device expertise** (IP)* - ***MRAM integration expertise** (IP)*
Density boosters	- ***> 1 bit per cell** (IP)*



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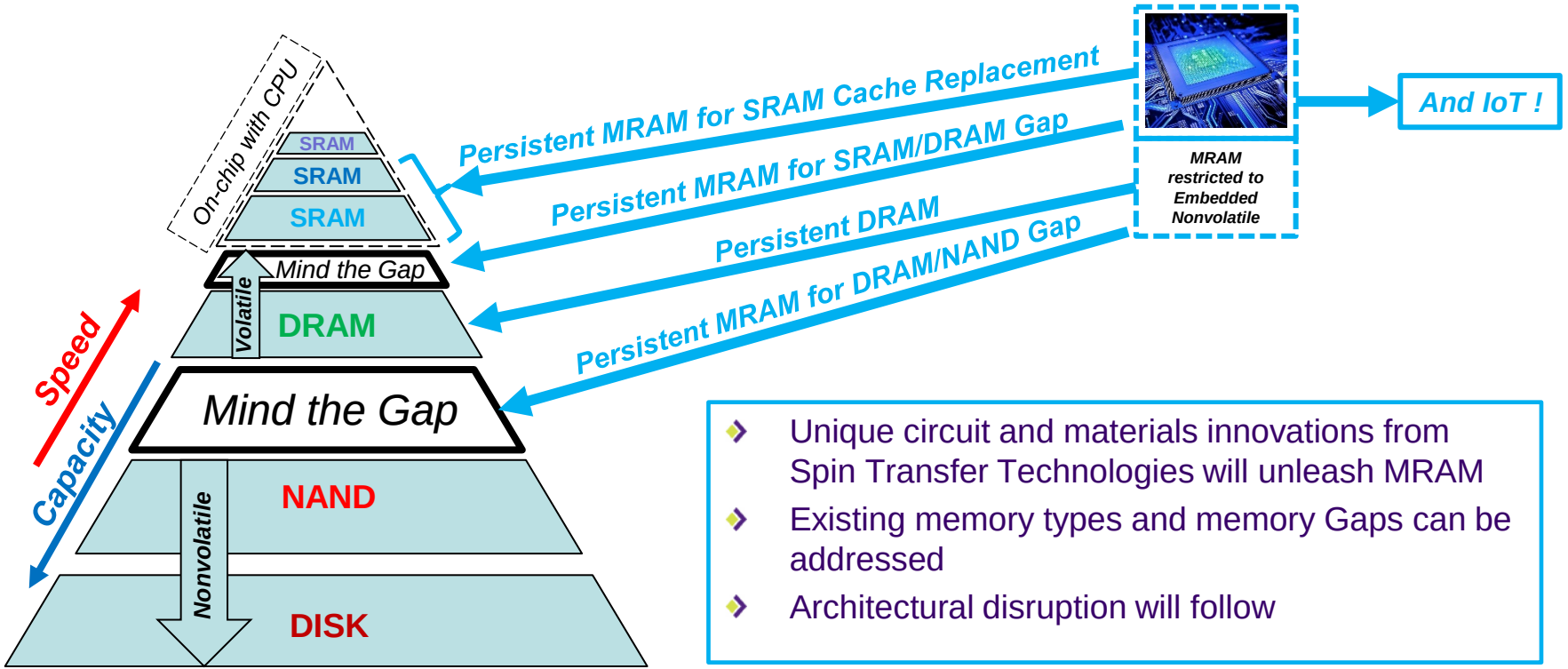
MRAM Unbound



- Unique circuit and materials innovations from Spin Transfer Technologies will unleash MRAM
- Existing memory types and memory Gaps can be addressed
- Architectural disruption will follow

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