Forthcoming Cross Point ReRAM

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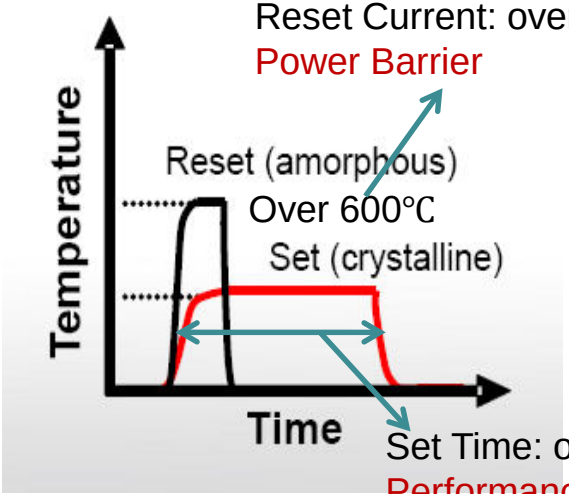
ReRAM: High Speed and Low Power

PCM

Two states of phase change material
Based on thermal operation

- Amorphous: low resistance
- Crystalline: high resistance



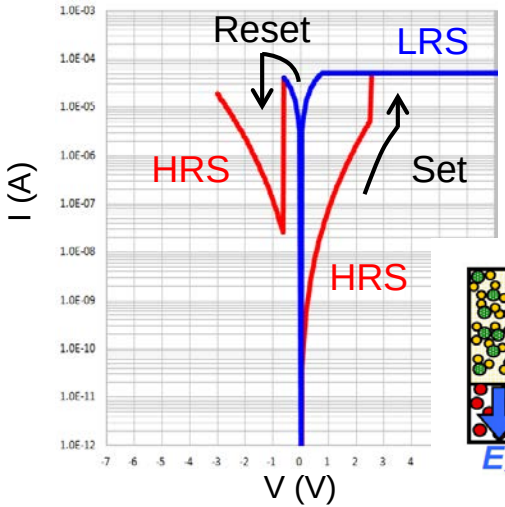
Reset Current: over 100uA
Power Barrier

Set Time: over 500ns
Performance Barrier

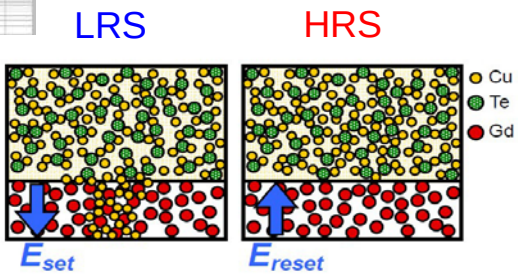
ReRAM

Two states of ReRAM material
Based on electric operation

- Metal bridge(pillar): low resistance
- No bridge(pillar): high resistance



Set/Reset Current: ~50uA
Set/Reset Time: <100ns

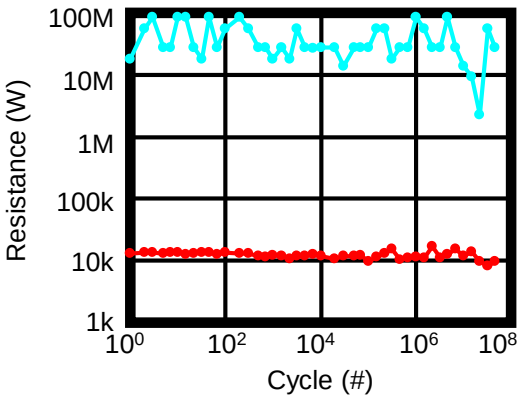


ReRAM: Faster Switching Possibility <5ns

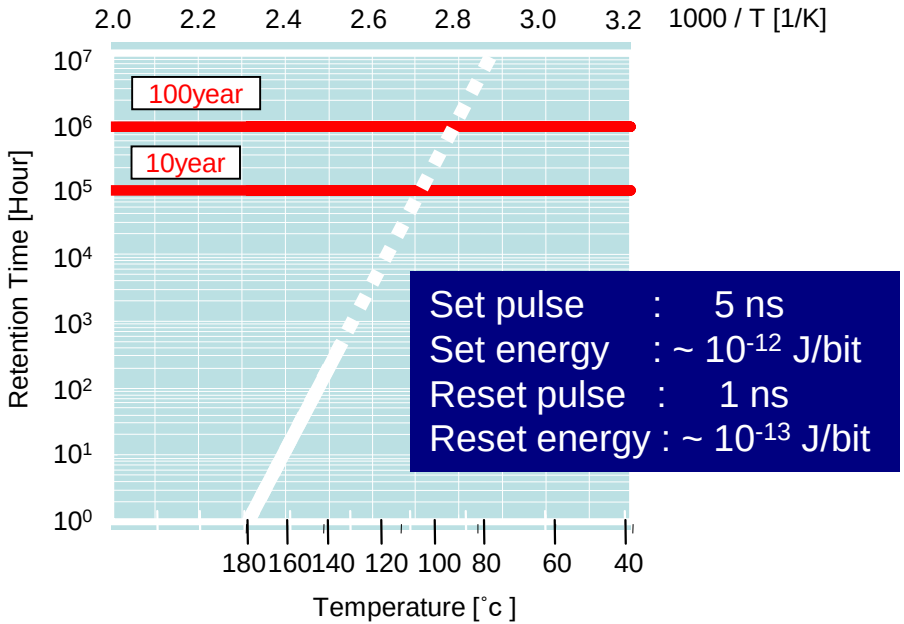
	Active cell area	40 nmΦ
Set	Set pulse width	**5 ns**
	Set current	110 µA
	Set voltage	+3 V
Reset	Reset pulse width	**1 ns**
	Reset current	125 µA
	Reset voltage	–1.7 V

K. Aratani, “A Novel Resistance Memory with High Scalability and Nanosecond Switching” IEDM 2007

Set / Reset cycle test

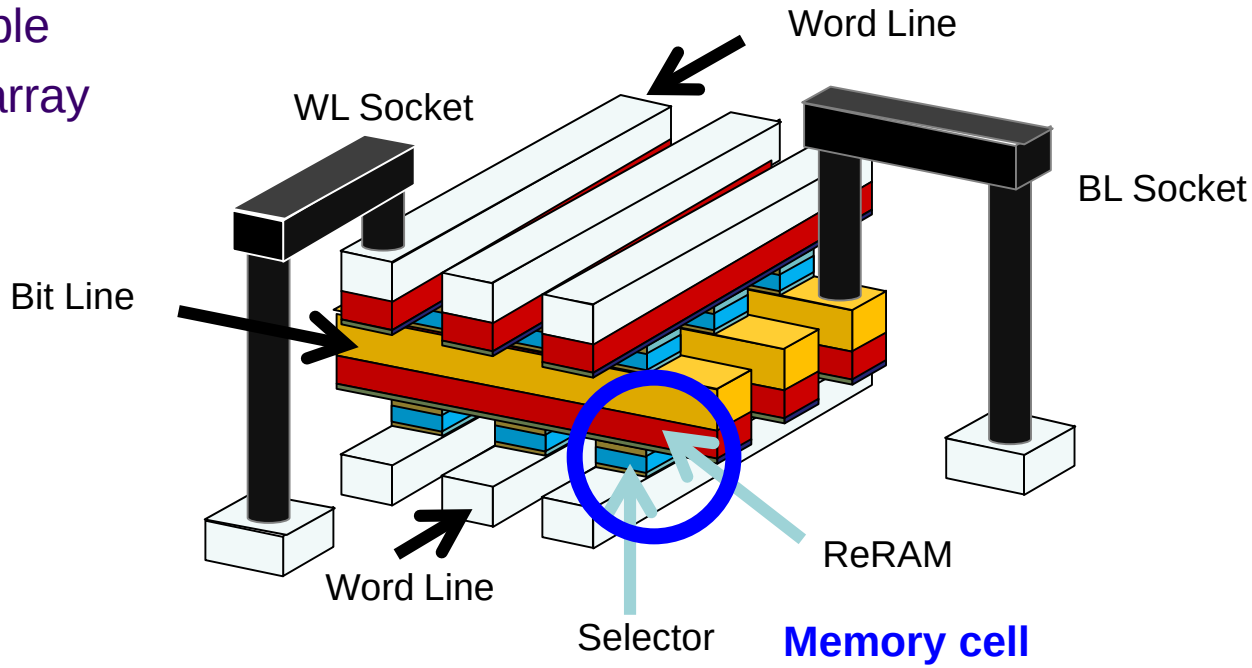


Retention test



(XP) Cross Point ReRAM

- Cell dimension $4F^2$
- Multiple decks feasible
- CMOS underneath array

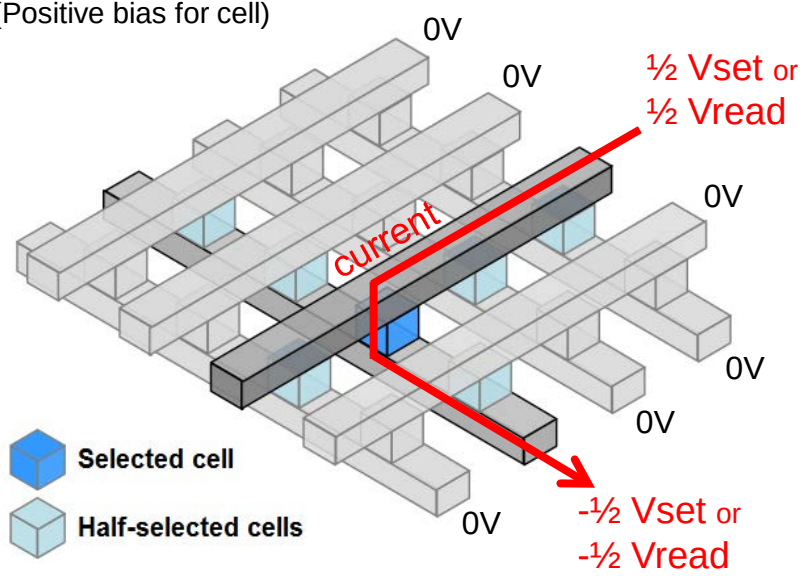


Cross Point Array Bipolar Operation

- Positive bias for Set and Read, negative bias for Reset
- Half-selected cells (½ Vset or ½ Vreset) SHOULD NOT turn on. This limitation is from XP architecture.

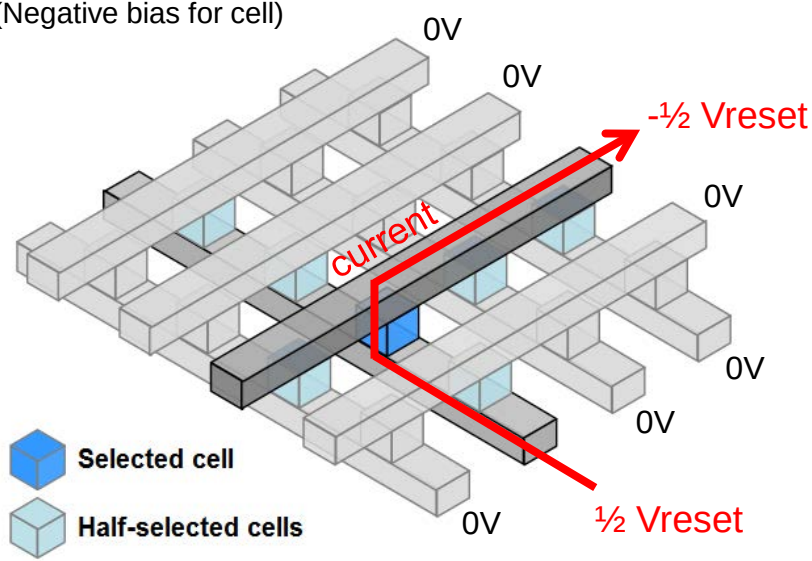
Set and Read

(Positive bias for cell)



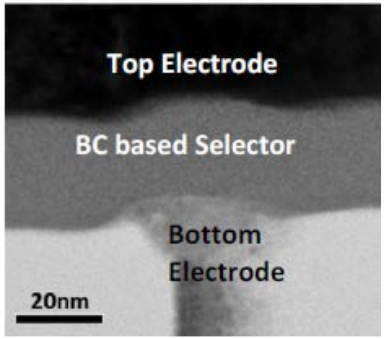
Reset

(Negative bias for cell)



Selector for Cross Point ReRAM

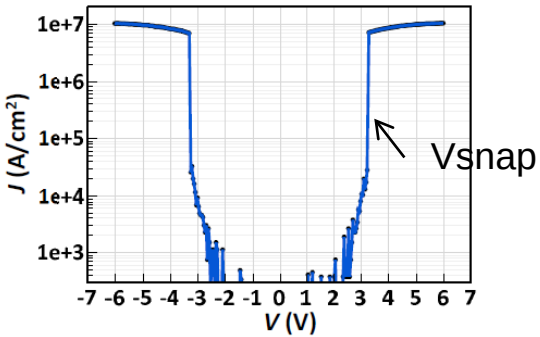
TEM cross section



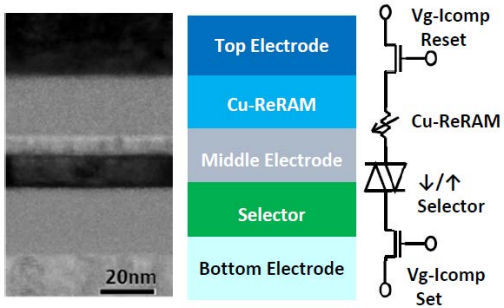
Two key technologies have been developed for 100Gb-class Persistent Memory,,,,,

S. Yasuda, “A Cross Point Cu-ReRAM with a Novel OTS Selector” VLSI Symposium 2017

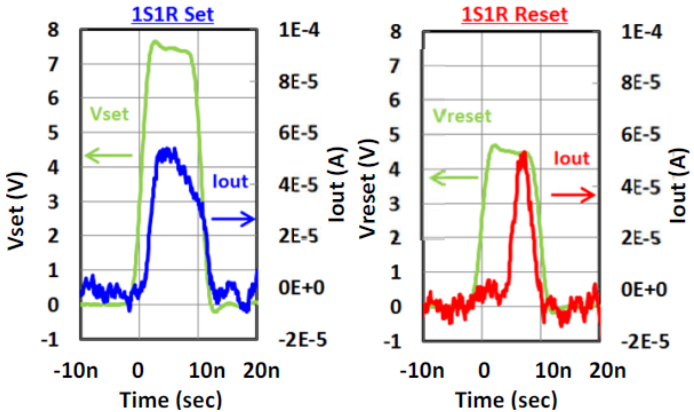
Pulsed JV curve



Cross section



Transient Analysis



1S1R device can Set/Reset in 10ns.

Possible Performance

XP ReRAM

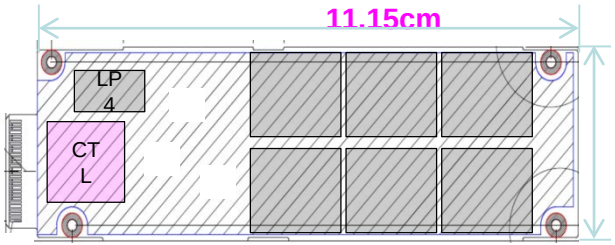
Item	Target
R/W sector size	512B
Read Throughput	3.2GB/s
Read Latency	0.4us
Write Throughput	1.2GB/s
Write Latency	2us

XP ReRAM + Controller

Item	Target
R/W sector size	512B
Read Throughput	3.2GB/s
Read Latency	1.4us
Write Throughput	1.2GB/s
Write Latency	2.4us

Item	8chip Target	16chip Target
R/W size	4kB	8kB
Read Throughput	25.6GB/s	51.2GB/s
Read Latency	1.4us	1.4us
Write Throughput	9.6GB/s	19.2GB/s
Write Latency	2.4us	2.4us

Example : Power Barrier for Small Form Factor



Item	8chip Target	16chip Target
R/W size	4kB	8kB
Read Throughput	25.6GB/s	51.2GB/s
Read Latency	1.4us	1.4us
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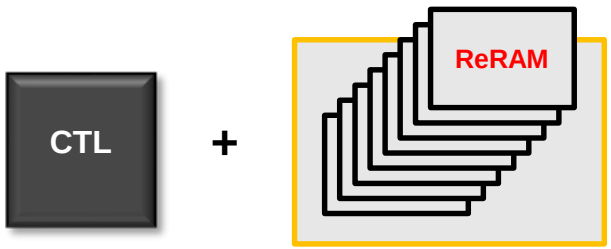
Write Latency	2.4us	2.4us
	PCIe Gen5 x8	***PCIe Gen5 x16***

If CTL > 5W and ReRAM > 1.2W, Total in 8chip >14.6W
If CTL > 8W and ReRAM > 1.2W, Total in 16chip >27.2W



ReRAM power is less than PCM, but bigger than DRAM
Need to reduce power of ReRAM and controller
Care for thermal budget of small form factor

Summary

- XP ReRAM is expected to high performance application such as Persistent Memory
- The power consumption must be considered for small form factor application
- The dedicated controller design is also needed to reduce the total power