CXL: Expanding the Memory Ecosystem

A Panel Discussion Moderated by
Tom Coughlin, President, Coughlin Associates
How To Participate

• Ask questions via the Q&A button on the bottom of the zoom window
• You can see other attendees’ questions, so upvote for your favorites to be answered during the session
• We’ll try to get to as many questions as possible
• Connect with the panelists via Slack channels during the event
• And look for our post-Summit Evaluation Survey
Abstract

- CXL is an open industry standard that provides high bandwidth low latency interconnection. This panel will discuss how CXL works and how it changes the use of memory, accelerators and memory management as well as use cases, availability and how to get involved.
Panelists

• Stephen Bates, Chief Technology Officer, Eideticom
• Chris Petersen, Hardware Systems Technologist, Facebook
• Andy Rudoff, Persistent Memory Software Architect, Intel Corporation
• Leah Schoeb, Sr. Developer Relations Manager, AMD
• David Wang, Director, Memory Product Planning, Samsung Semiconductor
• Hao Zhong, CEO, ScaleFlux
Where To Find Out More About Compute, Memory, & Storage

Website Resources
snia.org/CMSI

Twitter
@SNIACoMputeMemoryStorage

SNIA CMSI Blog
sniacmsiblog.org

Videos
youtube.com/SNIAVideo

Educational Materials
snia.org/educational-library

Join SNIA and the Compute, Memory, and Storage Initiative
snia.org/join

CMSI Engages and Educates

CMSI Accelerates Standards

CMSI Propels Technology Adoption
CXL Delivers the Right Features & Architecture

Challenges

- Industry trends driving demand for faster data processing and next-gen data center performance
- Increasing demand for heterogeneous computing and server disaggregation
- Need for increased memory capacity and bandwidth
- Lack of open industry standard to address next-gen interconnect challenges

CXL
An open industry-supported cache-coherent interconnect for processors, memory expansion and accelerators

Coherent Interface
Leverages PCIe with 3 mix-and-match protocols

Low Latency
Cache and Memory targeted at near CPU cache coherent latency

Asymmetric Complexity
Eases burdens of cache coherent interface designs
Representative CXL Usages

Caching Devices / Accelerators

- TYPE 1
  - DDR
  - Processor
  - CXL
    - CXL.io
    - CXL.cache
  - Accelerator
    - NC
    - Cache

- USAGES
  - PGAS NIC
  - NIC atomics

Accelerators with Memory

- TYPE 2
  - DDR
  - Processor
  - CXL
    - CXL.io
    - CXL.cache
    - CXL.memory
  - Accelerator
    - Cache

- USAGES
  - GP GPU
  - Dense computation

Memory Buffers

- TYPE 3
  - DDR
  - Processor
  - CXL
    - CXL.io
    - CXL.memory
  - Memory Buffer
    - Cache

- USAGES
  - Memory BW expansion
  - Memory capacity expansion
  - Storage class memory
Storage/Memory Hierarchy Gap

CXL Helps Narrow the Storage and Memory Gaps – Both In Capacity and Performance
In Summary

CXL Consortium momentum continues to grow

• 130+ members and growing
• Celebrating first anniversary of incorporation – second generation specification
• Responding to industry needs and challenges

Call to action

• Join CXL Consortium
• Follow us on Twitter and LinkedIn for more updates!