SNIA PERSISTENT MEMORY + SUMMIT 2021 COMPUTATIONAL STORAGE

FROM DATACENTER TO EDGE : VIRTUAL EVENT
APRIL 21-22, 2021

Compute Express Link™ (CXL™) 2.0 – Architecture and Benefits for Computational Storage

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Industry Landscape

Proliferation of Cloud Computing

Growth of AI & Analytics

Cloudification of the Network & Edge

CXL Consortium

CXL Board of Directors

Alibaba Group
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IBM
intel
MICROCHIP
Microsoft
XILINX

Open Industry Standard for Cache Coherent Interconnect

150+ Member Companies

CXL Delivers the Right Features & Architecture

Challenges

Industry trends driving demand for faster data processing and next-gen data center performance

Increasing demand for heterogeneous computing and server disaggregation

Need for increased memory capacity and bandwidth

Standards-based interconnect with configuration flexibility for memory, storage, or accelerators

CXL

An open industry-supported cache-coherent interconnect for processors, memory expansion and accelerators

Coherent Interface

Leverages PCIe with 3 mix-and-match protocols

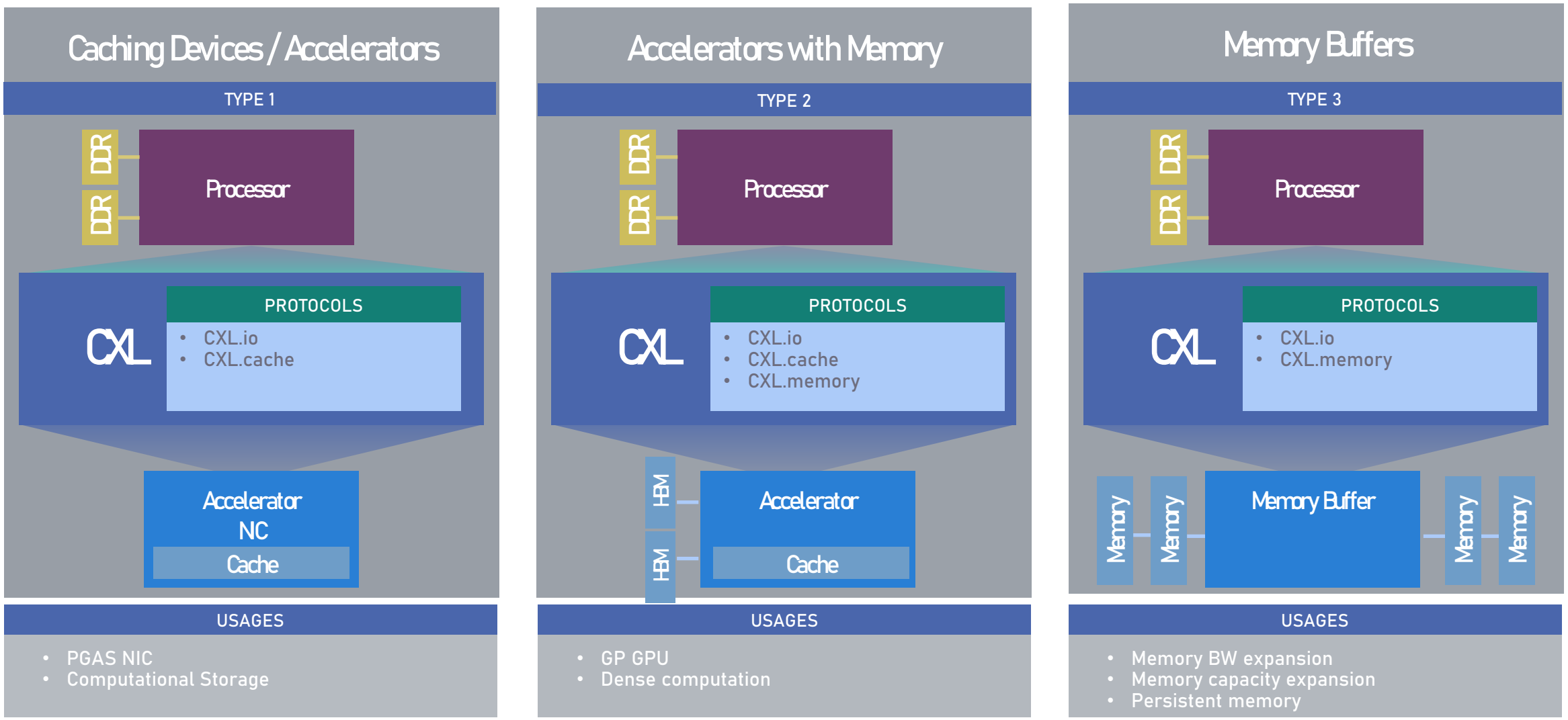
Low Latency

.Cache and .Memory targeted at near CPU cache coherent latency

Asymmetric Complexity

Eases burdens of cache coherent interface designs

Representative CXL Usages



CXL and Computational Storage

<table>
<tr><td colspan="2" rowspan="4">CXL
Cache
Mem
Flit</td><td colspan="66">Flit Byte #</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td><td>48</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td><td>64</td><td>65</td></tr>
<tr><td colspan="16">Slot Byte #</td><td colspan="16">Slot Byte #</td><td colspan="16">Slot Byte #</td><td colspan="16">Slot Byte #</td><td colspan="2"></td></tr>
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<tr><td rowspan="8">Bit #</td><td>0</td><td colspan="16" rowspan="8">Data Chunk</td><td colspan="16" rowspan="8">Data Chunk</td><td colspan="16" rowspan="8">Data Chunk</td><td colspan="16" rowspan="8">Data Chunk</td><td colspan="2" rowspan="8">CRC</td></tr>
<tr><td>1</td></tr>
<tr><td>2</td></tr>
<tr><td>3</td></tr>
<tr><td>4</td></tr>
<tr><td>5</td></tr>
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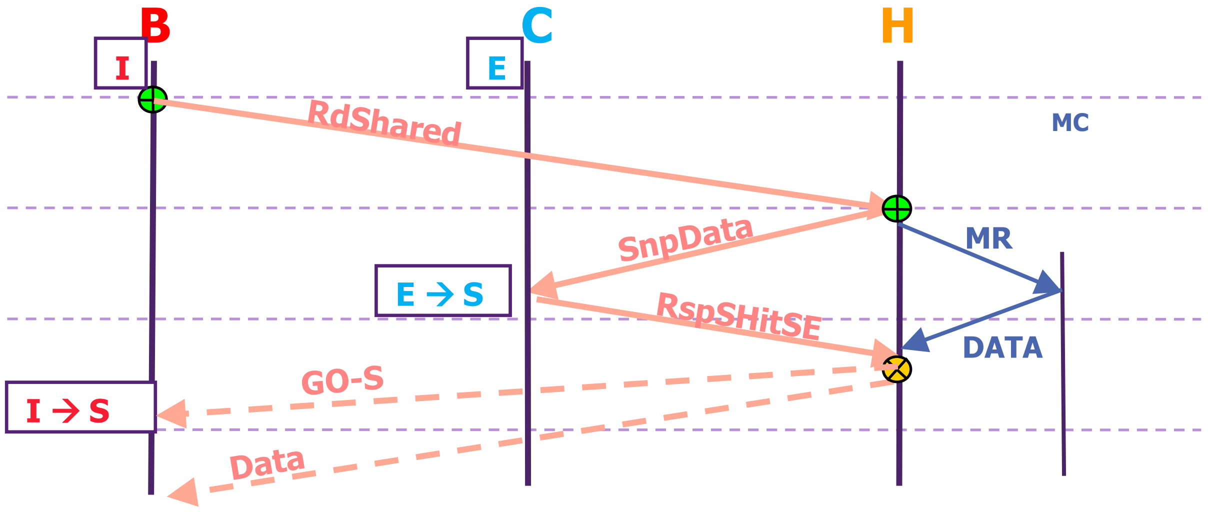
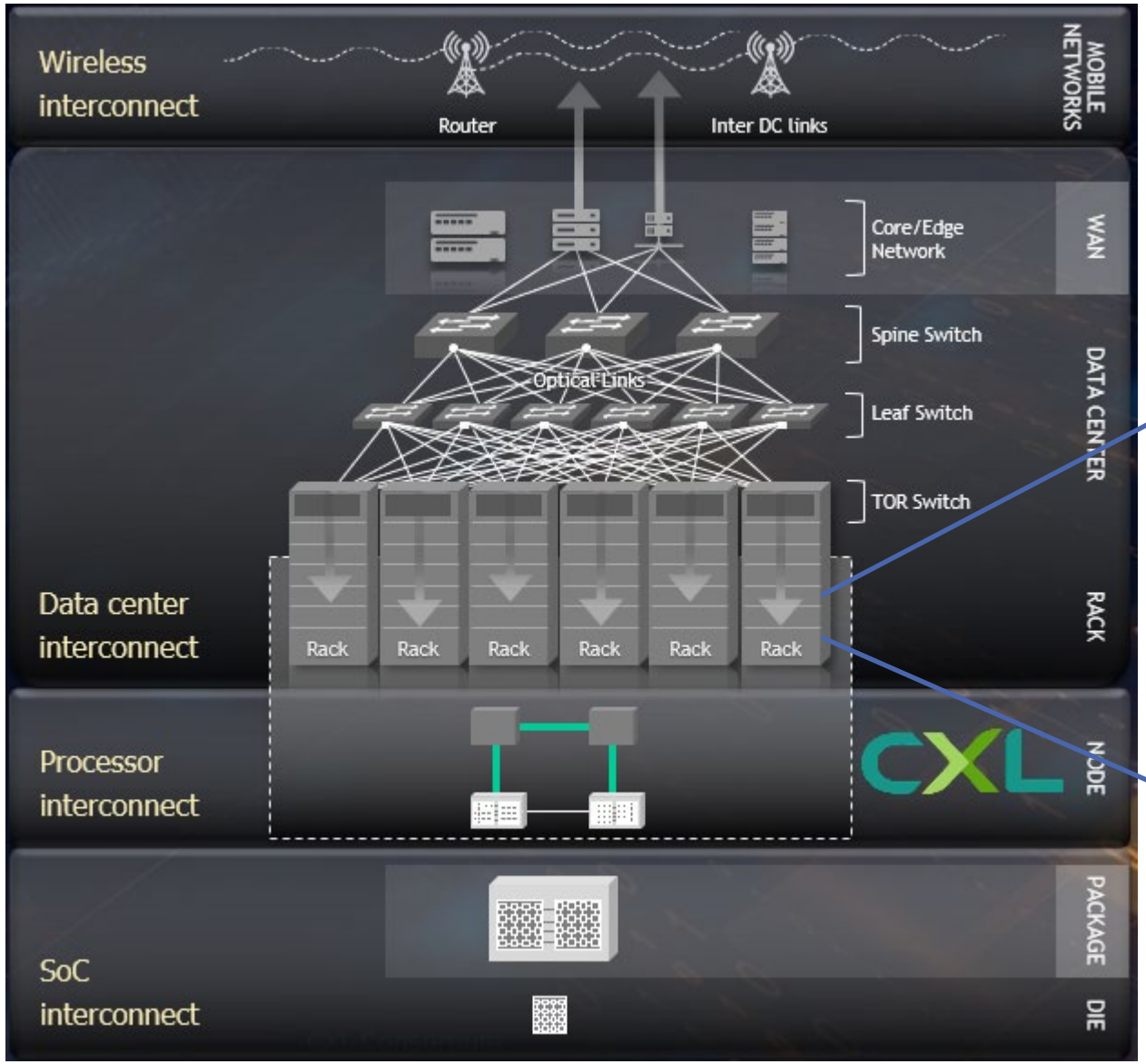
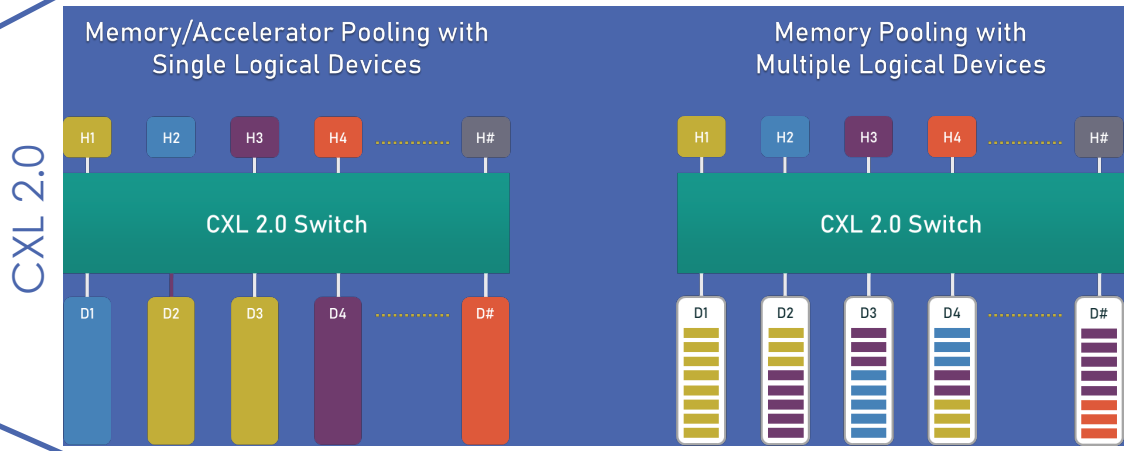
- Efficient (512b data + CRC) FLIT-based data movement



- Host managed asymmetric coherence

Data Center: Looking Outside in: Scope of CXL 2.0 over CXL 1.1





CXL 2.0 across Multiple Nodes inside a Rack/Chassis supporting pooling of resources

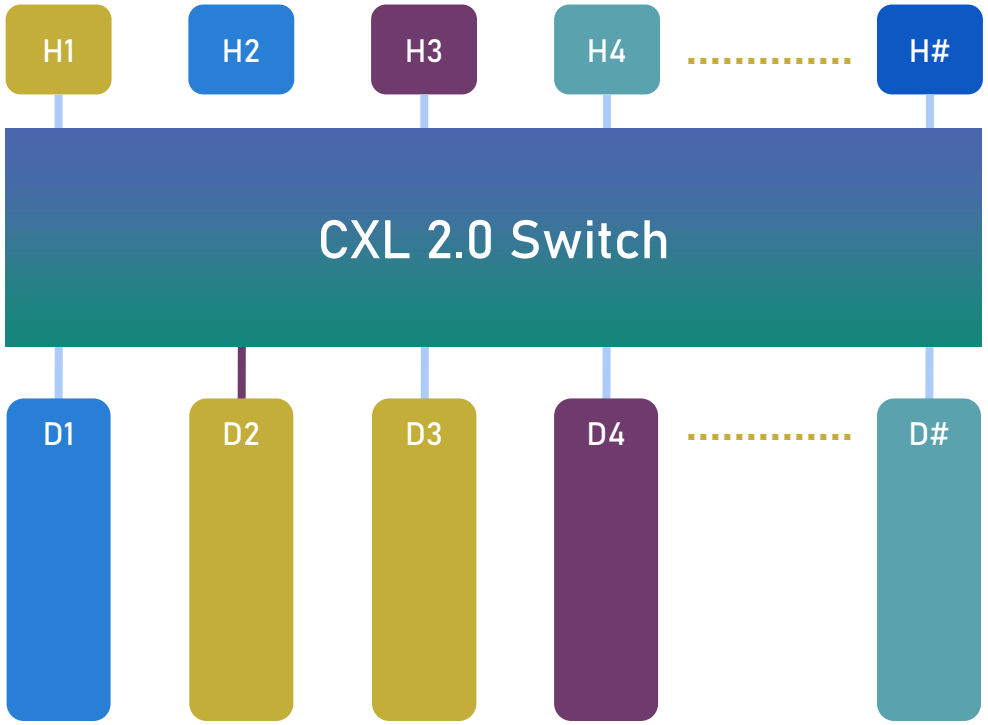
CXL 2.0 Scope: Hot-Plug, Persistence, Switching, and Dis-aggregation

Feature	Description
CXL PCIe End-Point	CXL device to be discovered as PCIe Endpoint Support of CXL 1.1 devices directly connected to Root-Port or Downstream Switch Port
Switching	Single level of switching with multiple Virtual Hierarchies (cascaded possible in a single hierarchy) CXL Memory Fan-Out & Pooling with Interleaving CXL.Cache is direct routed between CPU and device with a single caching device within a hierarchy. Downstream port must be capable of being PCIe.
Resource Pooling	Memory Pooling for Type3 device – Multiple Logical Device (MLD), a single device to be pooled across 16 Virtual Hierarchies.
CXL.cache and CXL.mem enhancements	Persistence (Global Persistence Flush), Managed Hot-Plug, Function Level Reset Scope Clarification, Enhanced FLR for CXL Cache/Mem, Memory Error Reporting and QoS Telemetry
Security	Authentication and Encryption – CXL.IO uses PCIe IDE, CXL defines similar capability for CXL.$Mem
Software Infrastructure/ API	ACPI & UEFI ECNs to cover notification and management of CXL Ports and devices CXL Switch API for a multi-host or memory pooled CXL switch configuration and management

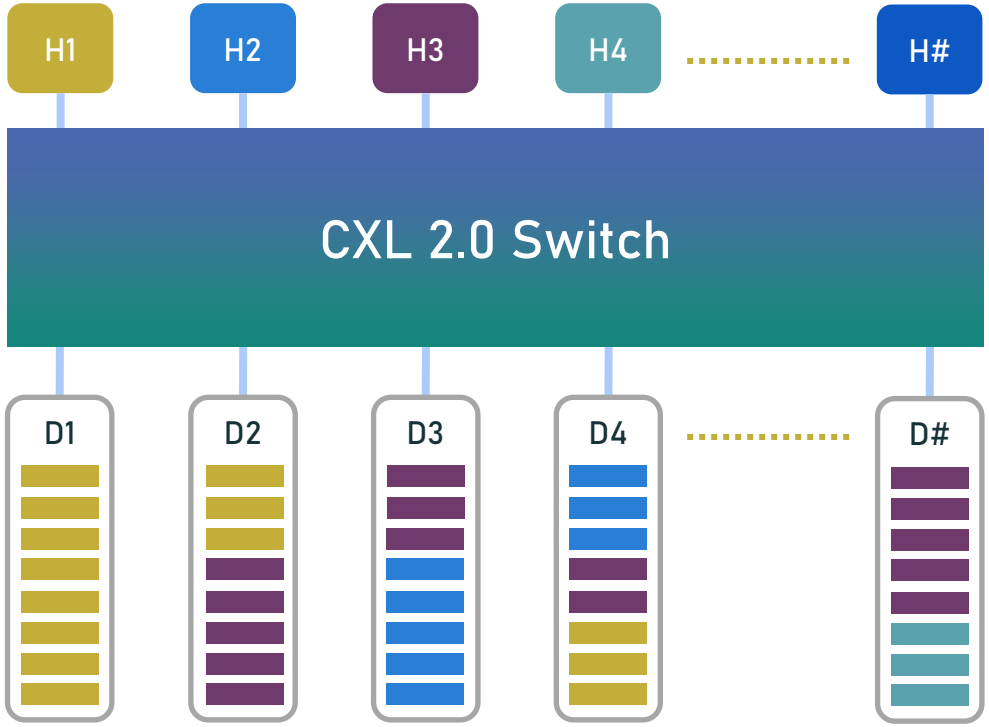
CXL 2.0 is fully backwards compatible with CXL 1.0/1.1
CXL 2.0 spec Rev 0.7 in Q1, 2020; Rev 0.9 in Q2, 2020, and CXL 2.0 in Q3, 2020
Predictable spec release cadence by CXL consortium to help the ecosystem plan better.

Benefits of CXL 2.0 Switching Pooling

Memory/Accelerator Pooling with Single Logical Devices



Memory Pooling with Multiple Logical Devices

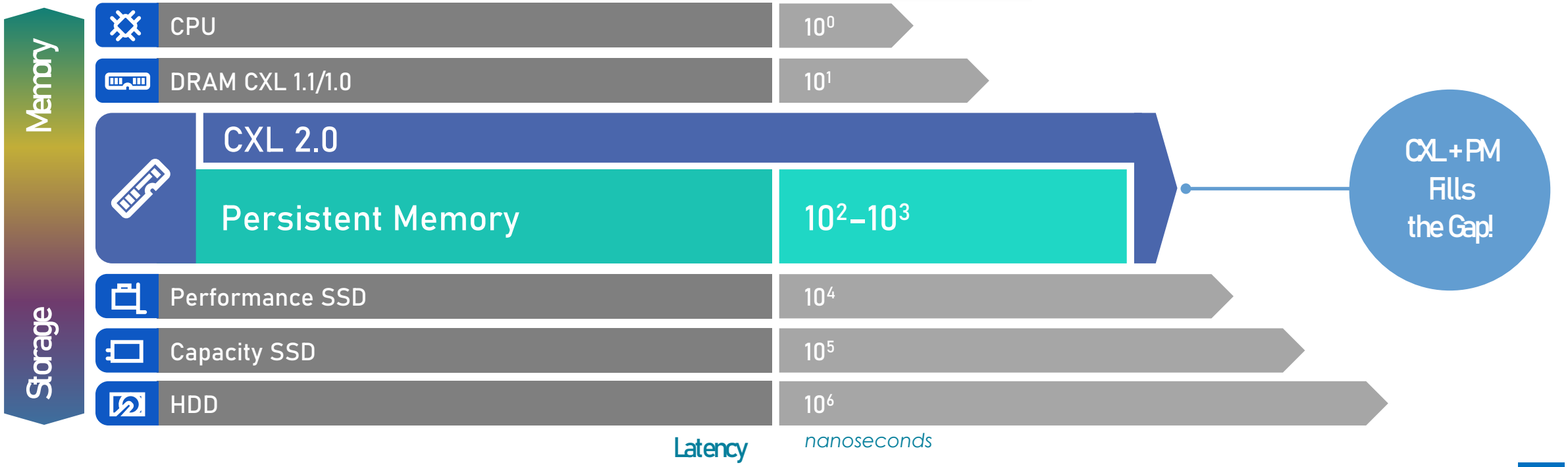


Benefits of CXL 2.0 and Persistent Memory

Moves Persistent Memory from Controller to CXL

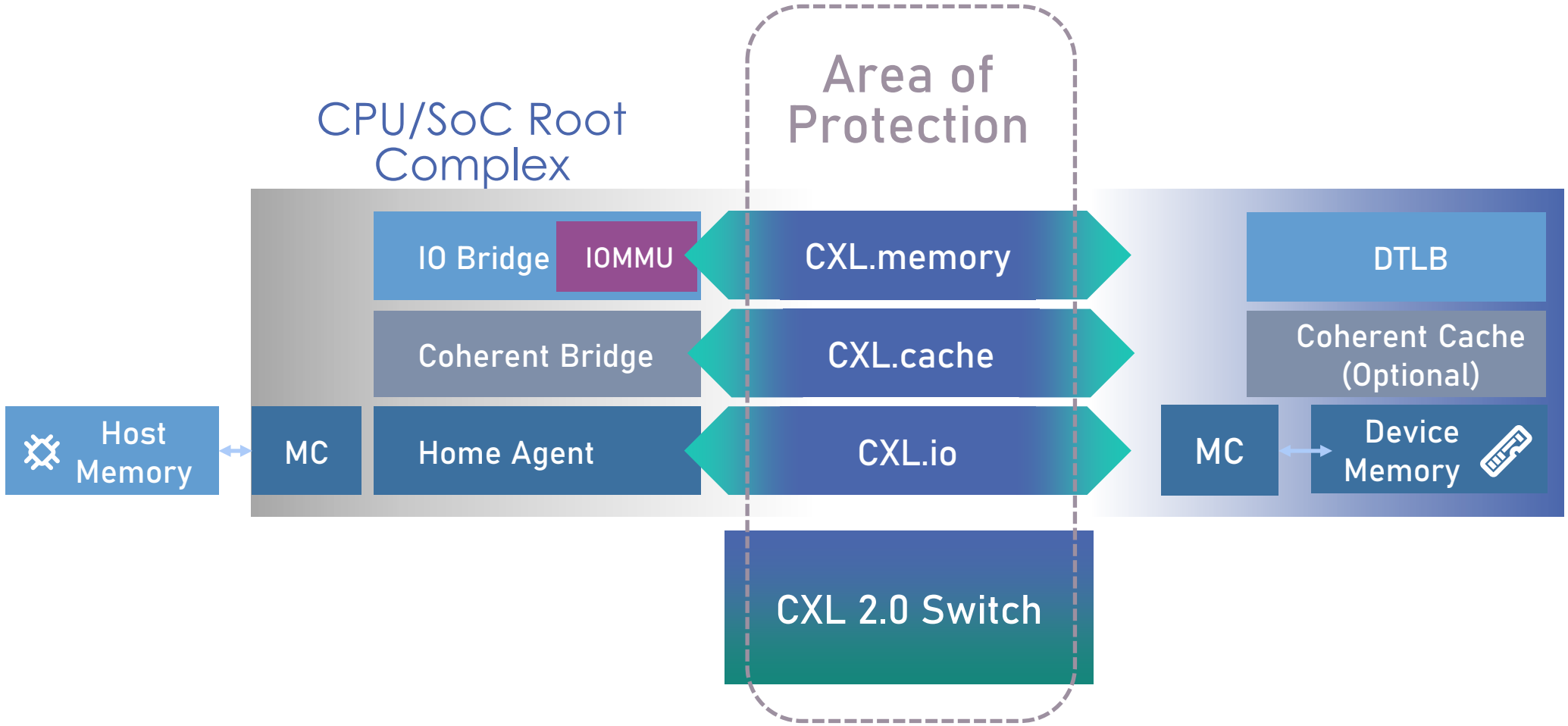
Enables Standardized Management of the Memory and Interface

Supports a Wide Variety of Industry Form Factors



CXL 2.0 Security Benefits

CXL 2.0 provides Integrity and Data Encryption of traffic across all entities (Root Complex, Switch, Device)



In Summary

CXL Consortium momentum continues to grow

- 150+ members and growing
- Responding to industry need and challenges
- Celebrating first anniversary of incorporation – second generation specification
- Responding to industry needs and challenges

CXL 2.0 introduces new features & usage models

- Switching, pooling, persistent memory support, security
- Fully backward compatible with CXL 1.1 and 1.0
- Built in Compliance & Interop program & Interop program

Call to action

- Join CXL Consortium
- Visit www.computeexpresslink.org for more information
- Follow us on Twitter and LinkedIn for more updates!

CXL Compute Express Link™

Thank you

Please visit www.snia.org/pm-summit for presentations