Compute Express Link™ (CXL™) 2.0 – Architecture and Benefits for Computational Storage

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Industry Landscape

- Proliferation of Cloud Computing
- Growth of AI & Analytics
- Cloudification of the Network & Edge
CXL Consortium

CXL Board of Directors

Open Industry Standard for Cache Coherent Interconnect

150+ Member Companies
CXL Delivers the Right Features & Architecture

Challenges

- Industry trends driving demand for faster data processing and next-gen data center performance
- Increasing demand for heterogeneous computing and server disaggregation
- Need for increased memory capacity and bandwidth
- Standards-based interconnect with configuration flexibility for memory, storage, or accelerators

CXL
An open industry-supported cache-coherent interconnect for processors, memory expansion and accelerators

Coherent Interface
- Leverages PCIe with 3 mix-and-match protocols

Low Latency
- Cache and Memory targeted at near CPU cache coherent latency

Asymmetric Complexity
- Eases burdens of cache coherent interface designs
Representative CXL Usages

Caching Devices / Accelerators

- Type 1
  - CXL.io
  - CXL.cache

- USAGES
  - PGAS NIC
  - Computational Storage

Accelerators with Memory

- Type 2
  - CXL.io
  - CXL.cache
  - CXL.memory

- USAGES
  - GP GPU
  - Dense computation

Memory Buffers

- Type 3
  - CXL.io
  - CXL.memory

- USAGES
  - Memory BW expansion
  - Memory capacity expansion
  - Persistent memory

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CXL and Computational Storage

- Efficient (512b data + CRC) FLIT-based data movement

- Host managed asymmetric coherence
CXL 2.0 across Multiple Nodes inside a Rack/Chassis supporting pooling of resources
### CXL 2.0 Scope: Hot-Plug, Persistence, Switching, and Dis-aggregation

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
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<tbody>
<tr>
<td>CXL PCIe End-Point</td>
<td>CXL device to be discovered as PCIe Endpoint Support of CXL 1.1 devices directly connected to Root-Port or Downstream Switch Port</td>
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<tr>
<td>Switching</td>
<td>Single level of switching with multiple Virtual Hierarchies (cascaded possible in a single hierarchy) CXL Memory Fan-Out &amp; Pooling with Interleaving</td>
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<td>CXL Cache is direct routed between CPU and device with a single caching device within a hierarchy. Downstream port must be capable of being PCIe.</td>
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<tr>
<td>Resource Pooling</td>
<td>Memory Pooling for Type 3 device – Multiple Logical Device (MLD), a single device to be pooled across 16 Virtual Hierarchies.</td>
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<td>CXL.cacheenhancements</td>
<td>Persistence (Global Persistence Flush), Managed Hot-Plug, Function Level Reset Scope Clarification, Enhanced FLR for CXL Cache/Mem, Memory Error Reporting and QoS Telemetry</td>
</tr>
<tr>
<td>Security</td>
<td>Authentication and Encryption – CXL.IO uses PCIe IDE, CXL defines similar capability for CXL.$Mem</td>
</tr>
<tr>
<td>Software Infrastructure/API</td>
<td>ACPI &amp; UEFI ECNs to cover notification and management of CXL Ports and devices CXL Switch API for a multi-host or memory pooled CXL switch configuration and management</td>
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</tbody>
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CXL 2.0 is fully backwards compatible with CXL 1.0/1.1
CXL 2.0 spec Rev 0.7 in Q1, 2020; Rev 0.9 in Q2, 2020, and CXL 2.0 in Q3, 2020
Predictable spec release cadence by CXL consortium to help the ecosystem plan better.
Benefits of CXL 2.0 Switching Pooling

Memory/Accelerator Pooling with Single Logical Devices

CXL 2.0 Switch

H1 H2 H3 H4 H#
D1 D2 D3 D4 D#

Memory Pooling with Multiple Logical Devices

CXL 2.0 Switch

H1 H2 H3 H4 H#
D1 D2 D3 D4 D#
Benefits of CXL 2.0 and Persistent Memory

Moves Persistent Memory from Controller to CXL

Enables Standardized Management of the Memory and Interface

Supports a Wide Variety of Industry Form Factors

CPU

DRAM CXL 1.1/1.0

CXL 2.0

Persistent Memory

Performance SSD

Capacity SSD

HDD

Latency

nanoseconds

Supports a Wide Variety of Industry Form Factors

CXL + PM Fills the Gap!

10^0

10^1

10^2–10^3

10^4

10^5

10^6
CXL 2.0 Security Benefits

CXL 2.0 provides Integrity and Data Encryption of traffic across all entities (Root Complex, Switch, Device)
In Summary

CXL Consortium
momentum continues to grow
• 150+ members and growing
• Responding to industry need and challenges
• Celebrating first anniversary of incorporation – second generation specification
• Responding to industry needs and challenges

CXL 2.0 introduces
new features & usage models
• Switching, pooling, persistent memory support, security
• Fully backward compatible with CXL 1.1 and 1.0
• Built in Compliance & Interop program & Interop program

Call to action
• Join CXL Consortium
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Thank you

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