CXL & UCIe

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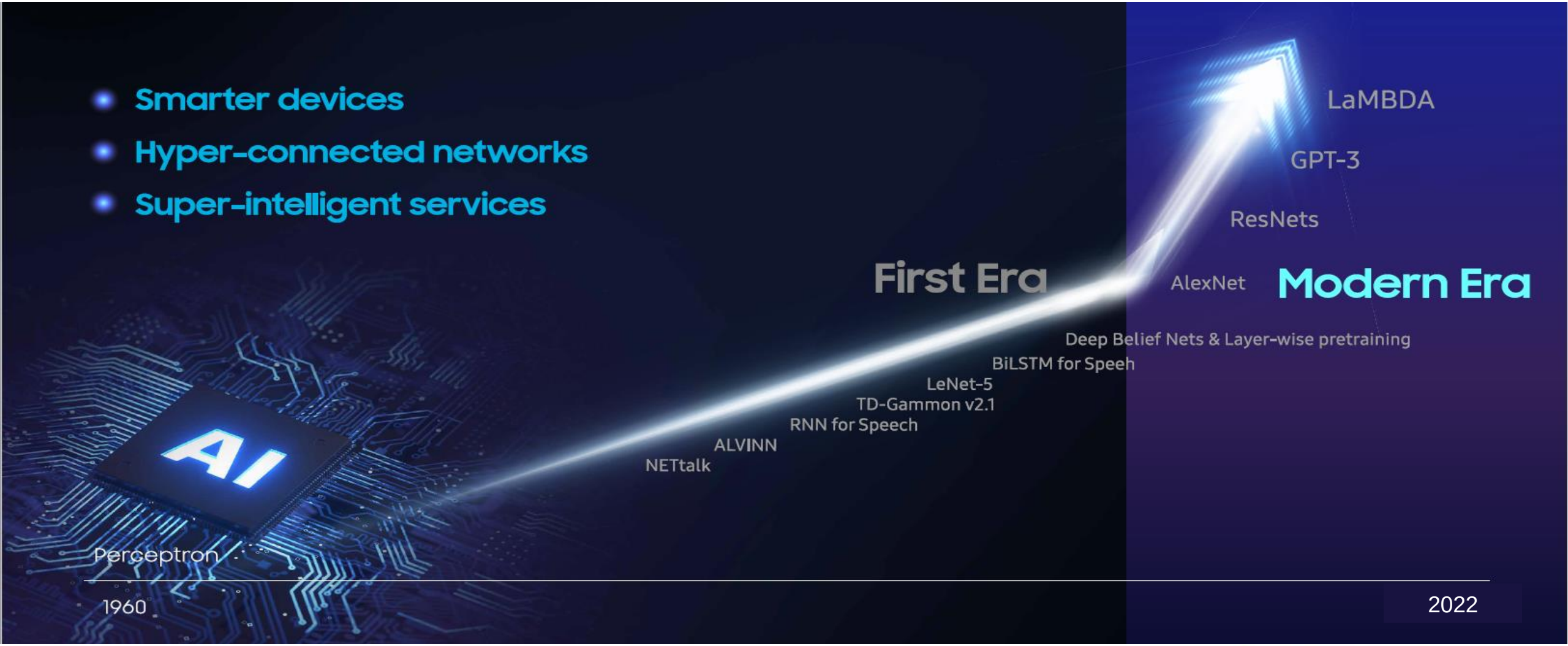
Vice President, New Business Planning Team, Samsung Electronics

Compute Express Link

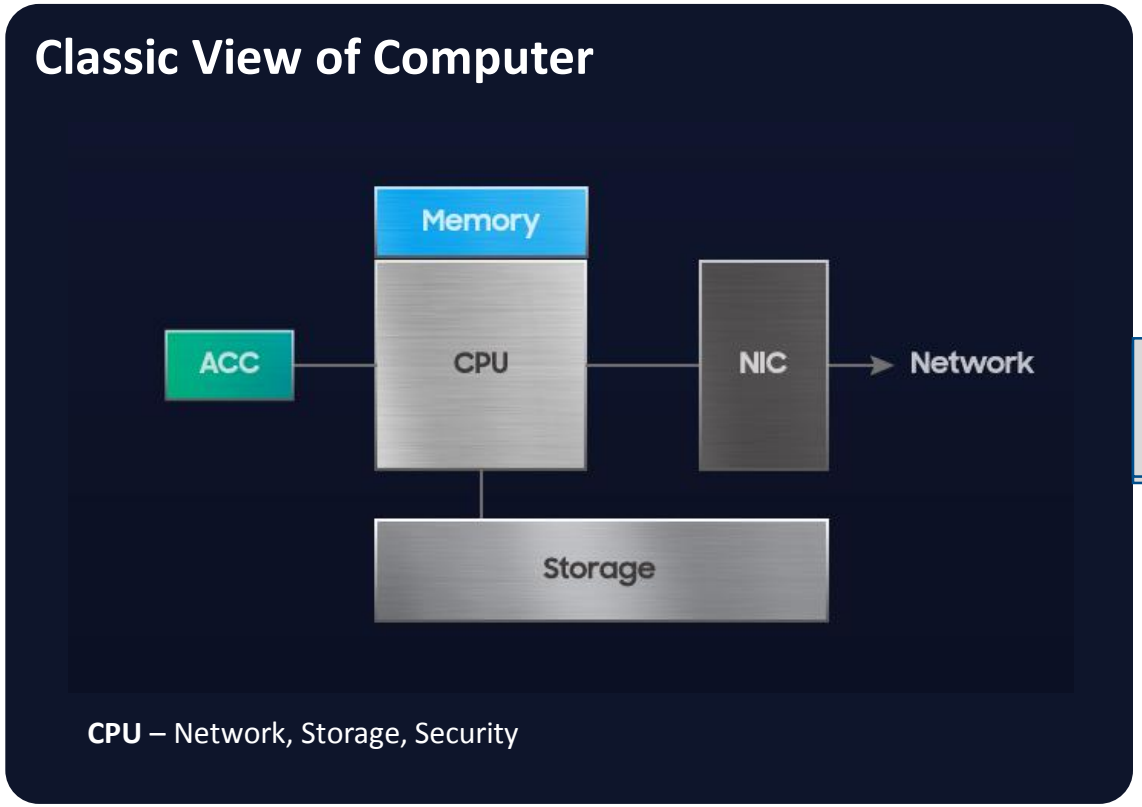
Driving the era of heterogeneous computing

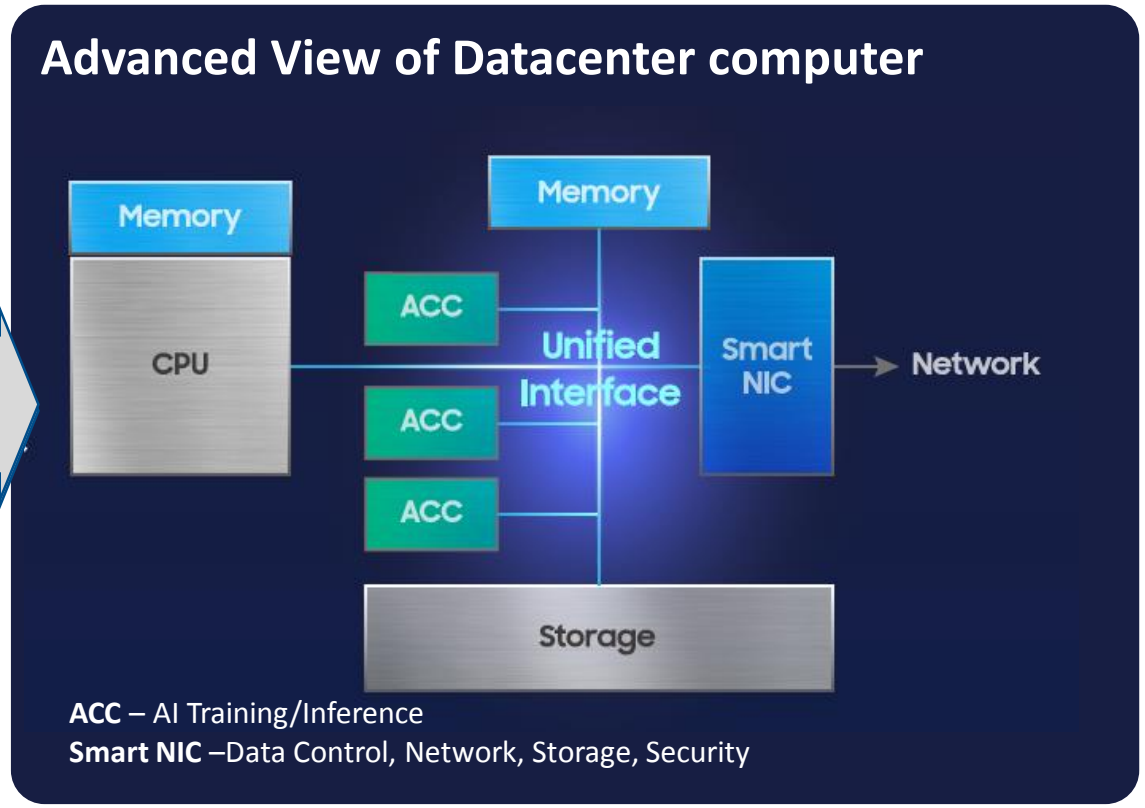
The Fast Growing Workloads of AI



System Architecture Changed by AI

From CPU centric to Heterogeneous Computing





The Rising Need for Better Connectivity

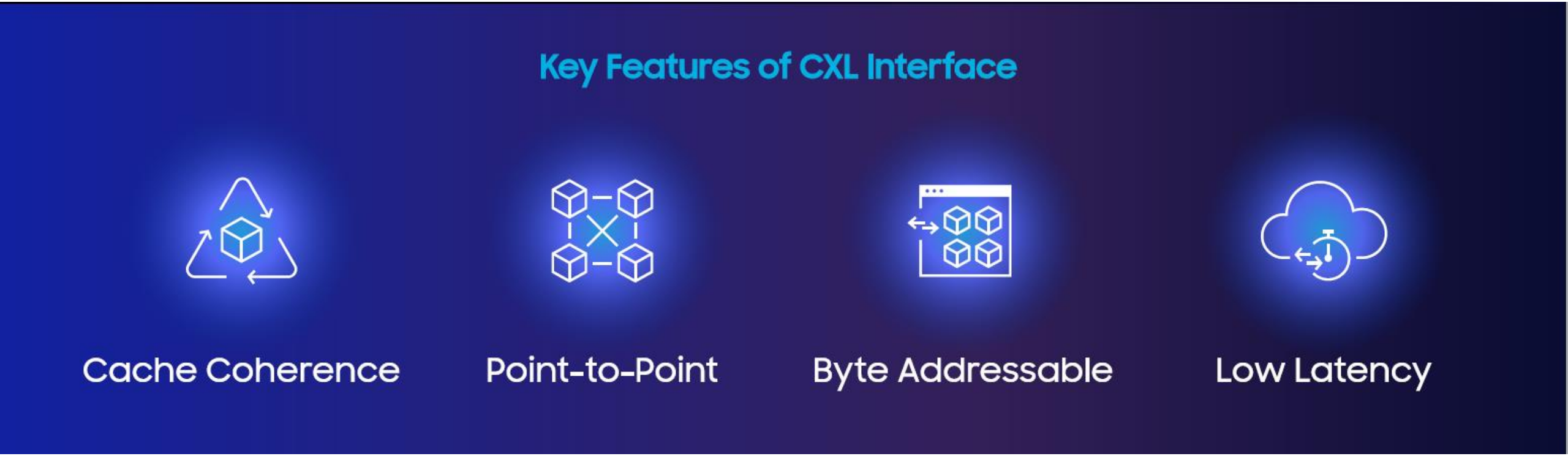
SoC Interconnect

Processor Interconnect

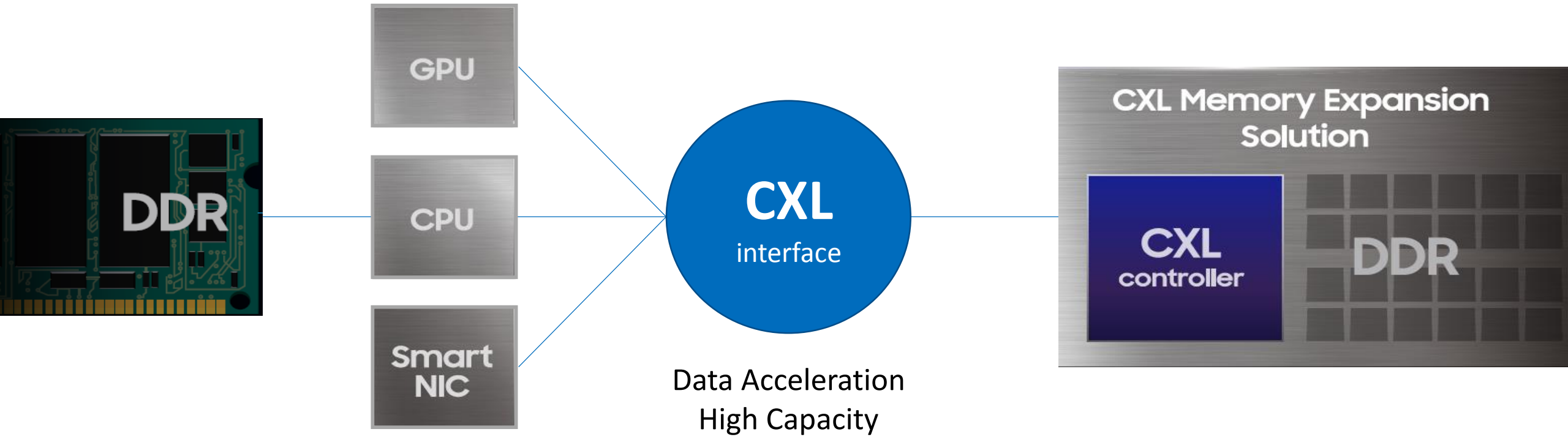
Data Center Interconnect

Customer Interconnect

CXL interface as Solution for the Era of AI



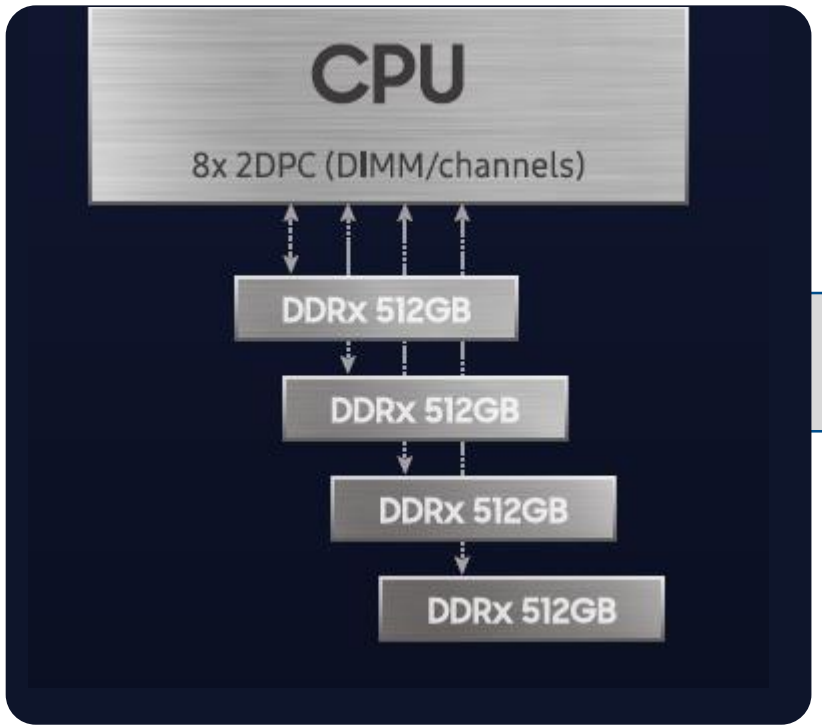
CXL Memory Expansion Solution



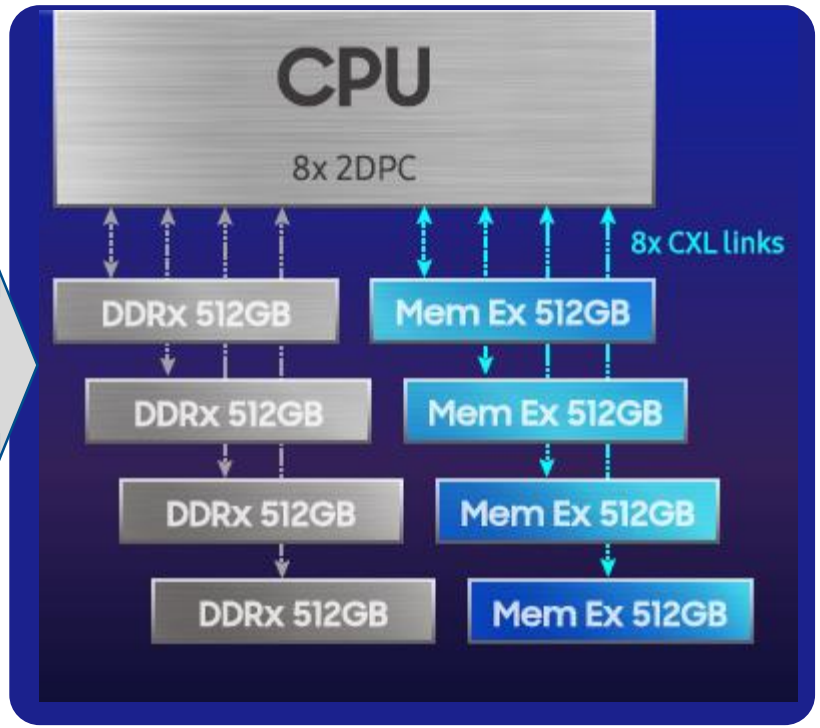
Data Acceleration
High Capacity
Enhanced Security/RAS

CXL Memory Expansion Solution

Max. 8TB for 1 CPU



Max. 16TB for 1 CPU



World's First CXL™ Memory Expander

SNIA PERSISTENT MEMORY + SUMMIT 2022 COMPUTATIONAL STORAGE

CXL Memory Expansion Solution

Increasing System Memory Capacity

Widening Memory Bandwidth

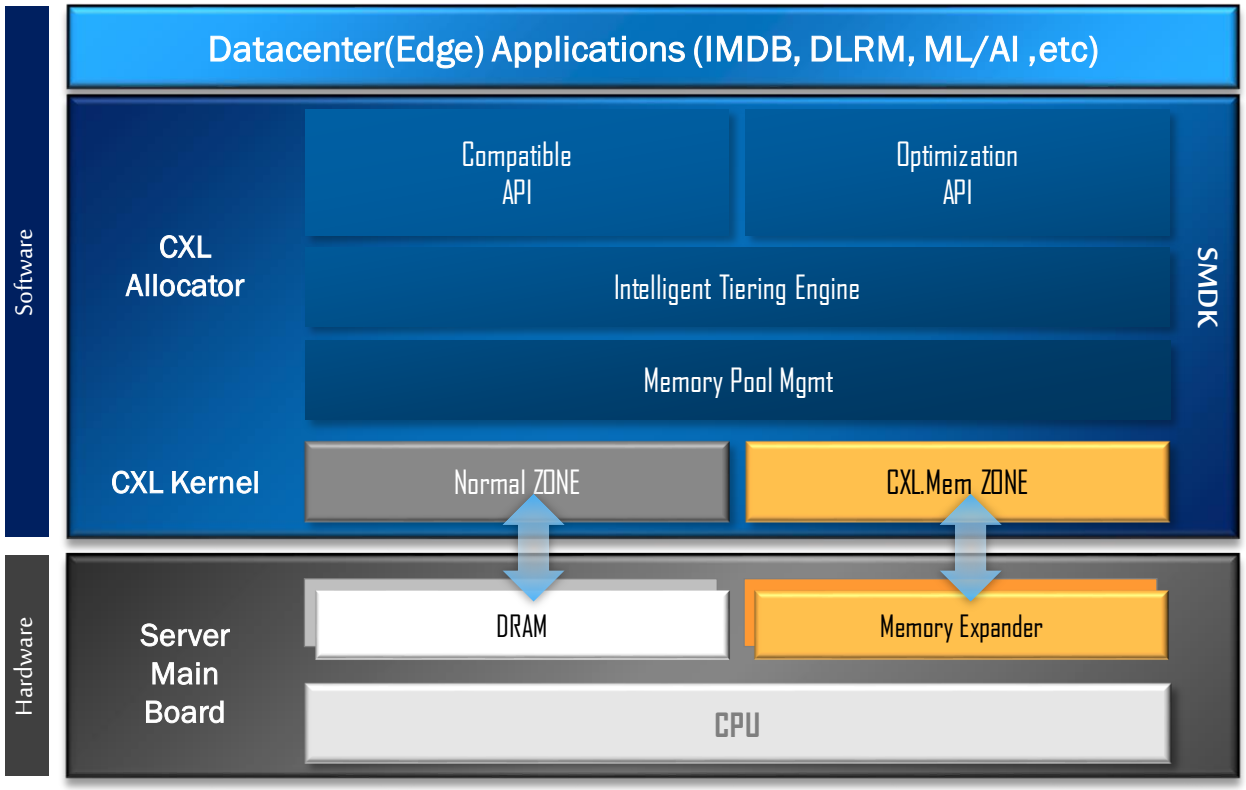
Supporting RAS/Security based on Memory Controller

World's First CXL™ Memory Expander

SMDK, Unified Interface for Memory Systems

Scalable Memory Development Kit (SMDK)

Memory development kit optimized for heterogeneous memory systems



Easy–to-integrate

No modifications needed

Intelligent Tiering

Supports tiering priorities,
Aggregate and limit capacity and bandwidth

Accelerate Data Service

BW+Capacity Expansion

Open Source

Early Access to CXL memory

Universal Chiplet Interconnect Express

Building an open ecosystem of chiplets for on-package innovations

Moore Predicted "Day of Reckoning"

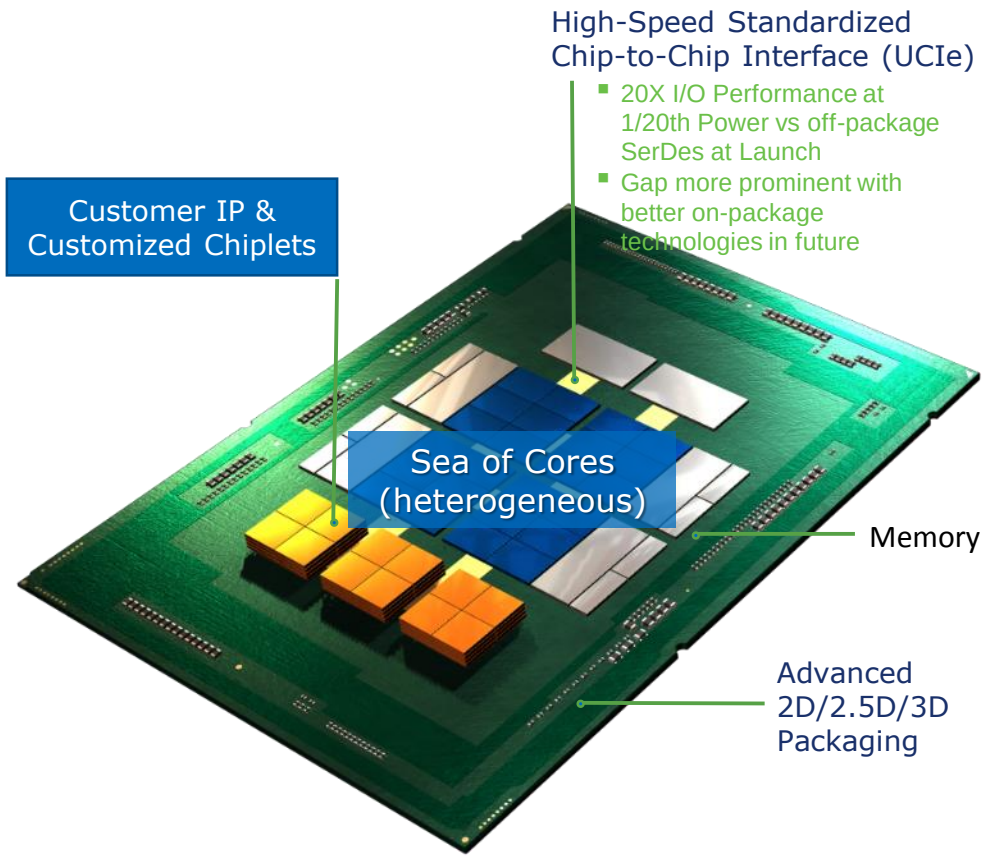
*"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."**

- Gordon E. Moore

* "Cramming more components onto integrated circuits," Electronics, Volume 38, Number 8, April 19, 1965

Motivation

OPEN CHIPLET: PLATFORM ON A PACKAGE



Heterogeneous Integration Fueled by an Open Chiplet Ecosystem
(Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing and process locked IPs)

Key Metrics and Adoption Criteria

UCIe - Architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria

Key Performance Indicators

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
  - Technology, frequency, & BER
- Reliability & Availability
- Cost
  - Standard vs advanced packaging

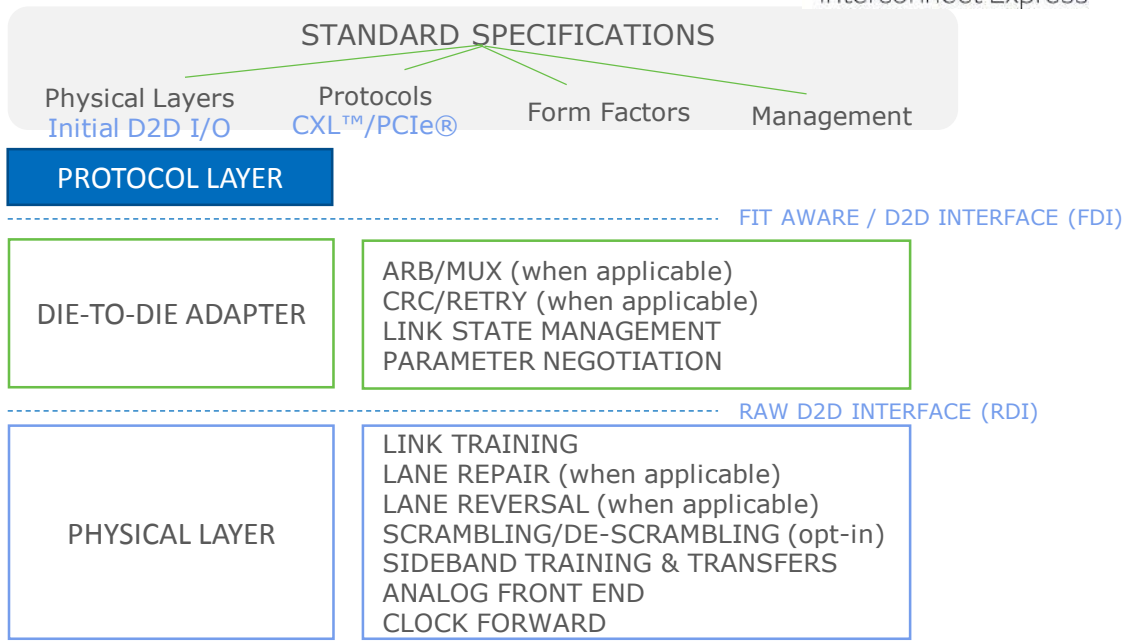
Factors Affecting Wide Adoption

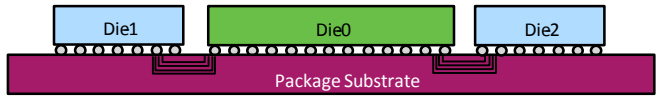
- Interoperability
  - Full-stack, plug-and-play with existing s/w is+
  - Different usages/segments
  - Technology
    - Across process nodes & packaging options
    - Power delivery & cooling
    - Repair strategy (failure/yield improvement)
    - Debug – controllability & observability
- Broad industry support / Open ecosystem
  - Learnings from other standards efforts

Jumpstarting UCIe

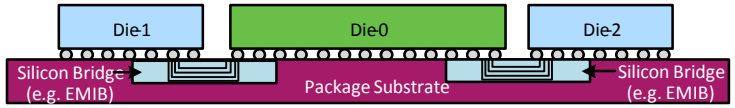
Intel donates initial specification

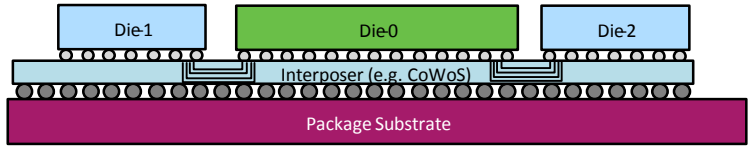
- **Focus of UCIe 1.0 Specification**
  - **Physical Layer:** Die-to-Die I/O with industry-leading KPIs
  - **Protocol:** CXL™/PCIe® for near term volume attach
    - SoC construction issues are addressed since CXL/PCIe is a board-to-board interface
    - CXL/PCIe addresses common use cases
      - I/O attach with PCIe/CXL.io
      - Memory use cases: CXL.mem
      - Accelerator use cases: CXL.cache
  - **Well defined specification**: ensure interoperability and future evolution
- **Future:** the chiplet journey is just starting!!
  - Other protocols
  - Advanced Chiplet form-factors (e.g., 3D)
  - Chiplet management
  - More to come ….

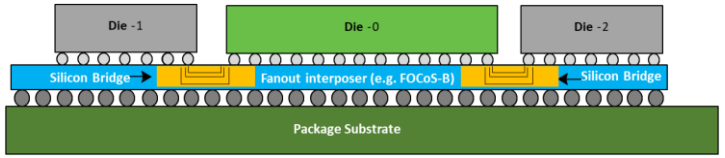




(Standard Package)



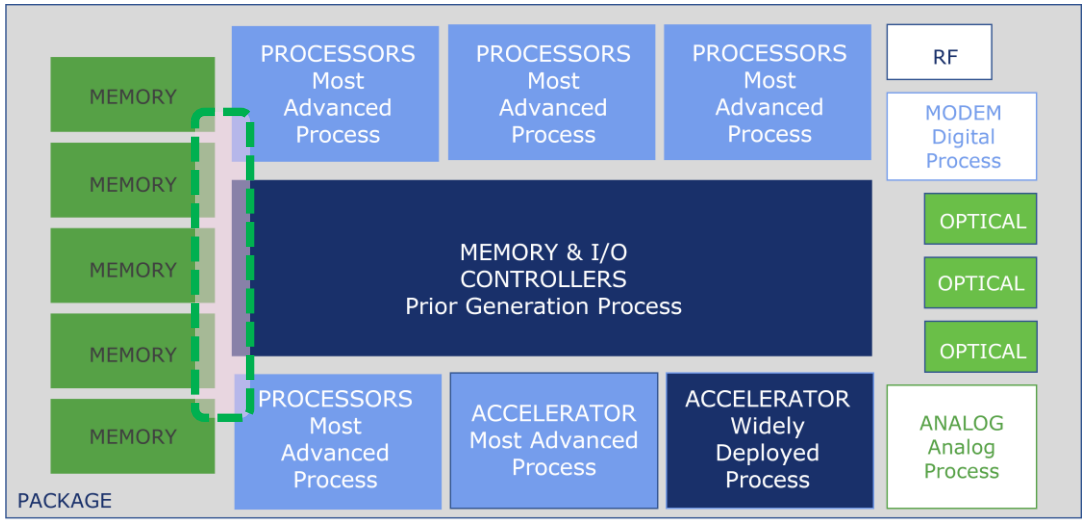




(Multiple Advanced Package Choices)

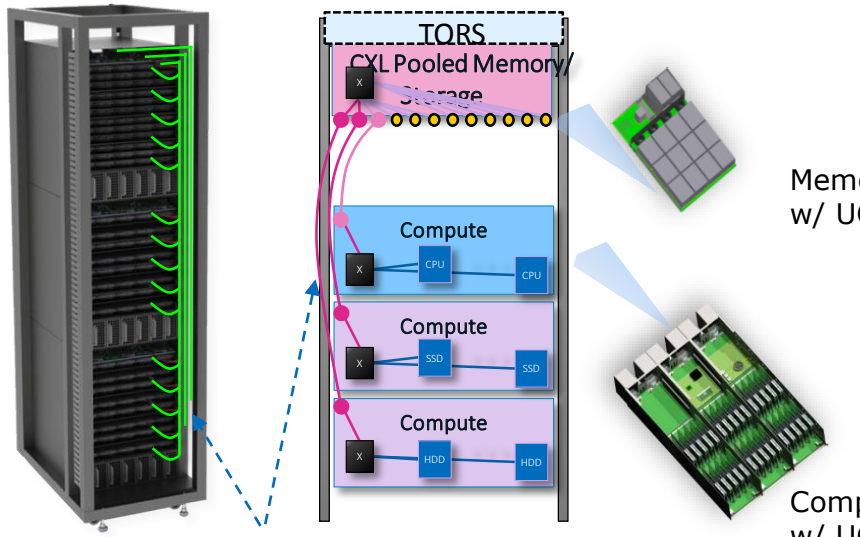
(Different flavors of packaging options supported to build an open ecosystem)

Usage Models Supported by UCIe



SoC Package level construction for wide range of usages from Hand-held to high-end servers

- ✓ Mix and match dies from multiple sources with different packaging options
- ✓ Plan to define chiplet DRAM Integration in UCIe



UCIe / CXL through UCIe Retimer

Provision to extend off-package with UCIe Retimers connecting to other media
(e.g., optics, electrical cable, mmWave)

UCIe
Universal Chiplet Interconnect Express

PROMOTERS

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive a new open chiplet ecosystem.

AMD
arm
ASE GROUP
Google Cloud
intel
Meta
Microsoft
Qualcomm
SAMSUNG
tsmc

Summary

- **Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers join forces** to launch new **Universal Chiplet Interconnect Express (UCIe)** technology to standardize the chiplet ecosystem today and future generations of chiplet technology.
- **UCIe 1.0 Specification** ratified to provide a complete standardized die-to-die interconnect with physical layer, protocol stack, software model, and compliance testing that will enable end users to easily mix and match chiplet components from a multi-vendor ecosystem for System-on-Chip (SoC) construction, including customized SoC.
- **New open standard establishes an open chiplet ecosystem and ubiquitous interconnect at the package level.**
- Interested companies and institutions are encouraged to join. **Learn more, including how to join:** www.UCIexpress.org