SDC
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Phase Change Memory and its positive influence on Flash Algorithms

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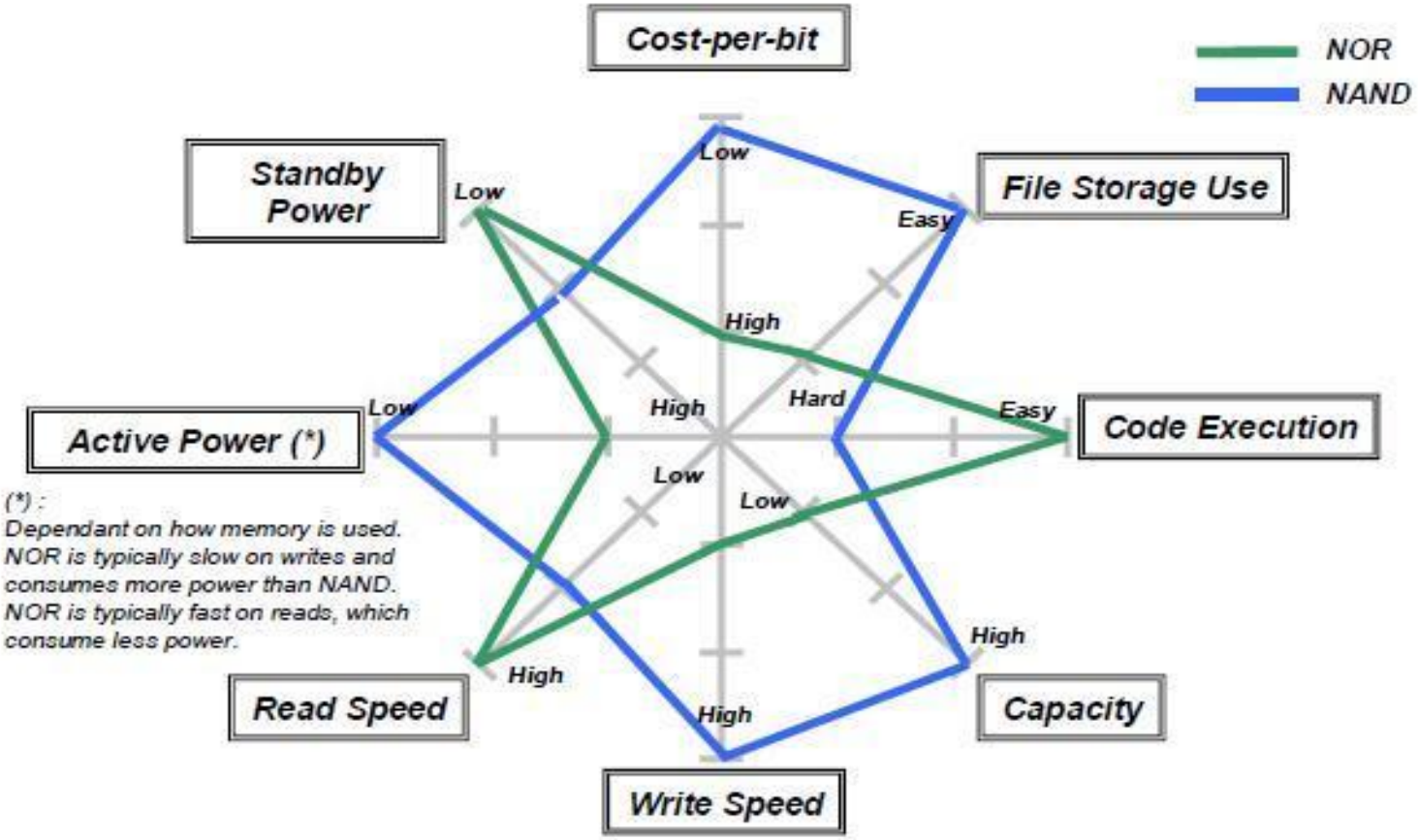
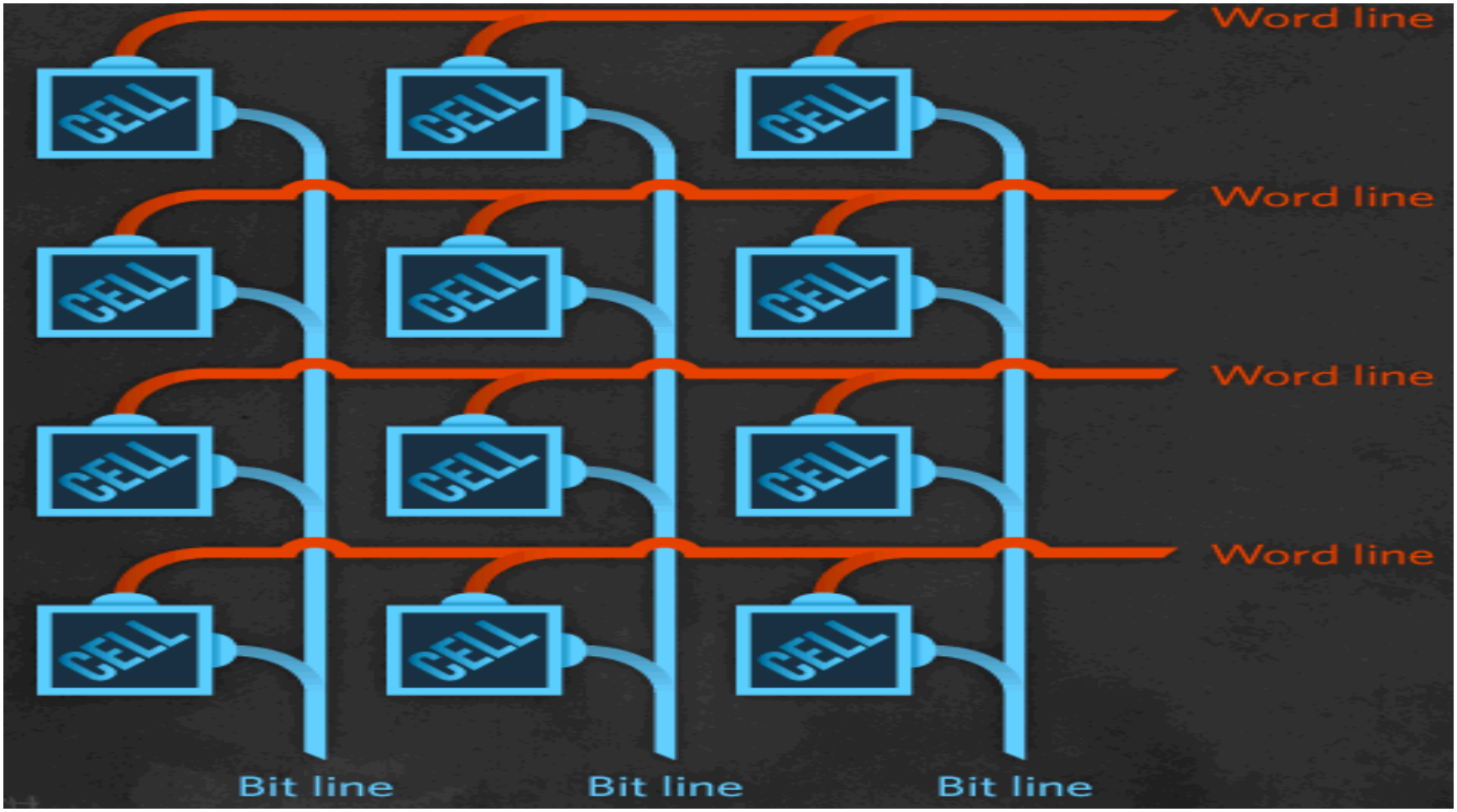
Agenda

- Why NAND / NOR ?
- NAND and NOR Electronics
- Phase Change Memory (PCM) Architecture
- Determine the limitations of NAND based storage and transition plan to PCM
- Evaluate strategies: PCM attributes comparison
- Recognize the efficiency and benefits of PCM
- Futuristic : How can the industry leverage ?

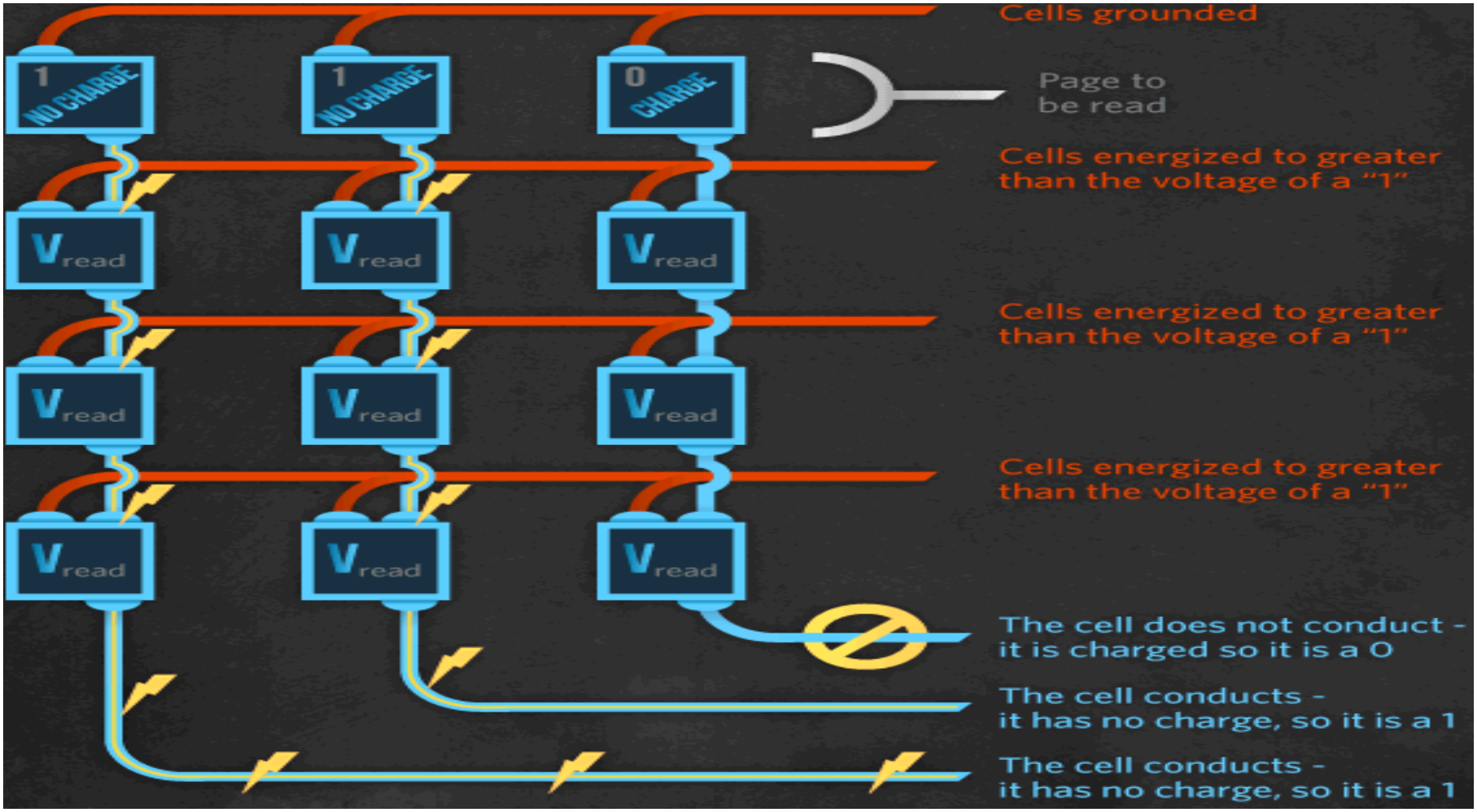
Why NAND or NOR ?



NOR Electronics

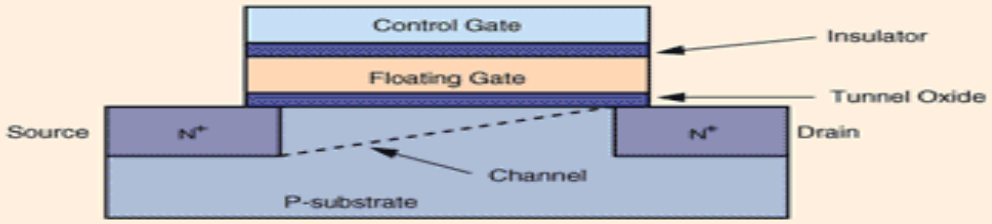


NAND Electronics



Cross Section

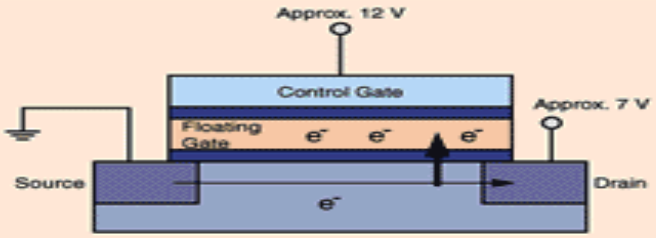
Cross Section of Flash Memory Cell



Principle of Operation (NOR type)

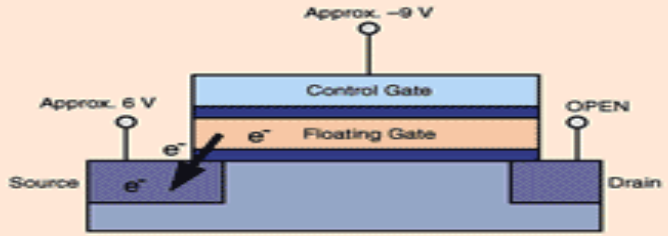
Write

Applies the voltage at approx. 7 V to the drain to activate the electrons (hot electron) around the channel, then also applies at approx. 12 V to the control gate. In this way the electrons are injected into the floating gate through the tunnel oxide.



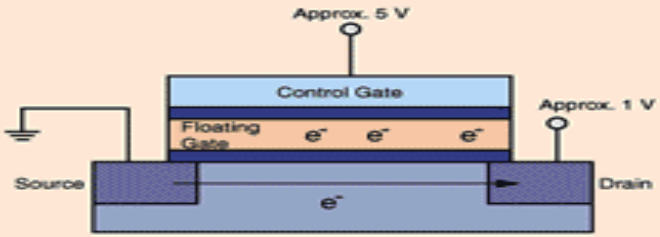
Erase

Applies the voltage at approx. −9 V to the control gate and at approx. 6 V to the source. The electrons in the floating gate are pulled off and transferred to the source (tunnel current).



Read

Applies the voltage at approx. 5 V to the control gate and at approx. 1 V to the drain. The state of the memory cell is distinguished by the current flowing between the drain and the source.



How does Flash work ?

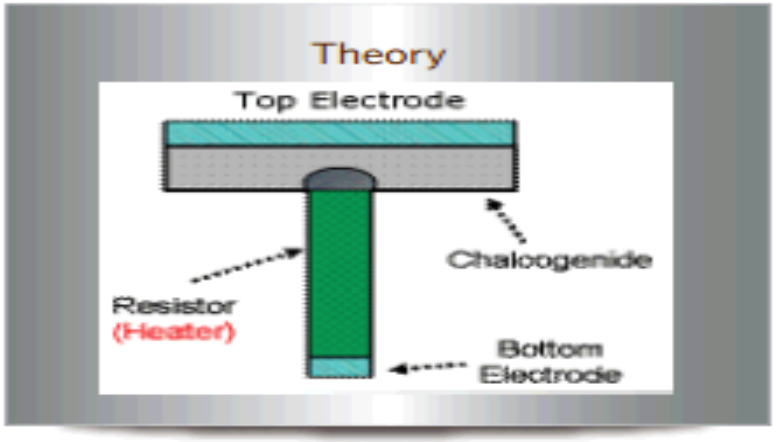
- Modulating charge stored within the gate of a MOS transistor.
- Presence of charge within the gate shifts the transistor's threshold voltage (1 or 0).
- Changing the bit's state requires removing the accumulated charge, which demands a relatively large voltage to suck the electrons off the floating gate.
- This burst of voltage is provided by a charge pump which takes some time to build up power.
- **Write time:** 0.1 millisecond for a block.

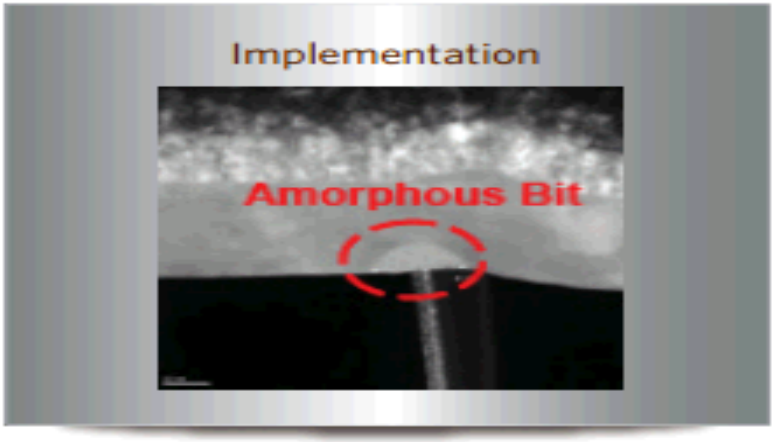
Phase Change Memory (PCM) Architecture

- Chalcogenide glass (Alloy of Germanium:Antimony:Tellurium 2:2:5).
- Material used in DVD-RW/CD-RW.
- Heat produced by passage of electric current changes states.
- **Two states:** Amorphous and Crystalline based on Electrical Resistivity.
- Amorphous represents binary 0 and is High Resistance state.
- Crystalline represents binary 1 and is Low Resistance state.
- Crystallization timescale : Order of 100 nanoseconds.
- **Partial Crystallization:** Two more states. **MLC PCM.**

Phase Change Memory Architecture

Structure	Sample	Properties
Amorphous		• Short-range atomic Order • High reflectivity • High resistivity
Polycrystalline		• Long-range atomic Order • Low reflectivity • Low resistivity





Example phase change storage element

Phase Change Memory : Industry Adoption

- Feb 2008 : Intel / STM revealed first MLC PRAM prototype.
- April 2010 : Numonyx announced the Omneo line of 128-Mbit NOR-compatible phase-change memories and Samsung announced shipment of its 512 Mb PCM in a multi-chip package (MCP) for use in mobile handsets by Fall 2010.
- June 2011 : IBM creates stable, reliable, multi-bit phase change memory with high performance and stability.
- July 2012 : Micron announced 45nm 1GB PCM chips.
- Aug 2014: HGST using PCM delivers three million random read I/Os (512-byte) and a random read access latency of 1.5 microseconds (i.e.) two orders of magnitude smaller than the fastest SLC NAND flash.

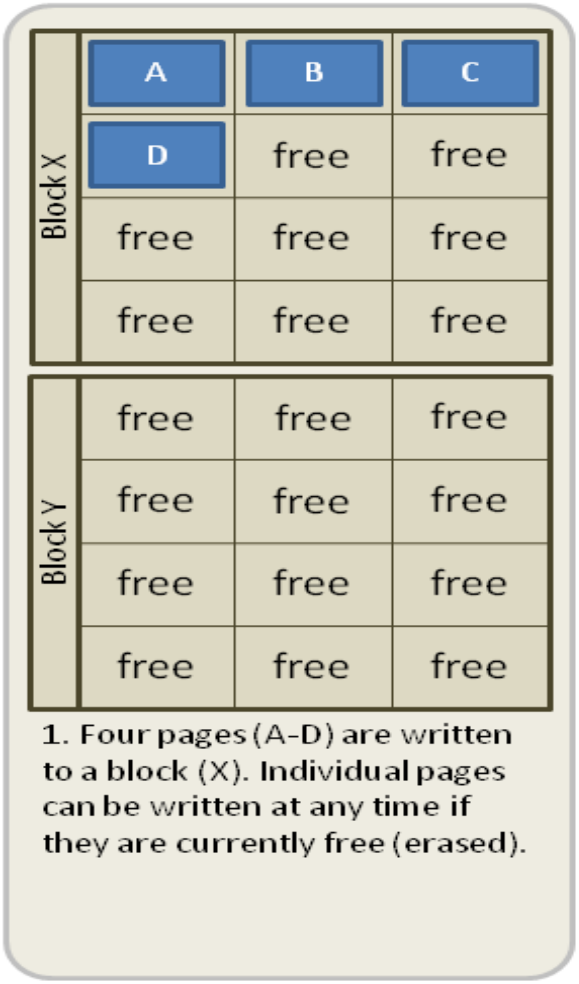
Determine the limitations of NAND based storage and transition plan to PCM

- Scaling difficulties as chip lithography shrinks.
- Each burst of voltage across the cell causes degradation.
- Flash memory leaks charges which causes corruption and loss of data.
- Flash devices traps electrons to store information. Susceptible to data corruption from radiation (unsuitable for space applications).

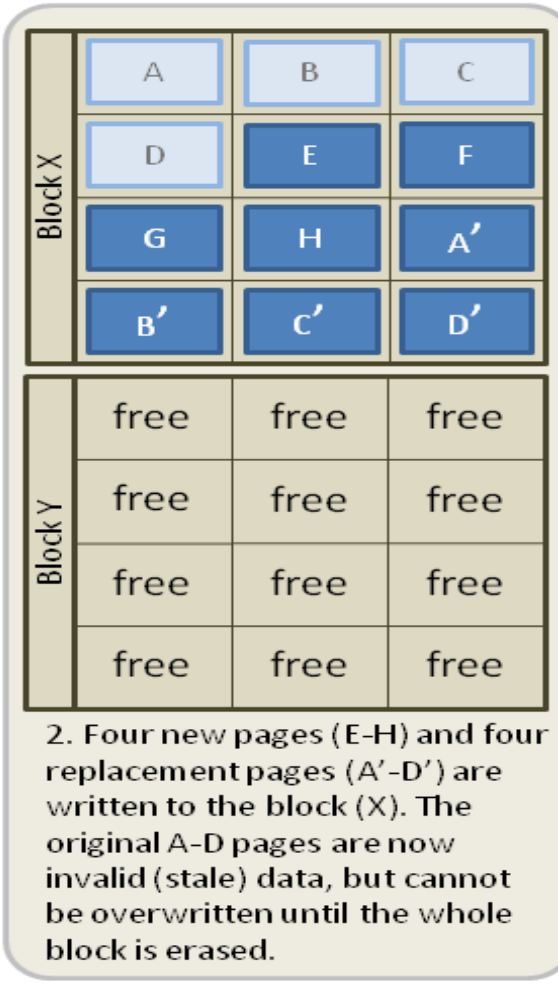
Determine the limitations of NAND based storage and transition plan to PCM (continued)

- The I/O interface of NAND flash does not provide a random-access external address bus. Rather, data must be read on a block-wise basis.
- Only finite amount of read/write cycles possible in a specific block.
- Repeated writes and rewrites of data blocks on a full SSD without giving the SSD time to perform garbage collection and cleaning can overwhelm the SSD controller's ability to manage free blocks and can lead to low observed performance.

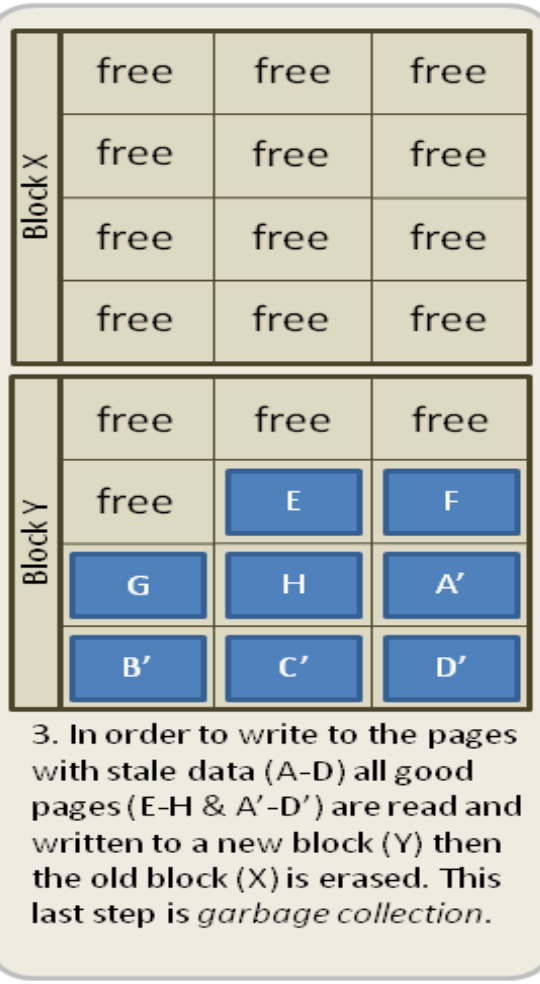
Determine the limitations of NAND : Write Amplification and Garbage Collection



1. Four pages (A-D) are written to a block (X). Individual pages can be written at any time if they are currently free (erased).

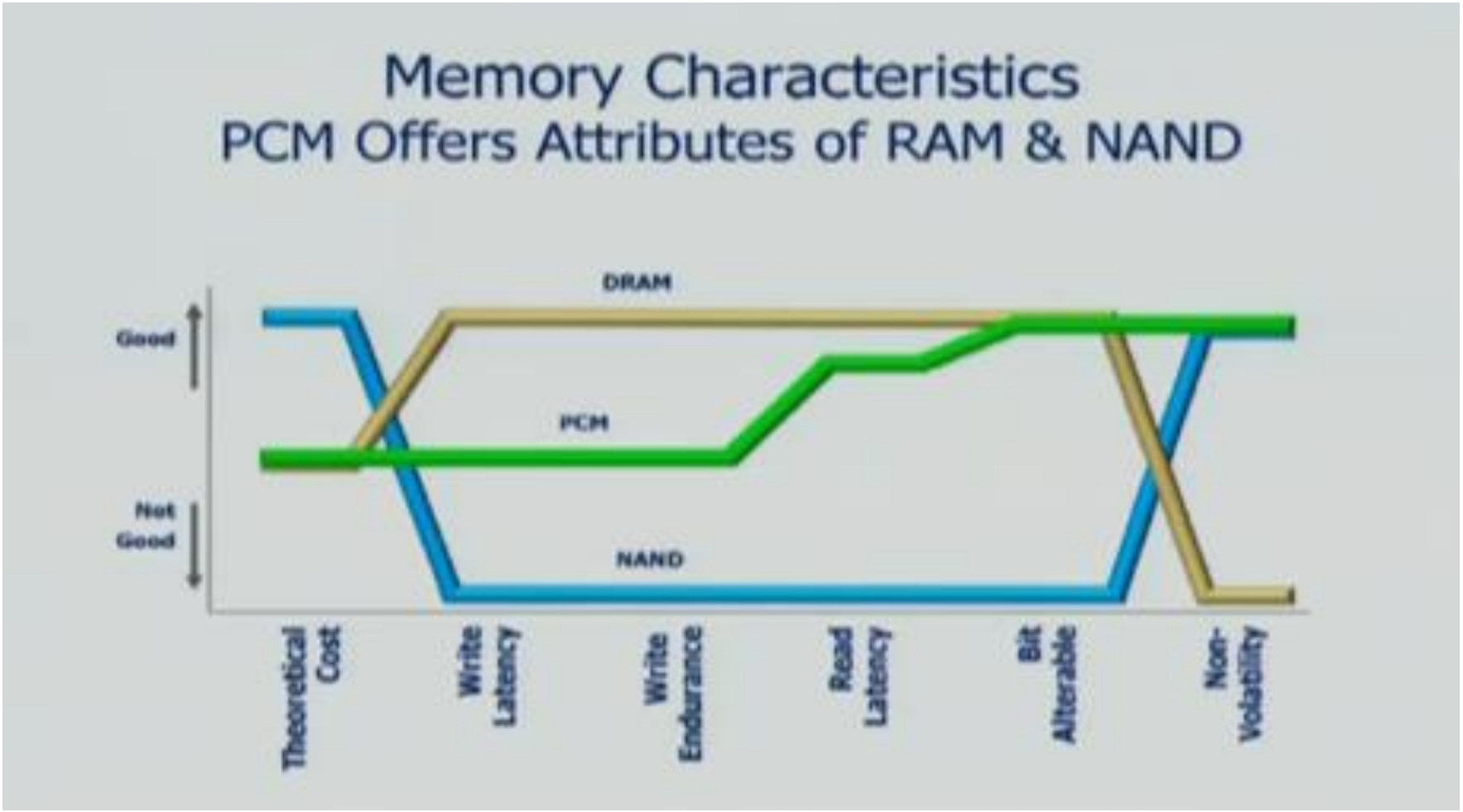


2. Four new pages (E-H) and four replacement pages (A'-D') are written to the block (X). The original A-D pages are now invalid (stale) data, but cannot be overwritten until the whole block is erased.



3. In order to write to the pages with stale data (A-D) all good pages (E-H & A'-D') are read and written to a new block (Y) then the old block (X) is erased. This last step is *garbage collection*.

Evaluate Strategies : PCM attributes comparison - 1



Evaluate Strategies : PCM attributes comparison - 2

Performance & Density Comparisons

Circa 2011, 45nm Silicon

Attributes	DRAM	PCM	NAND	HDD
Non-Volatile	No	Yes	Yes	Yes
Idle Power	~100mW/GB	~1 mW/GB	~1 mW/GB	~10W
Erase / Page Size	No / 64Byte	No / 32Byte	Yes / 256KB	No / 512Byte
Write Bandwidth	~GB/s per die	50-100 MB/s per die	5-40 MB/s per die	~200MB/s per drive
Page Write Latency	20-50 ns	~1 us	~500 us	~5 ms
Page Read Latency	20-50 ns	~70 ns	~25 µs	~5 ms
Endurance	∞	$10^{16} \rightarrow 10^{7}$	$10^{5} \rightarrow 10^{4}$	∞
Maximum Density	4Gbit	4Gbit	64Gbit	2TByte

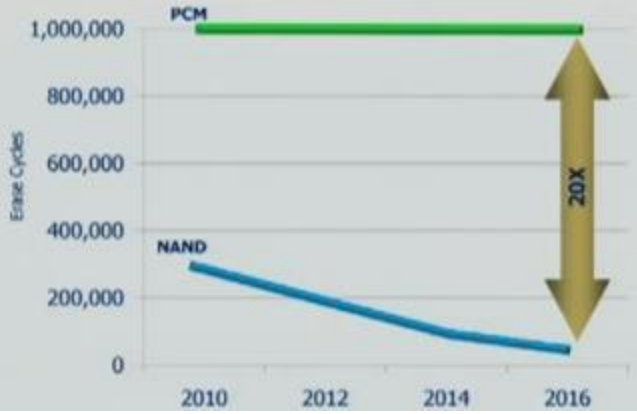
Evaluate Strategies : PCM attributes comparison - 3

Theoretical Chip Cost Factors

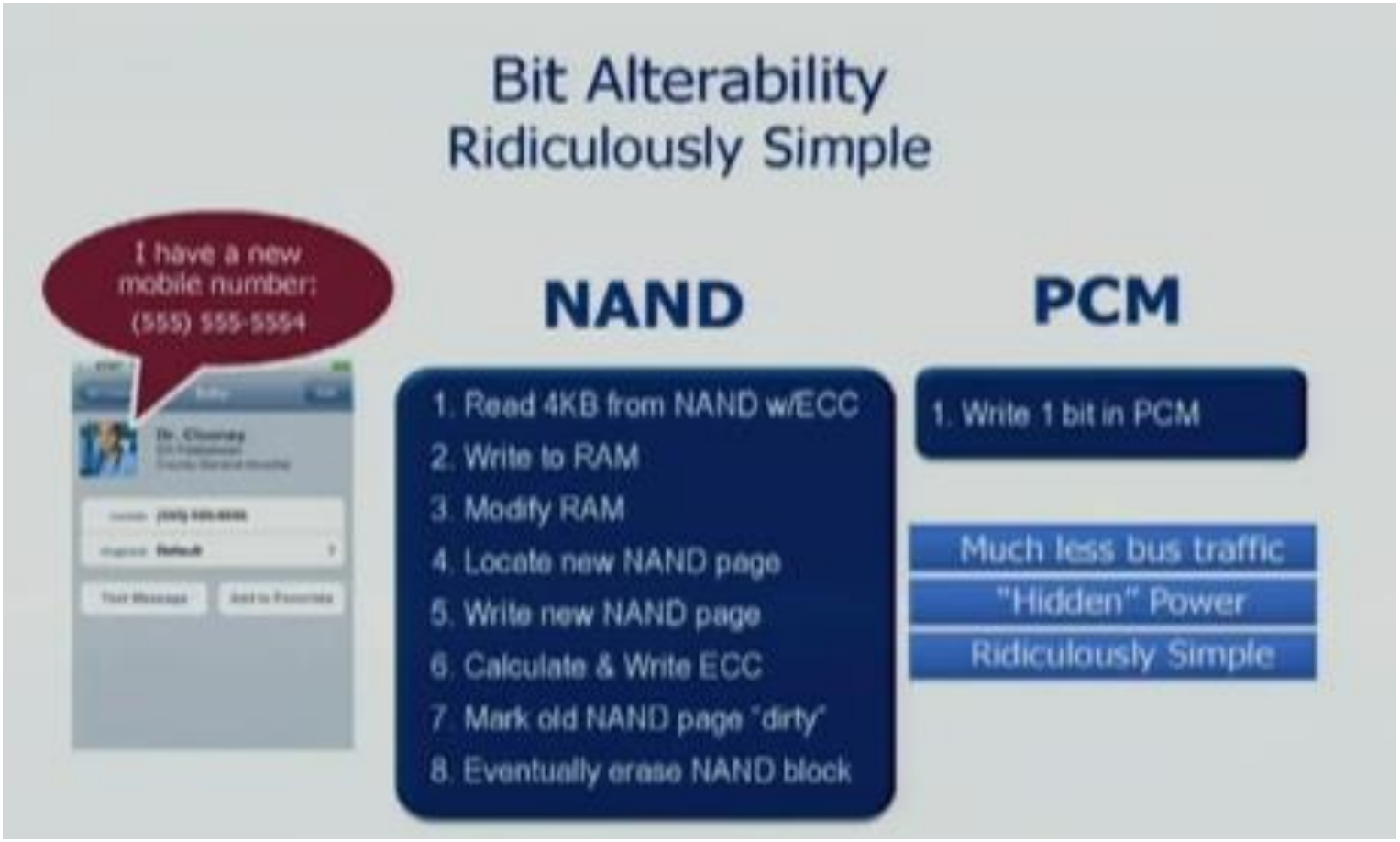
Silicon Cost Component		SLC PCM	DRAM	SLC NAND
Die Size	Cell Size (F^2)	5.5	6.0	5.0
	4G Prod Example	1.0x	1.2x	1.0x
Wafer Complexity	Total Process Mask Count	~35	~34	30
	300mm cost structure	1.2x	1.2x	1.0x
Theoretical Die Cost Summary		1.2x	1.4x	1.0x

- PCM will be cheaper than DRAM at lithography parity
- PCM scales to lower densities better than NAND
- PCM attributes can also save cost at system level

Endurance Scalability



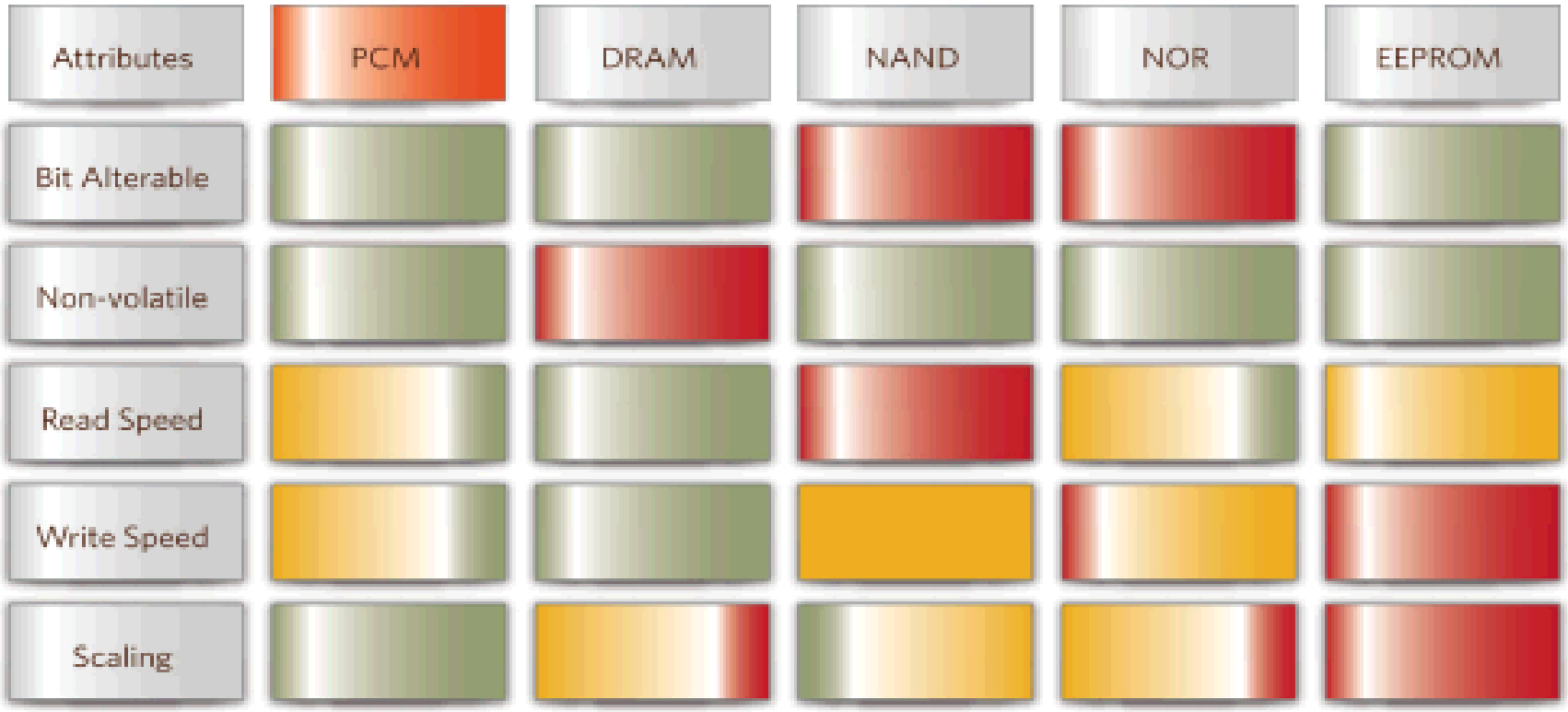
Evaluate Strategies : PCM attributes comparison - 4



Recognize the efficiency and benefits of PCM over Flash (NAND/NOR)

- Memory element can be switched more quickly.
- Single bit can be changed (1 or 0) without needing to first erase an entire block of cells.
- PCM can endure 100 million write cycles.
- At normal working temperature of 85 degree C, it can retain data for 300 years.
- PCM exhibits higher resistance to radiation.
- PCM is ideal for workloads with “read often, write rarely” characteristics.

Recognize the efficiency and benefits of PCM over Flash (NAND/NOR) (continued)



PCM Attributes: This new class of non-volatile memory brings together the best attributes of NOR, NAND and RAM.

Phase Change Memory : Limitations

- Degradation due to GST thermal expansion.
- Metal migration.
- Soldering creates high temperature which wipes pre-programmed PCM content.
- Need a way to program in PCM post soldering.
- Other unknown reasons.

Quartz : September 2012

- Hitachi creates a prototype where High-precision laser is used to embed dots of binary code across a tiny piece of quartz glass.
- Optical Microscope paired with computer to decipher original data.

- Stress test: 2cm^2 of quartz heated to 1000 degree centigrade for 2 hours and still the data was recovered.
- Data density: Multi-layered quartz glass maxing out around 40MB per square inch.

Futuristic : How can the Industry leverage?

- Leverage XIP (Execute in Place) feature of NOR for executables during bootup.
- If PCM gets widely deployed, exploit the bit alterability feature.
- Algorithms
  - The Flash write amplification and garbage collection algorithms will not be required anymore.
- Leverage “Flexible Storage Sharing” and “SmartIO” capability of Symantec Storage Foundation and High Availability on PCM.
- Measure the Evolution of MRAM, RRAM technologies in comparison with PCM.

Q & A

- Any questions / suggestions ?

Thanks to SNIA SDC Team ☺

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