SDC

STORAGE DEVELOPER CONFERENCE

SNIA SANTA CLARA, 2017

Latency and Throughput in SSD Controllers for Persistent Memory

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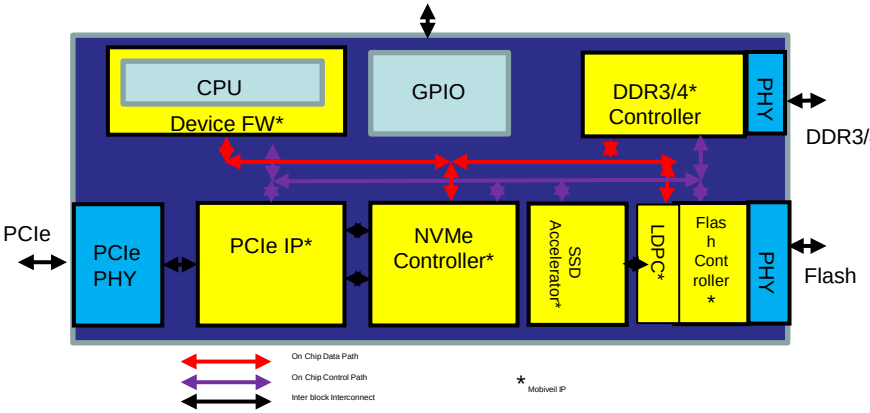
Mobiveil Inc.

SSD Controller Platform

- Mobiveil Inc. is Silicon IP and Platform Provider
- Wide range of customer requirements: Requires high degree of Scalability and Configurability in SSD Controller Platform



- Mobiveil SSD Controller Platform is being deployed for Persistent Memories
- Partnership with Crossbar on ReRAM SSD and ReRAM NVDIMM

ReRAM SSD M.2

ReRAM

- **500 MT/s** interface
  - 8-bit ONFI 4
- **1us Read** Time
- **2us Program** Time
- **No-Erase Required**
- **Multi-Bank Architecture**

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Controller

- **8 GT/s** per lane
  - PCIe Gen3 X 4 IF
- **8 ONFI 4** channels
- ECC
- No External DRAM

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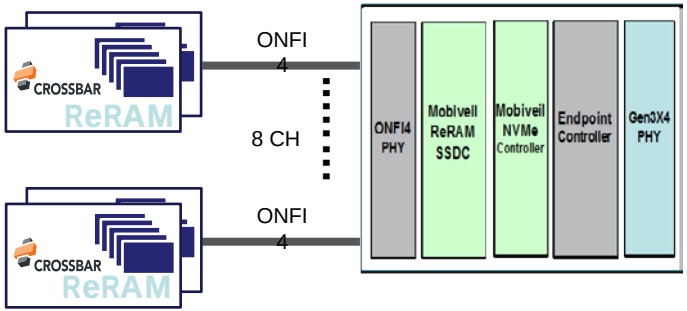
NVMe Module

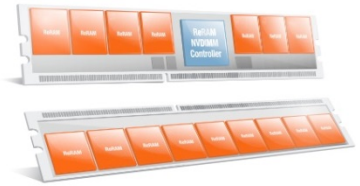
PCIe M.2

- Read Performance
  - **Random Read Latency: 10us** (Max)
  - **6.4M Random 512B IOPS**
  - 800K Random 4K IOPS
- Write Performance
  - **Write latency: 10us** (max, without caching)
  - **6.4 Million Random 512B IOPS**
  - 800K Random 4K IOPS
  - No Erase prior to Write command
- Endurance: **10^5 Write cycles**

Block Diagram



ReRAM NV-DIMM



ReRAM

- **800 MT/s** interface
  - 8-bit ONFI 4
- **1us Read** Time
- **2us Program** Time
- **No-Erase Required**
- **Multi-Bank Architecture**

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Controller

- **1600 MT/s** per lane
  - 64-bit DDR3
- **16 ONFI 4** channels
- ECC
- No External DRAM

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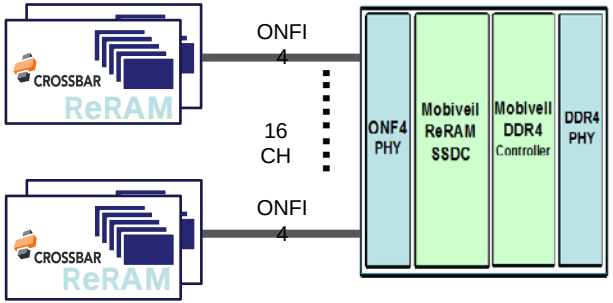
DIMM Module

- Read Performance
  - **Random Read Latency: 4us** (Max)
  - **24M Random 512B IOPS**
  - 3M Random 4K IOPS
- Write Performance
  - **Write latency: 4us** (max, without caching)
  - **24 Million Random 512B IOPS**
  - 3M Random 4K IOPS
  - No Erase prior to Write command
- Endurance: **10^5 Write cycles**

Block Diagram



Latency in Error-Correction Coding

- ECC is a necessary element in every memory
  - Wide range of latencies depending on correction capability, word size and type of ECC used
- Minimal latency for small (1 or 2 bit correction) codes

- Most powerful ECC option – LDPC can still have low latency
  - Example from Mobiveil LDPC compiler (decoding latency):
    - BOL: 75 clock cycles, EOL: 155 clock cycles
  - Significant further reduction in LDPC latency is possible
    - Theoretical limit <20 clock cycles EOL