

SDC 18

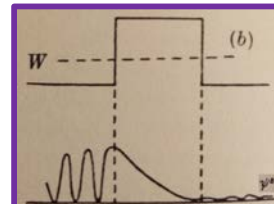
September 24-27, 2018
Santa Clara, CA

www.storagedeveloper.org

Tunneling through Barriers

The Key to the Evolution of Solid State Memories

Andrew J. Walker PhD
Spin Transfer Technologies



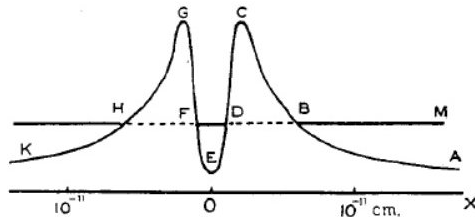
Link between α -particles, 3-D NAND and MRAM - Tunneling

3-D NAND

α -particles

SEPTEMBER 22, 1928] *NATURE*

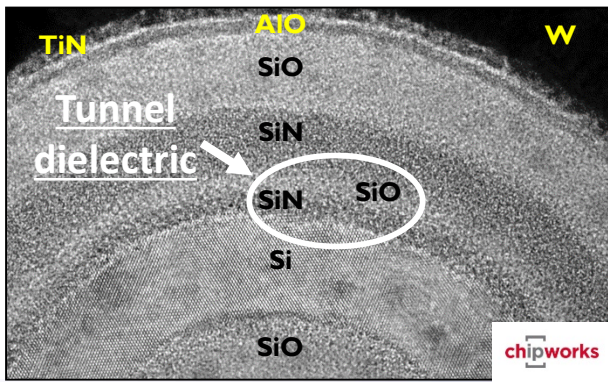
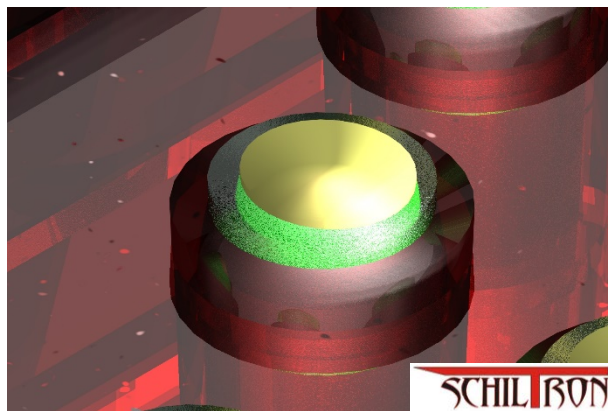
Wave Mechanics and Radioactive Disintegration



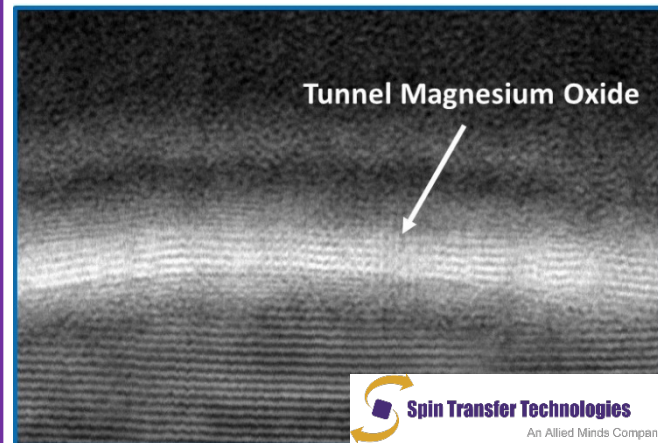
Much has been written of the explosive violence with which the α -particle is hurled from its place in the nucleus. But from the process pictured above, one would rather say that the α -particle slips away almost unnoticed.

RONALD W. GURNEY,
EDW. U. CONDON.

Palmer Physical Laboratory,
Princeton University,
July 30.



STT-MRAM

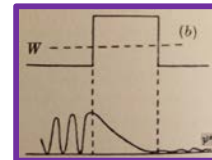


Free layer \downarrow CoFeB

Tunnel barrier MgO

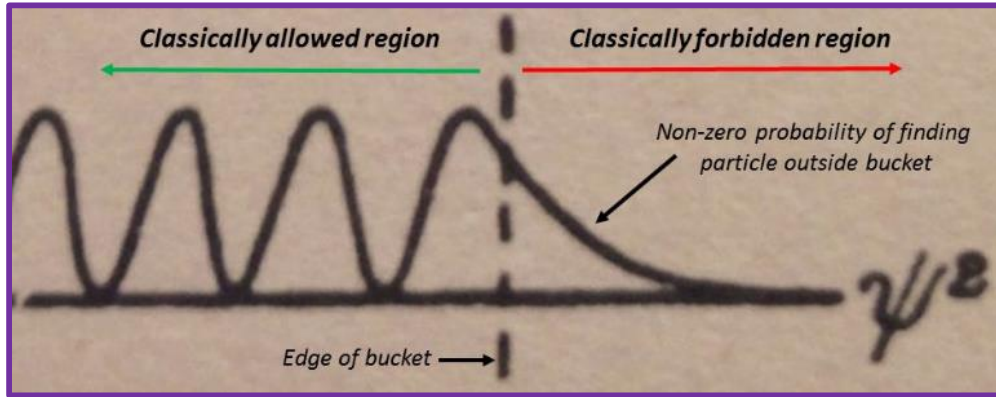
Reference layer \uparrow CoPt

Contents

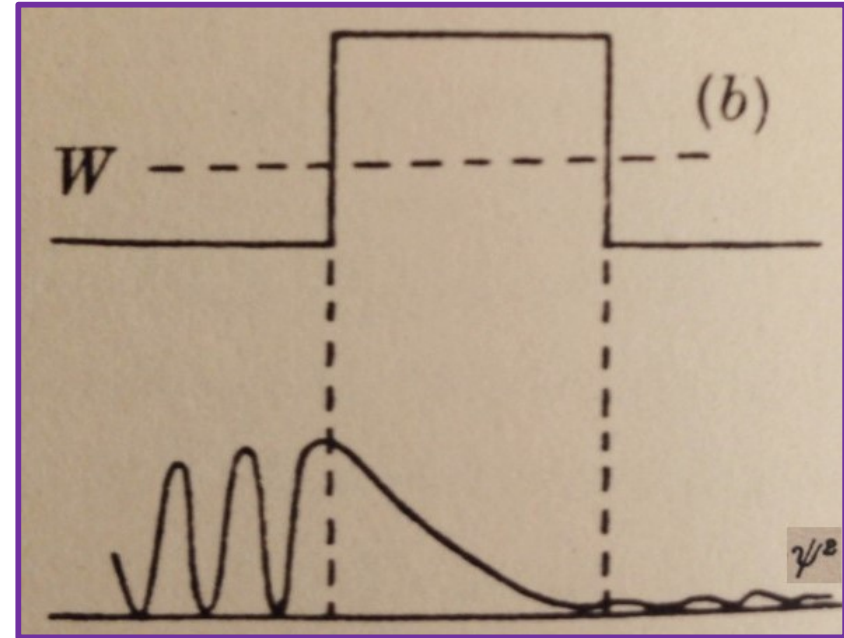


- ❑ ***What is Tunneling?***
- ❑ ***Tunneling in Solid State Memories***
 - ❑ 2-D NAND
 - ❑ 3-D NAND
 - ❑ Classic SONOS
 - ❑ STT-MRAM
- ❑ ***Tunneling Damage***
- ❑ ***The Golden Thread of Tunneling – From Fundamental Physics to Technological Innovation***
- ❑ ***The Golden Thread Continues – STT-MRAM: A Unique Tunneling Conundrum***
- ❑ ***Tunneling Engineering***
- ❑ ***Conclusions***
- ❑ ***Tunneling in Silicon Valley***
- ❑ ***Acknowledgements***
- ❑ ***Appendix***

What is Tunneling?

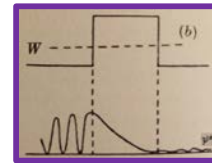


"We shall not expect to find in quantum mechanics anything so definite as this sharp dividing surface"



Elementary Quantum Mechanics, R.W. Gurney, 2nd ed., Cambridge University Press, 1940

Tunneling in Solid State Memories



❑ 2-D NAND

- ❑ Charge tunneling to and from a Floating Gate

❑ 3-D NAND

- ❑ Charge tunneling to and from:
 - ❑ Silicon Nitride (Samsung, Toshiba, WD-SanDisk, Hynix)
 - ❑ Floating gate (Intel, Micron)

❑ Classic SONOS

- ❑ Charge tunneling to and from silicon nitride

❑ STT-MRAM

- ❑ Electron tunneling between magnetic metals

Basic Components

Field Effect Device

- ❑ Electrometer to measure charge

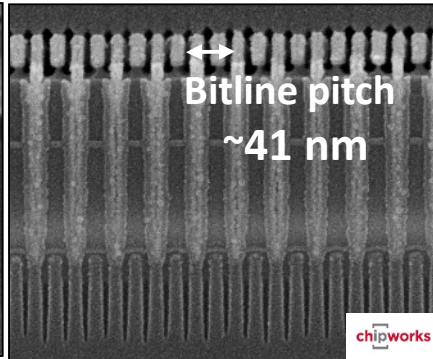
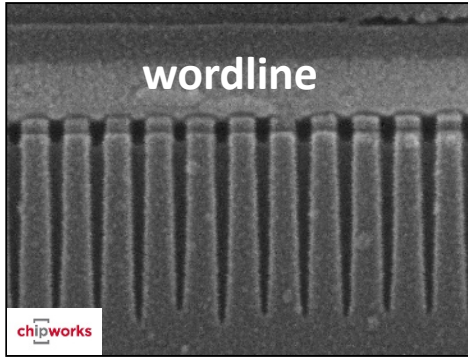
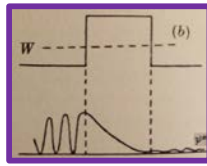
Charge Reservoir

- ❑ Nitride or Floating Gate

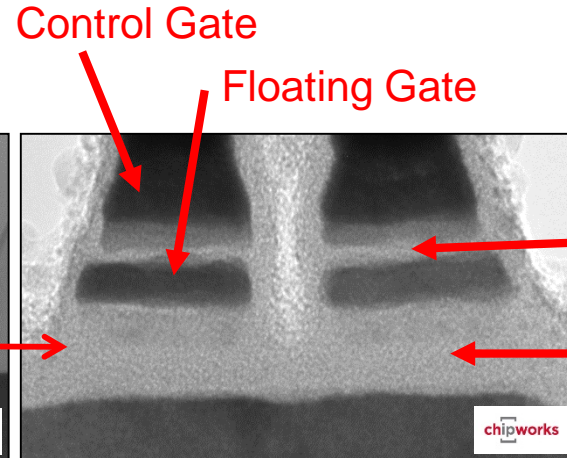
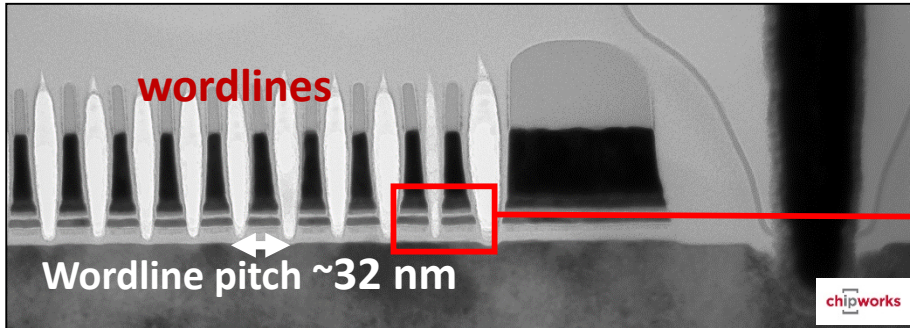
Move Charge In/Out

- ❑ Tunneling

2-D NAND Flash



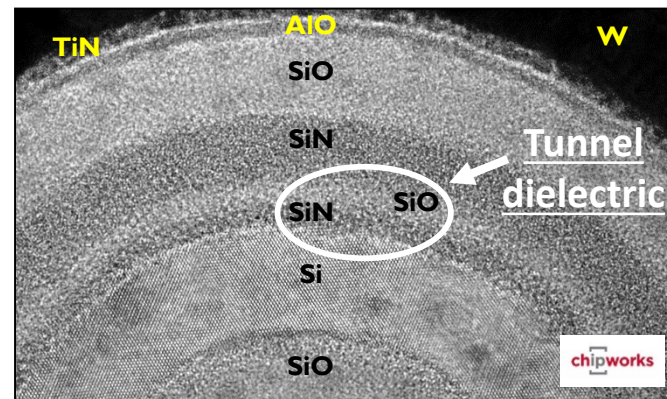
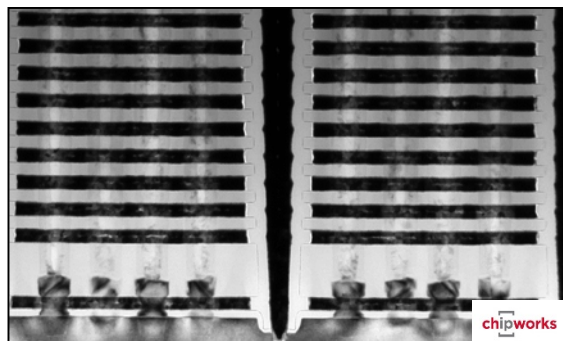
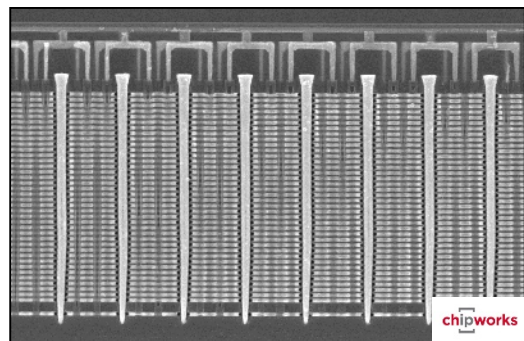
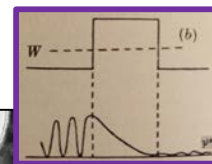
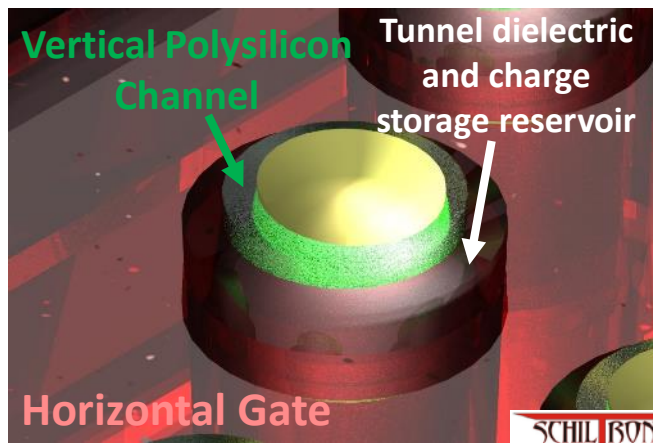
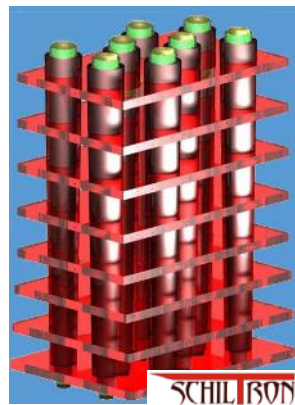
128 Gbit 16 nm 2-D NAND
from Intel/Micron



Control Gate
Floating Gate
Dielectrics between gates
Tunnel oxide
(~7 nm)

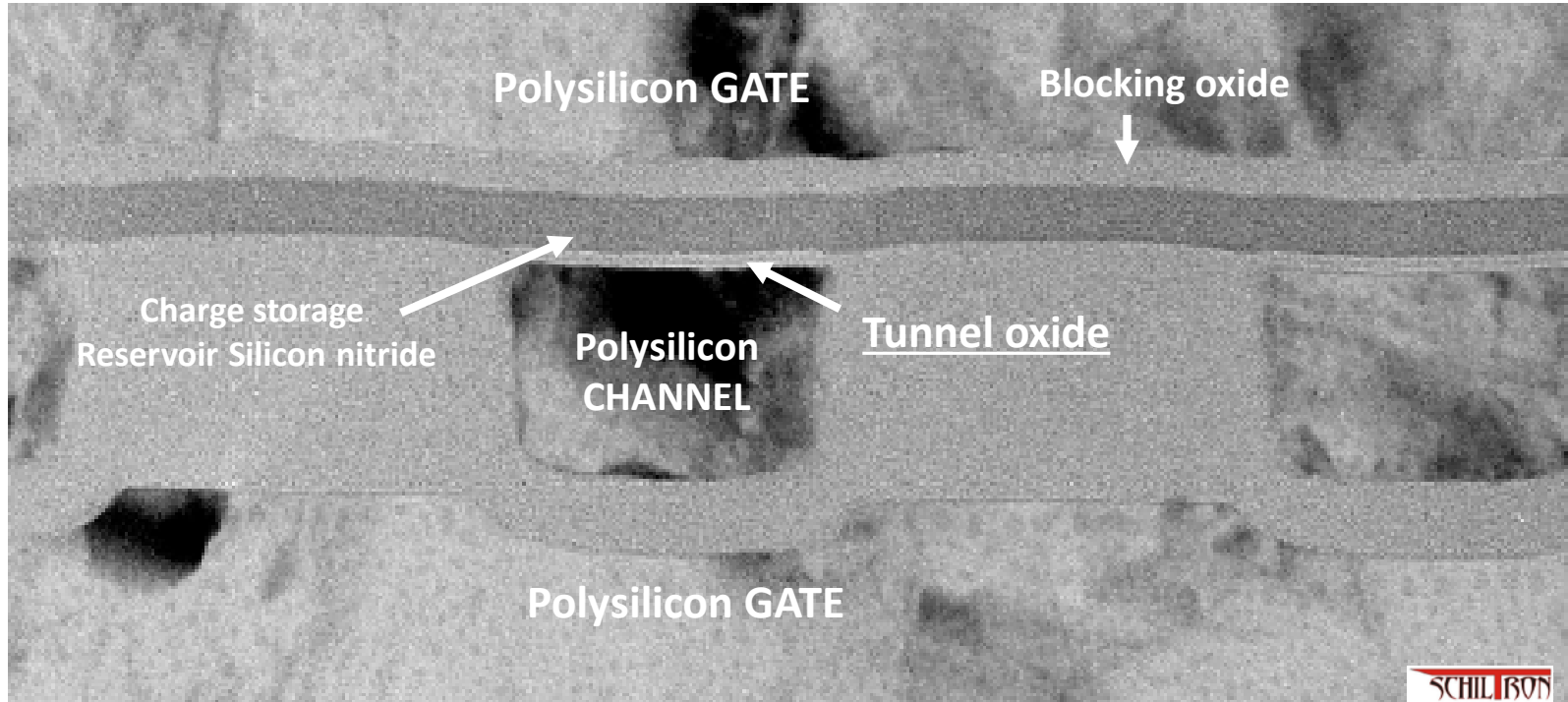
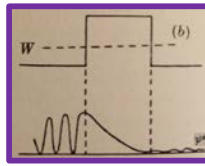


3-D NAND Flash



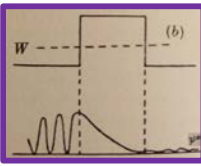
86 Gbit V-NAND from Samsung

Classic SONOS in 3-D

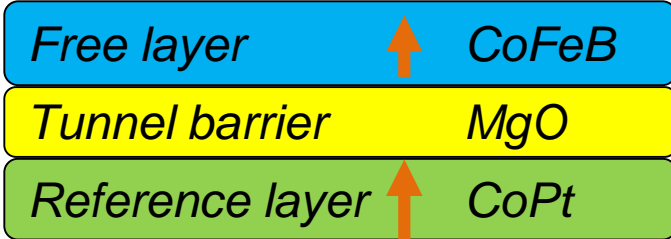


A.J. Walker, IEEE Trans. Elect. Dev., vol.56, Nov.2009

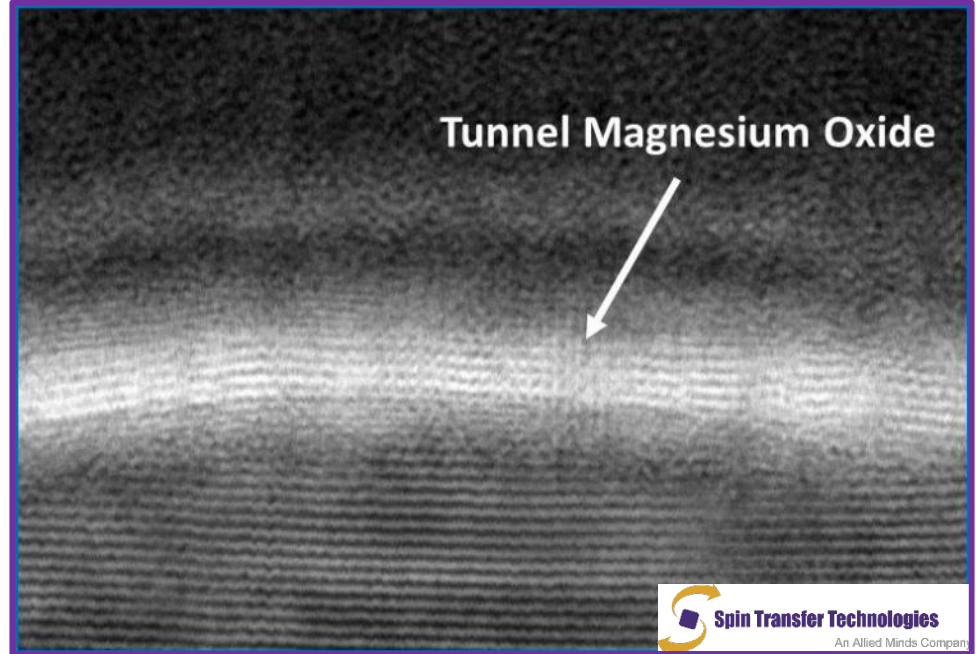
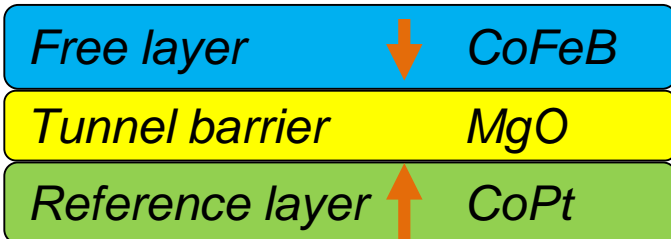
STT-MRAM



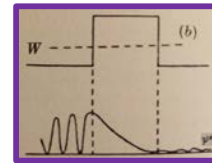
Low resistance P-state Logical "0"



High resistance AP-state Logical "1"



Tunneling Damage



❑ **Rule of Thumb:**

- ❑ Tunneling creates more damage in thicker tunnel dielectrics

❑ **What is thick and what is thin?**

- ❑ $>/\sim 3.5\text{nm}$ is THICK (2-D and 3-D NAND)
- ❑ $</\sim 3.5\text{nm}$ is THIN (Classic SONOS and STT-MRAM)

❑ **What is damage and what are the consequences?**

❑ Charge trapping:

- ❑ Threshold voltage shifts (in MOS-based memories – NAND and Classic SONOS)
- ❑ Shifts in Current-Voltage characteristics

❑ Stress induced damage:

- ❑ Limited retention (in MOS-based memories – NAND and Classic SONOS)
- ❑ Wear out and breakdown

Journal of Applied Physics

D. FROHMAN-BENTCKOWSKY AND M. LENZINGER
Fairchild Semiconductor, Research and Development Laboratory, 4001 Miranda Avenue, Palo Alto, California 94304
Received 19 February 1969; in final form 31 March 1969)



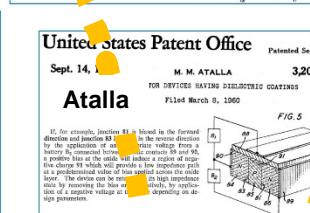
Wegener et al.

United States Patent [19] **4,115,914**
Harari [45] Sep. 26, 1978

**ELECTRICALLY ERASABLE
 NON-VOLATILE SEMICONDUCTOR
 MEMORY**

Inventor: **Eliyahu Harari, Irvine, Calif.**
 Assignee: **Hughes Aircraft Company, Culver City, Calif.**
 Appl. No.: **770,346**
 Filed: **Feb. 22, 1977**

The diagram is a cross-sectional view of a semiconductor device. It shows a substrate (40) with a layer (44) on top. A central structure (56) is formed on the substrate, with a top layer (64) and a side layer (58). A gate structure (62) is shown on the right side, with a top layer (60) and a side layer (46). A bottom layer (48) is also indicated. Various other components are labeled with numbers 40 through 64.



The storage mechanism will be discussed and experimental data that describe the wear-in, read-out, and storage characteristics of this device will be presented. The results of its application, in various experimental circuits, including a one-by-four electrically-alterable read-only memory, will be given in conclusion.

In order to study the emission through the potential energy step of fig. 1 we have only to solve the wave equations

$$\text{Fowler-Nordheim} \quad (x > 0), \quad (4)$$

$$(x < 0), \quad (5)$$

**A Floating Gate and Its Application
to Memory Devices**

By D. KAHN and S. M. SZE

(Manuscript received May 16, 1967)

DOI: 10.1002/jbm.10008

24.3 MONOS MEMORY ELEMENT, B. V. Keshavan at
inghouse Electric Corporation, Integrated Circuit
Md.

The use of metal-nitride-oxide-semiconductor structure was reported by Sze et al. at the 1967 Device
ence. When such a structure is used as p-channel
device, a positive gate voltage exceeding a certain critical
device into depletion mode. Later, when a negative gate
of this critical voltage is applied, the device changes be-
explained as electrons
the traps in the ni-
semiconductor with
nory element.

Fowler-Nordheim Tunneling into Thermally Grown SiO₂
M. LANGLEY and E. H. SNOW
Semiconductor Research and Development Laboratory, Palo Alto, California 94304
(Received 20 September 1968)

A NEW FLASH E²PROM CELL USING SIMPLE POLYSILICON TECHNOLOGY

FUJIO MASUOKA, MASAMICHI ASANO, HIROAKI IWASHASHI, TEISUKE KOMURO
and SHINICHI TANAKA

Lenzinger and Snow

INTEGRATED CIRCUIT DIV. TOSHIBA CORP.
KOMUKAI 1, SAINAIKU, KAWASAKI 210 JAPAN

Π - Π'

Control gate

Al_{0.9}Si_{0.1} gate line)

Floating gate

CONCLUSION

FLASH

1984

Selection transistor

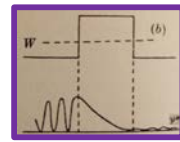
Masuoka et al.

FLOATING GATE 1967

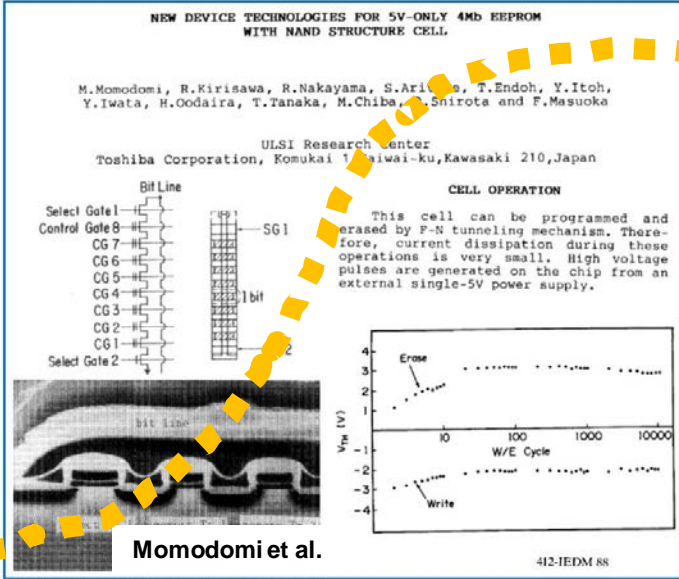
2018 Storage Developer Conference. © Spin Transfer Technologies. All Rights Reserved

The Golden Thread of Tunneling

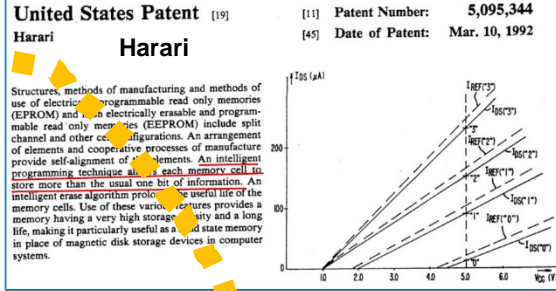
- From Fundamental Physics to Technological Innovation (2)



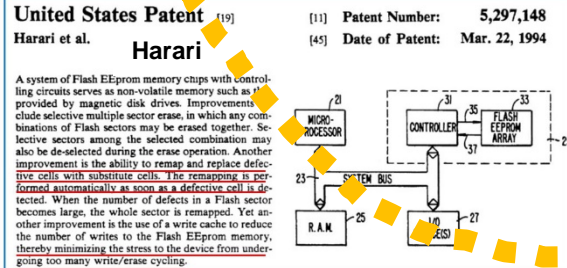
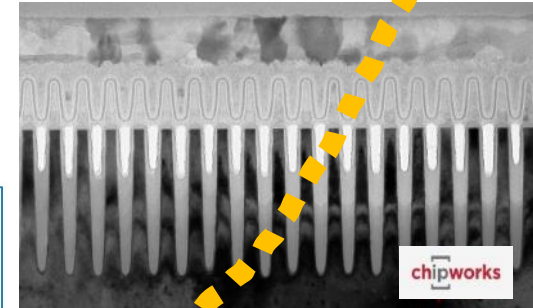
NAND FLASH 1988



MULTI-BIT 1992



LIMIT of 2-D NAND FLASH ~2016

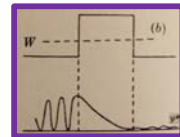


SYSTEM FLASH 1994

Enlargements in Appendix

The Golden Thread of Tunneling

- From Fundamental Physics to Technological Innovation (3)



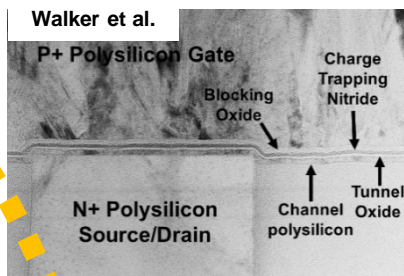
Thin Film Transistor (TFT) SONOS 2003

3D TFT-SONOS Memory Cell for Ultra-High Density File Storage Applications

Abstract

For the first time, a scalable, low power, deep-submicron TFT-SONOS (Thin Film Transistor Silicon-Oxide-Nitride-Oxide-Silicon) memory cell is described with characteristics rivaling those of single crystal devices ($>10^6$ cycles, $\sim 1.6V$ window after 10 years on cycled cell at 85C) showing the promise of 3D integration and ultra-small cell footprints. The ability to vertically stack device layers enables the current memory density record of $\sim 200\text{Mbyte/cm}^2$, set by 90nm NAND, to be surpassed.

(Keywords: TFT, SONOS, 3D, nonvolatile, memory)



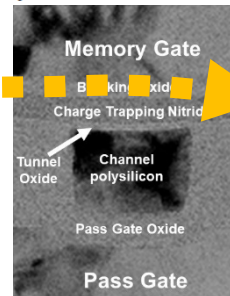
DG-TFT SONOS NAND 2008

Sub-50nm DG-TFT-SONOS – The Ideal Flash Memory for Monolithic 3-D Integration

Walker

Abstract

A revolutionary 3-D stackable sub-50nm double-gate TFT SONOS technology is presented here with series strings of up to 64 cells consisting of the smallest silicon-based TFT's to date. Read- and program-pass disturbs have been extinguished. Excellent endurance and retention are shown. Monolithic 3-D integration and scalability are ensured through close to zero source/drain diffusion. Finally, comparisons with TANOS are given.

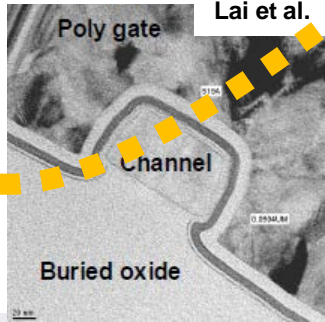


TFT SONOS NAND 2006

A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory

Abstract

A double-layer TFT NAND-type Flash memory is demonstrated, ushering into the era of three-dimensional (3D) Flash memory. A TFT device using bandgap engineered SONOS (BE-SONOS) [1,2] with fully-depleted (FD) poly silicon (60 nm) channel and tri-gate P⁺-poly gate is integrated into a NAND array. Small devices ($L/W=0.2/0.09\text{ }\mu\text{m}$) with excellent performance and reliability properties are achieved. The bottom layer shows no sign of reliability degradation compared to the top layer, indicating the potential for further multi-layer stacking. The present work illustrates the feasibility of 3D Flash memory.

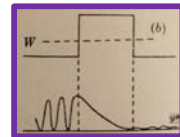


The Rise of Monolithic 3-D Flash

Enlargements in Appendix

The Golden Thread of Tunneling

- From Fundamental Physics to Technological Innovation (4)

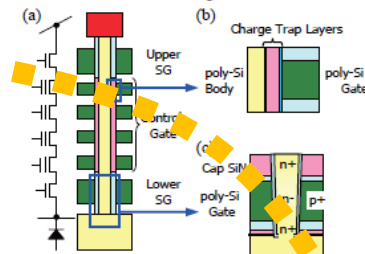


Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory

Tanaka et al.

Abstract

We propose Bit-Cost Scalable (BiCS) technology which realizes a multi-stacked memory array with a few constant critical lithography steps regardless of number of stacked layer to keep a continuous reduction of bit cost. In this technology, whole stack of electrode plate is punched through and plugged by another electrode material. SONOS type flash technology is successfully applied to achieve BiCS flash memory. Its cell array concept, fabrication process and characteristics of key features are presented.



The Rise of Vertical Channel 3-D NAND Flash

Vertical Channel TFT SONOS TCAT NAND 2009

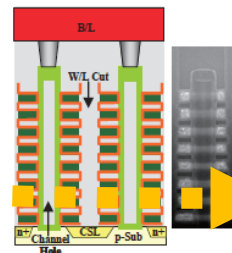
Vertical Channel TFT SONOS BiCS NAND 2007

Vertical Cell Array using TCAT(Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory

Jang et al.

Abstract

Vertical NAND flash memory cell array by TCAT (Terabit Cell Array Transistor) technology is proposed. Damascened metal gate SONOS type cell in the vertical NAND flash string is realized by a unique 'gate replacement' process. Also, conventional bulk erase operation of the cell is successfully demonstrated. All advantages of TCAT flash is achieved without any sacrifice of bit cost scalability.

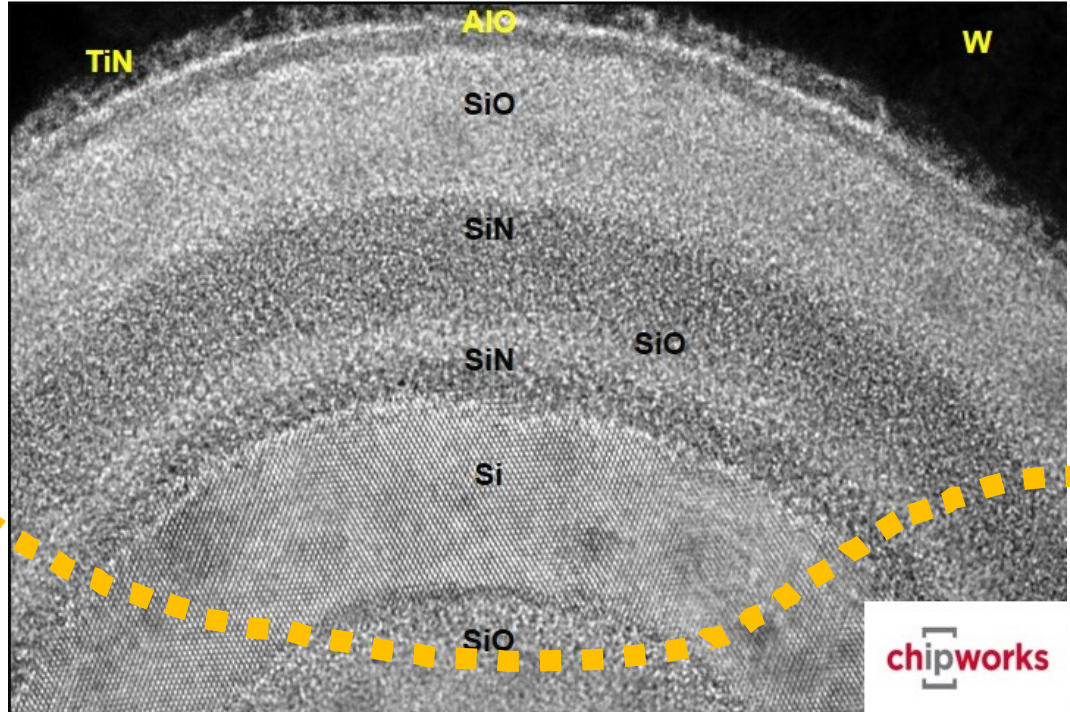
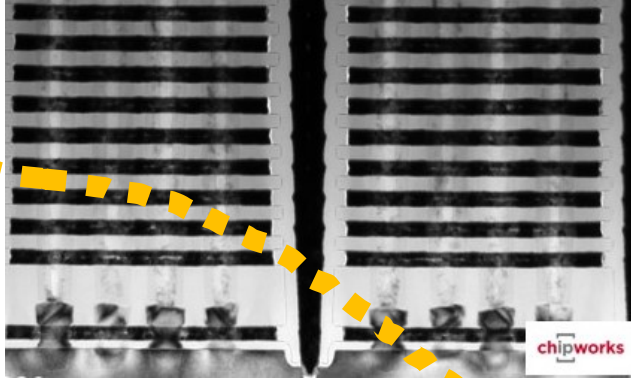
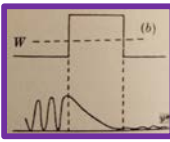


Enlargements in Appendix

The Golden Thread of Tunneling

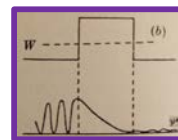
- From Fundamental Physics to Technological Innovation (5)

Rise of 3-D NAND FLASH > 2013



The Golden Thread Continues:

STT-MRAM: A Unique Tunneling Conundrum



Magnetic
Tunnel
Junction
(MTJ)

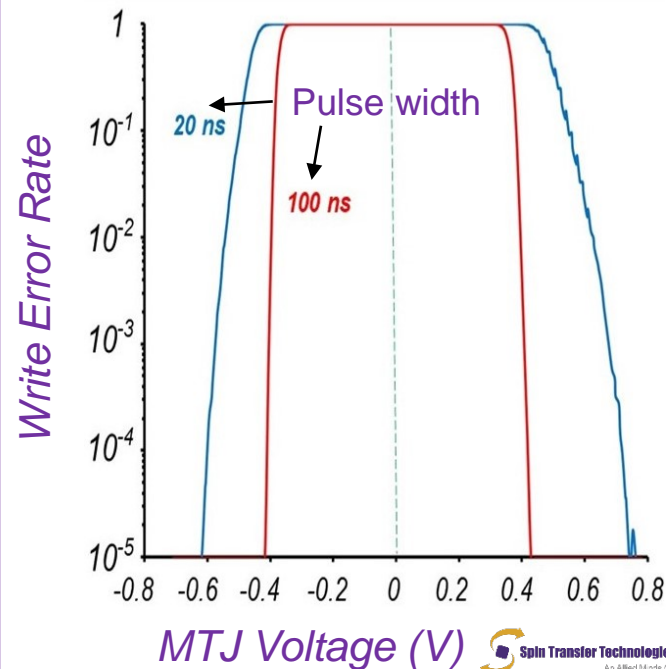
Free layer CoFeB

Tunnel barrier MgO

Reference layer CoPt

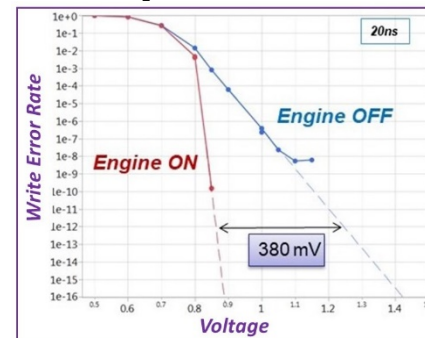
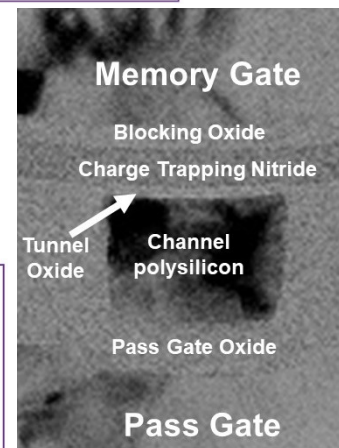
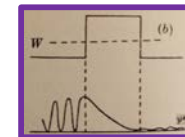
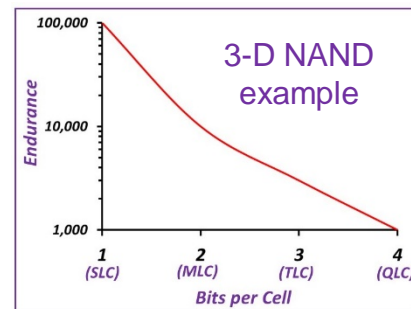
- **Write Error Rate needs large tunnel current**
 - Limits endurance due to oxide wear out mechanism
- **High endurance with low Write Error Rate needs reduced tunnel current**
 - Make Free Layer magnetically less “stiff”
 - Reduce MTJ area
 - Use special design techniques

The Stochastic “Top Hat”

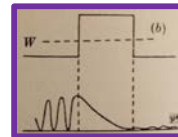


Tunneling Engineering

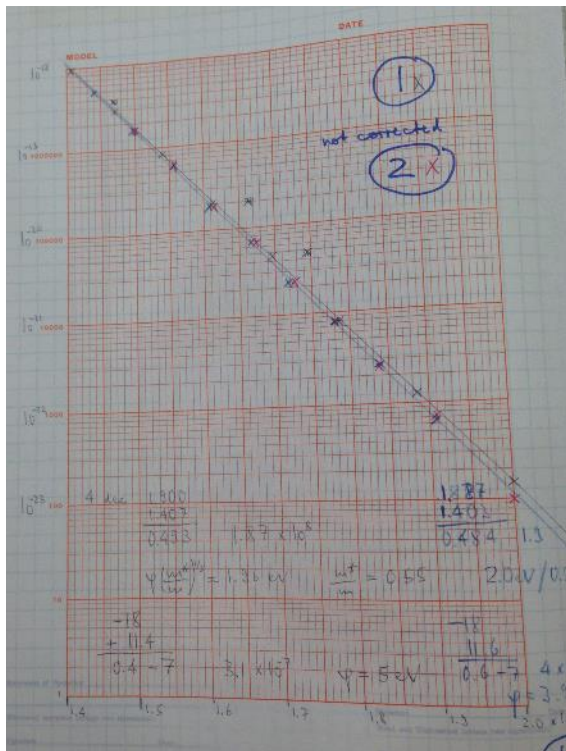
- ❑ **NAND Flash increases electrical bits/cell:**
 - ❑ Cost in endurance (orders of magnitude reduction)
 - ❑ Cost also in read and program speeds
- ❑ **SLC NAND endurance limited by thick tunnel oxide damage**
- ❑ **New device architectures can allow thin tunnel oxides**
 - ❑ 3-D Dual-Gate SONOS allows millions of endurance cycles
- ❑ **STT-MRAM endurance boosted by design techniques**
 - ❑ Up to 6 orders of magnitude gain allowing SRAM/DRAM replacement



Tunneling Conclusions



- ❑ *A long and illustrious history*
- ❑ *The foundation of many solid state memory technologies*
- ❑ *Creates damage and must be monitored*
 - ❑ Architectures, circuits and systems can take advantage of the physics knowledge to control and boost endurance
- ❑ *Continues to grow in importance:*
 - ❑ 3-D NAND evolution
 - ❑ Other 3-D solid state memory approaches
 - ❑ STT-MRAM



Lab Notebook #764
Martin Lenzlinger

Type ② characteristics seem to be temperature independent. They fit a Fowler-Nordheim plot, resulting in reasonable values for the Si-SiO₂ and Al-SiO₂ barrier height.

Conclusion: The current through the oxide is limited by the tunneling injection.

Signature M. Lenziger Date Nov. 1, 67
Read and Understood (obtain two signatures):

LIST:
~~xxx~~ R&D - D. Forsythe
 A. Grove
 T. Klein
 G. Moore
 R. Seeds
 E. Snow
 L. Vadasz

 M.V - H. Blume
 J. Kelley
 P. Mogensen
 G. Vashel
 M. Wilder

Acknowledgements

- ❑ Eli Harari – Founder of SanDisk
- ❑ Dick James – Chipworks/TechInsights
- ❑ Malcolm Longair – University of Cambridge
- ❑ Thomas Boone – Spin Transfer Technologies
- ❑ Shustek Center at The Computer History Museum
- ❑ Cambridge University Press

Appendix

- ❑ Enlargements of the articles in the Golden Thread timeline

Fowler-Nordheim Tunneling

Electron Emission in Intense Electric Fields.

By R. H. FOWLER, F.R.S., and Dr. L. NORDHEIM.

(Received March 31, 1928.)

Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character, Volume 119, Issue 781 (May 1, 1928), 173-181.

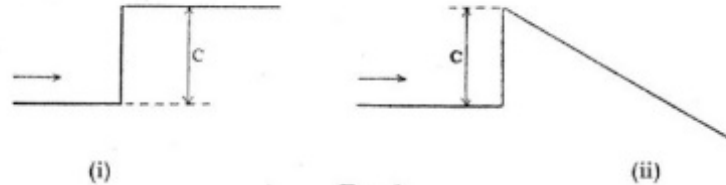


FIG. 1.

In order to study the emission through the potential energy step of fig. 1 we have only to solve the wave equations

$$\frac{d^2\psi}{dx^2} + \kappa^2 (W - C + Fx) \psi = 0 \quad (x > 0), \quad (4)$$

$$\frac{d^2\psi}{dx^2} + \kappa^2 W \psi = 0 \quad (x < 0), \quad (5)$$

Kahng and Atalla - MOSFET

United States Patent Office
3,102,230
Patented Aug. 27, 1963

Aug. 27, 1963
DAWON KAHNG
3,102,230

ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE
Filed May 31, 1960

In accordance with the present invention useful characteristics are obtained from a device of this type by arranging the associated circuitry to vary an electric field across the oxide in response to variations in voltage across the junctions. In particular, voltage regulation or amplification can be achieved by the invention.

United States Patent Office
3,206,670
Patented Sept. 14, 1965

Sept. 14, 1965
M. M. ATALLA
3,206,670

SEMICONDUCTOR DEVICES HAVING DIELECTRIC COATINGS
Filed March 8, 1960

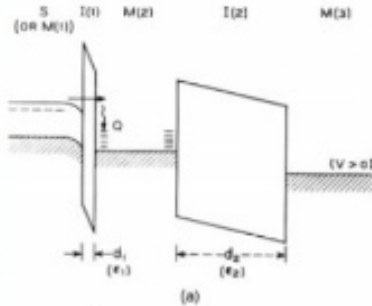
If, for example, junction 81 is biased in the forward direction and junction 83 is biased in the reverse direction by the application of an appropriate voltage from a battery B₂ connected between ohmic contacts 89 and 90, a positive bias at the oxide will induce a region of negative charge 91 which will provide a low impedance path at a predetermined value of bias applied across the oxide layer. The device can be returned to its high impedance state by removing the bias or, alternatively, by application of a negative voltage at the oxide depending on design parameters.

Kahng and Sze – Floating Gate Memory

A Floating Gate and Its Application to Memory Devices

By D. KAHNG and S. M. SZE

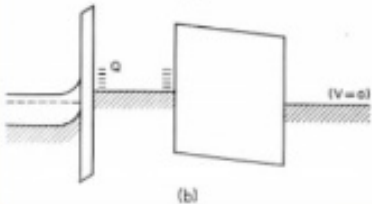
(Manuscript received May 16, 1967)



When the emission is of Fowler-Nordheim tunneling type, then the current density, j , has the form

$$j = C_1 E^2 \exp(-E_a/E), \quad (2a)$$

In conclusion, it has been demonstrated that the controlled field emission to the buried "floating" gate may be capacitively induced by pulsing the outer gate electrode. This combination can therefore be used as a memory device, with holding time as long as the dielectric relaxation time of the gate structure and with continuous nondestructive read-out capability. There seems to be no inherent reason why read-in read-out cannot be performed in a very short time, say in the nanosecond range or even shorter.



Wegener – “ON” Charge Trap Transistor

11.4 THE VARIABLE THRESHOLD TRANSISTOR, A NEW ELECTRICALLY-ALTERABLE, NON-DESTRUCTIVE READ-ONLY STORAGE DEVICE, H. A. R. Wegener, A. J. Lincoln, H. C. Pao, M. R. O'Connell, and R. E. Oleksiak, Sperry Rand Research Center, Sudbury, Mass.; H. Lawrence, Sperry Semiconductor, Norwalk, Conn.

A memory element has been developed that has the structure of a typical silicon planar p-channel enhancement insulated-gate field-effect transistor (IGFET). The information is stored by setting the threshold voltage of the IGFET to a high or low value. Interrogation is accomplished by applying a gate voltage intermediate to the threshold voltage extremes. Current will flow between source and drain if the recorded threshold voltage is less negative than the interrogating gate voltage; none will flow if the recorded threshold voltage is more negative. A high (negative) threshold voltage is written by applying a pulse of -50 v or higher for a duration of 1 msec or less between gate and substrate. A low threshold voltage is similarly obtained with positive 50 v pulse. The persistence of stored information has been demonstrated for periods of at least several months.

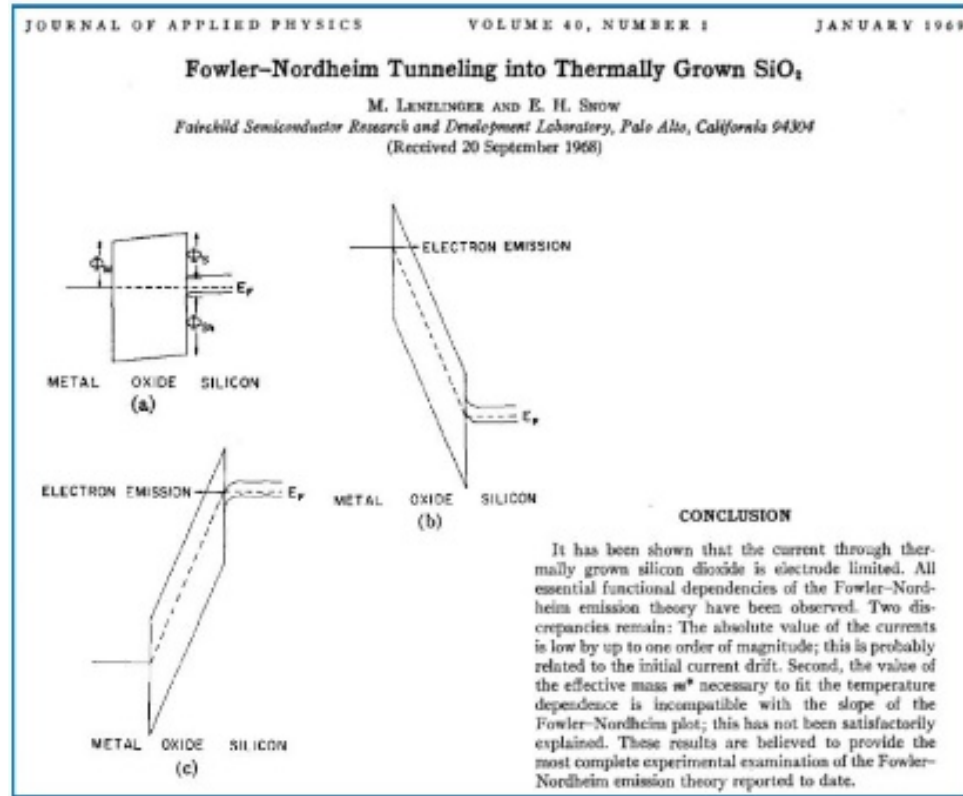
The storage mechanism will be discussed and experimental data that describe the write-in, read-out, and storage characteristics of this device will be presented. The results of its application, in various experimental circuits, including a one-by-four electrically-alterable read-only memory, will be given in conclusion.

Keshavan – “ONO” Charge Trap Transistor

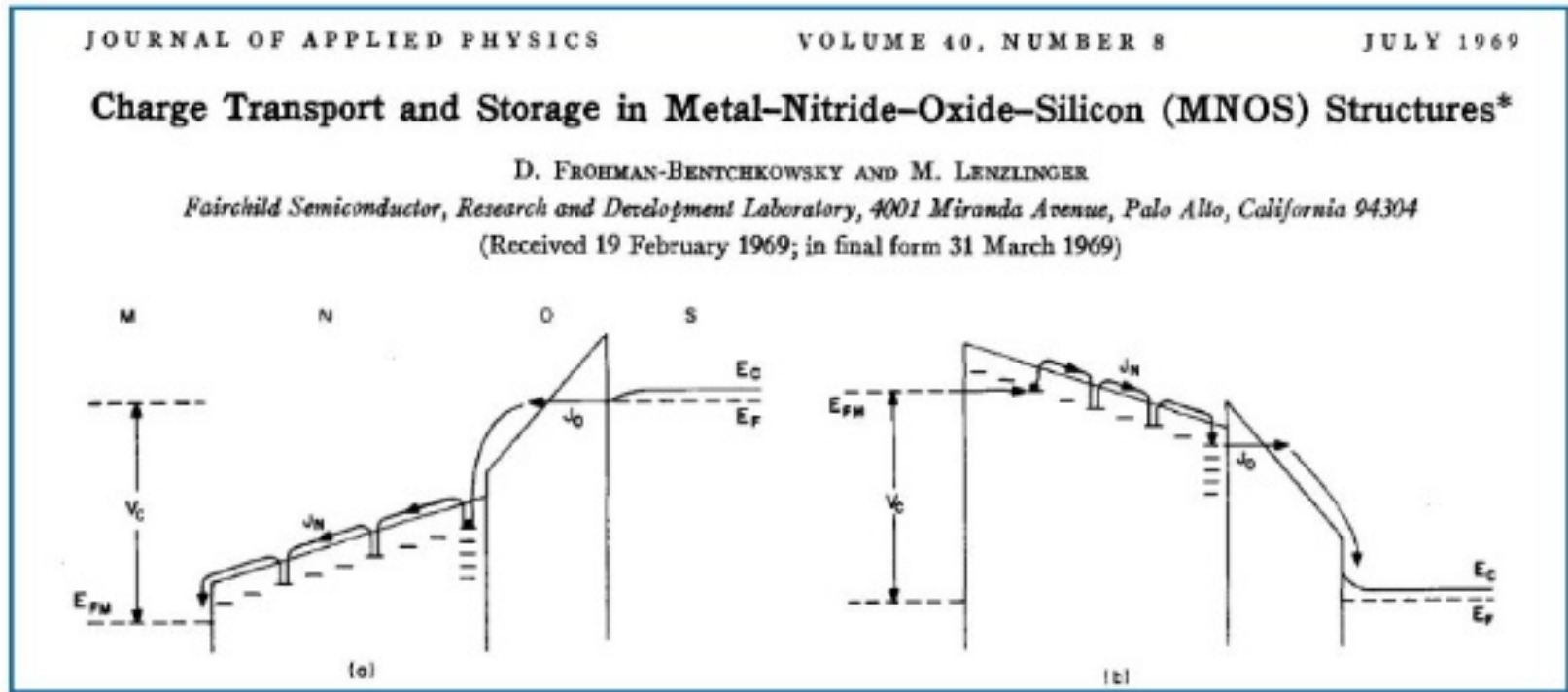
24.3 MONOS MEMORY ELEMENT, B. V. Keshavan and H. C. Lin, Westinghouse Electric Corporation, Integrated Circuit Division, Linthicum, Md.

The use of metal-nitride-oxide-semiconductor structure as a storage element was reported by Szedon at the 1967 Device Research Conference. When such a structure is used as p-channel enhancement mode device, a positive gate voltage exceeding a certain critical value changes the device into depletion mode. Later when a negative gate voltage of the order of this critical voltage is applied, the device changes back to enhancement mode. This phenomenon has been explained as electron tunneling from the semiconductor through the oxide into the traps in the nitride with a positive gate bias, and from traps into the semiconductor with negative gate bias. This can be used as a nonvolatile memory element.

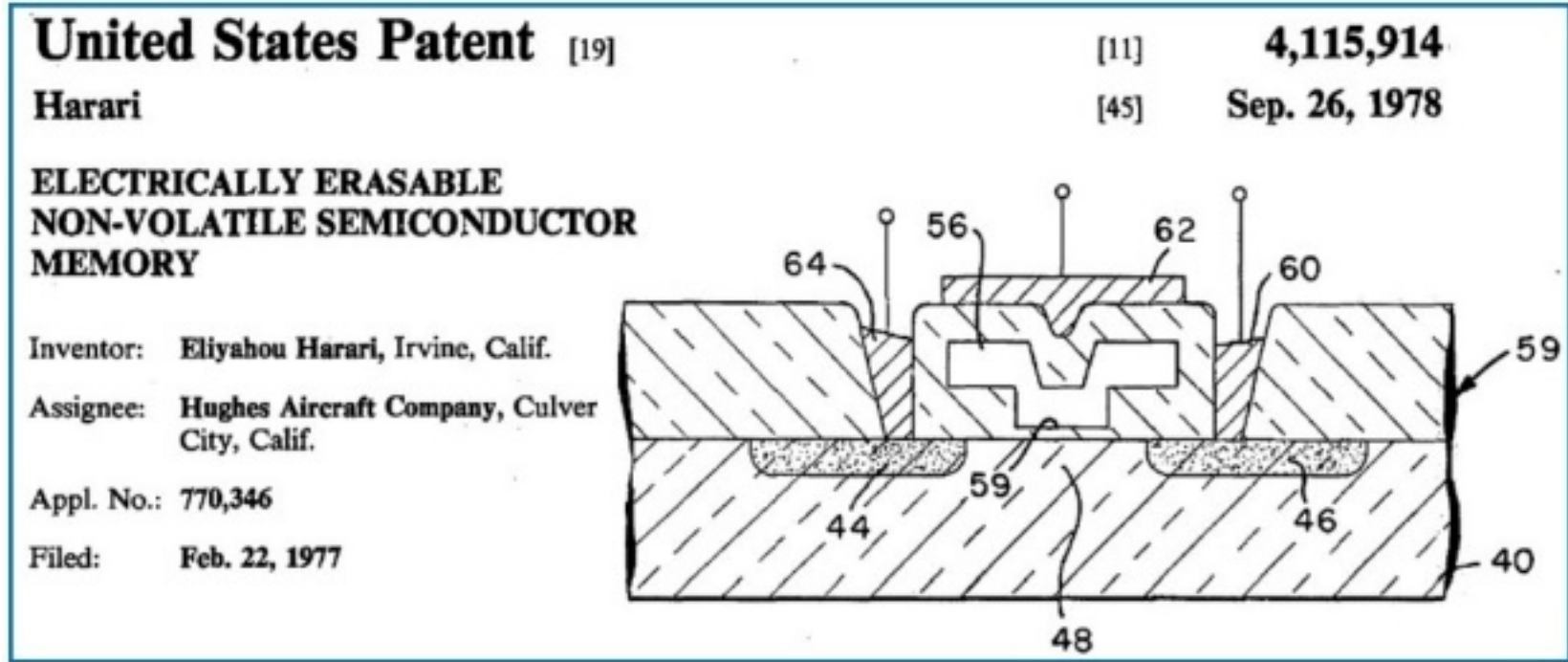
Lenzlinger – Theory of FN tunneling in SiO_2



Frohman-Bentchkowsky – Charge Trap charge transport and storage



Harari – EEPROM with tunneling

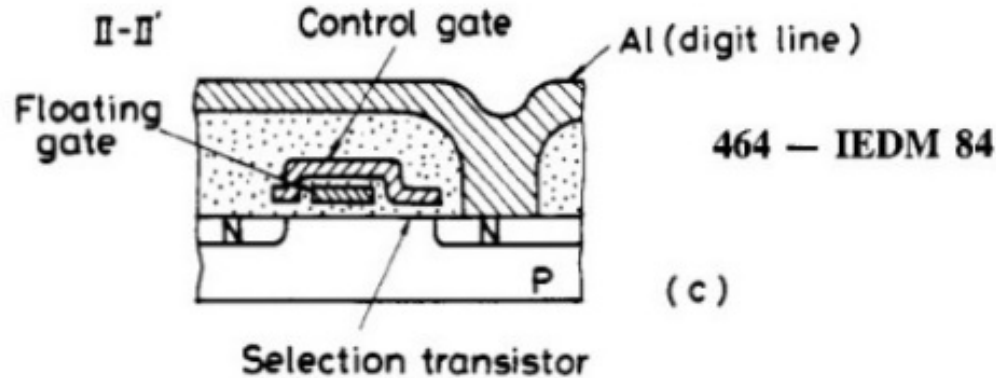


Masuoka - Flash

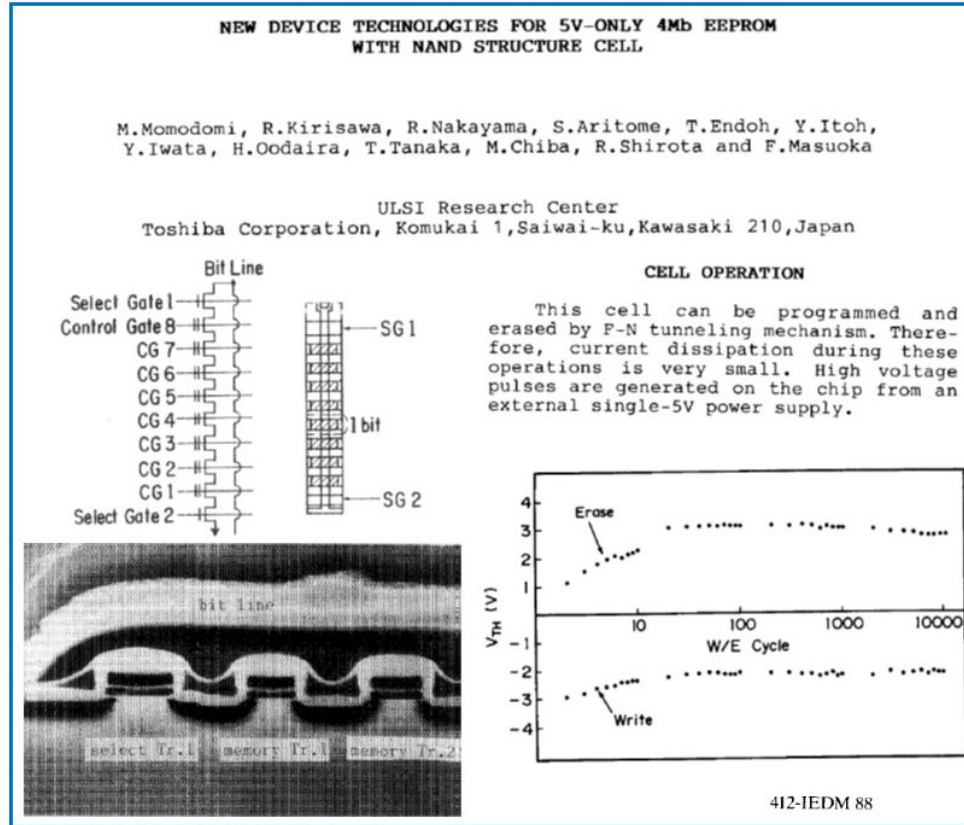
A NEW FLASH E²PROM CELL USING TRIPLE POLYSILICON TECHNOLOGY

FUJIO MASUOKA, MASAMICHI ASANO, HIROSHI IWAHASHI, TEISUKE KOMURO
and SHINICHI TANAKA

INTEGRATED CIRCUIT DIV. TOSHIBA CORP.
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Momodomi – NAND Flash (2-D)



Harari - Multibit

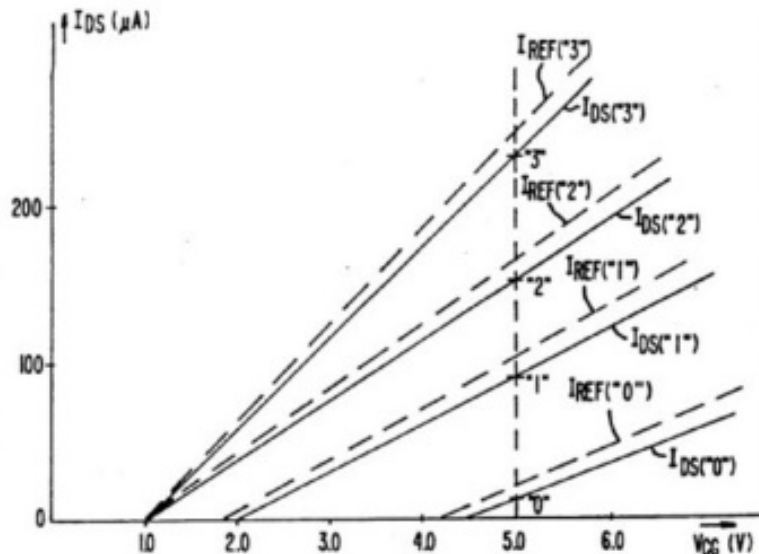
United States Patent [19]

Harari

[11] Patent Number: 5,095,344

[45] Date of Patent: Mar. 10, 1992

Structures, methods of manufacturing and methods of use of electrically programmable read only memories (EPROM) and flash electrically erasable and programmable read only memories (EEPROM) include split channel and other cell configurations. An arrangement of elements and cooperative processes of manufacture provide self-alignment of the elements. An intelligent programming technique allows each memory cell to store more than the usual one bit of information. An intelligent erase algorithm prolongs the useful life of the memory cells. Use of these various features provides a memory having a very high storage density and a long life, making it particularly useful as a solid state memory in place of magnetic disk storage devices in computer systems.



Harari – System Flash

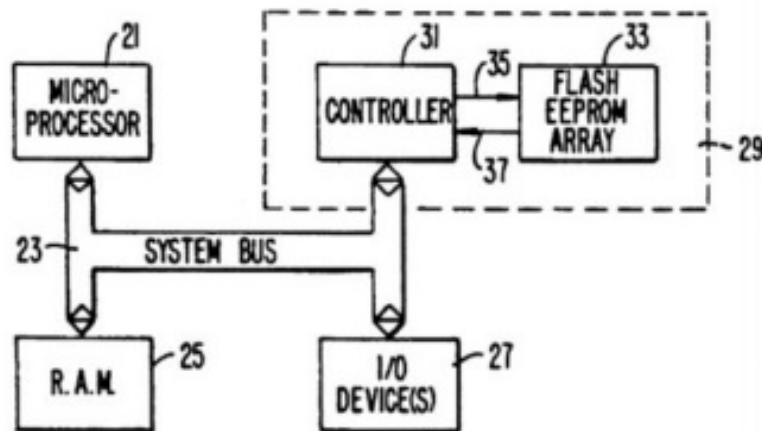
United States Patent [19]

Harari et al.

[11] Patent Number: 5,297,148

[45] Date of Patent: Mar. 22, 1994

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.



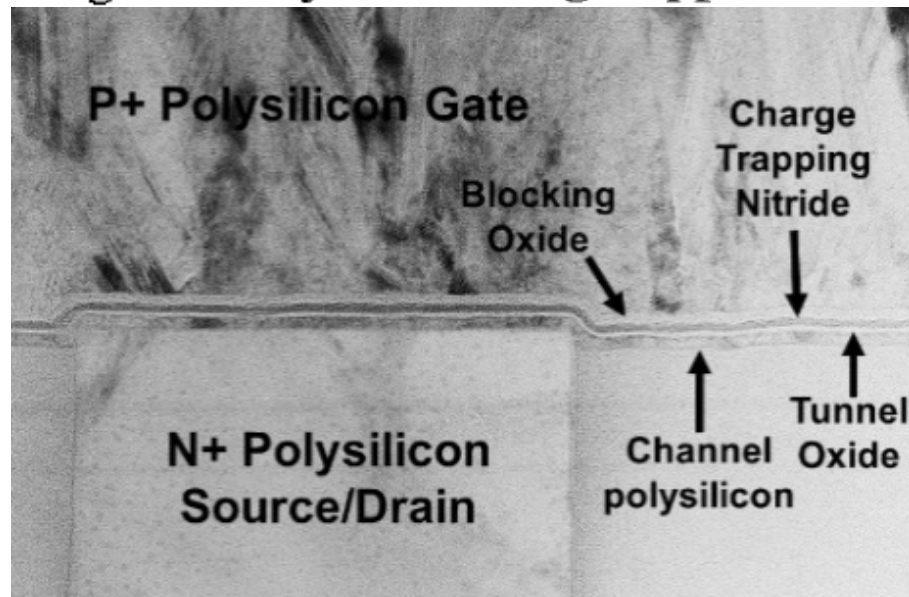
Walker – TFT SONOS

3D TFT-SONOS Memory Cell for Ultra-High Density File Storage Applications

Abstract

For the first time, a scalable, low power, deep-submicron TFT-SONOS (Thin-Film Transistor Silicon-Oxide-Nitride-Oxide-Silicon) memory cell is described with characteristics rivaling those of single crystal devices ($>10^6$ cycles, $\sim 1.6\text{V}$ window after 10 years on cycled cell at 85°C) showing the promise of 3D integration and ultra-small cell footprints. The ability to vertically stack device layers enables the current memory density record of $\sim 200\text{Mbyte}/\text{cm}^2$, set by 90nm NAND, to be surpassed.

(Keywords: TFT, SONOS, 3D, nonvolatile, memory)

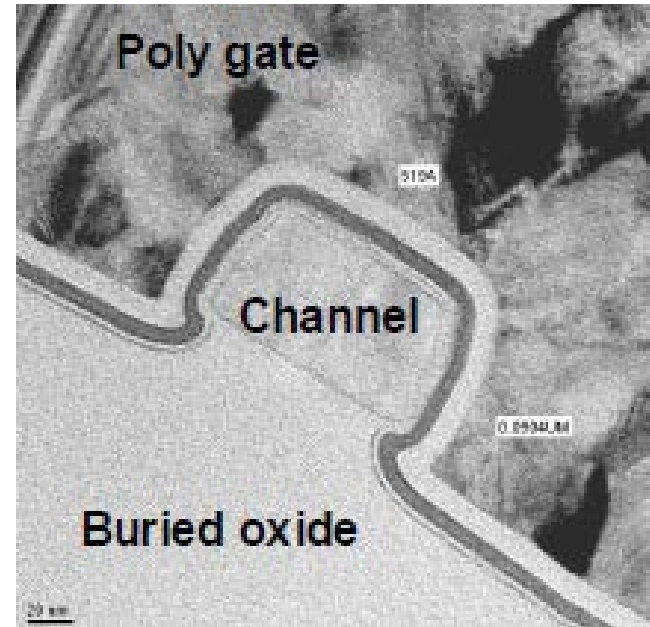


Lai – TFT SONOS NAND

A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory

Abstract

A double-layer TFT NAND-type Flash memory is demonstrated, ushering into the era of three-dimensional (3D) Flash memory. A TFT device using bandgap engineered SONOS (BE-SONOS) [1,2] with fully-depleted (FD) poly silicon (60 nm) channel and tri-gate P⁺-poly gate is integrated into a NAND array. Small devices (L/W=0.2/0.09 μm) with excellent performance and reliability properties are achieved. The bottom layer shows no sign of reliability degradation compared to the top layer, indicating the potential for further multi-layer stacking. The present work illustrates the feasibility of 3D Flash memory.

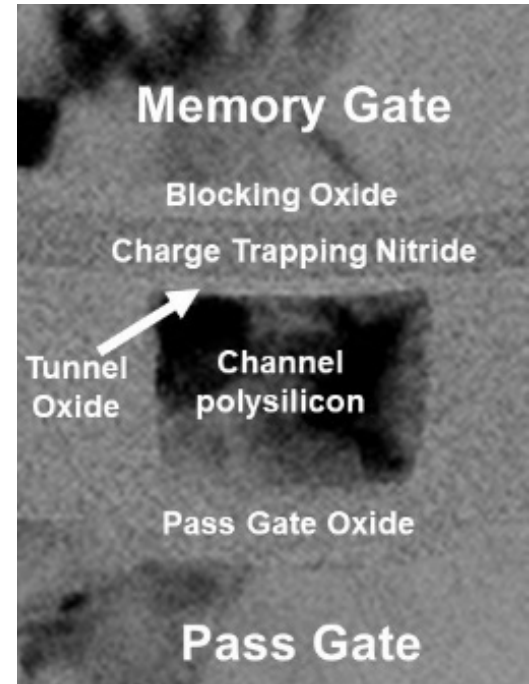


Walker – Dualgate TFT SONOS

Sub-50nm DG-TFT-SONOS – The Ideal Flash Memory for Monolithic 3-D Integration

Abstract

A revolutionary 3-D stackable sub-50nm double-gate TFT SONOS technology is presented here with series strings of up to 64 cells consisting of the smallest silicon-based TFT's to date. Read- and program-pass disturbs have been extinguished. Excellent endurance and retention are shown. Monolithic 3-D integration and scalability are ensured through close to zero source/drain diffusion. Finally, comparisons with TANOS are given.

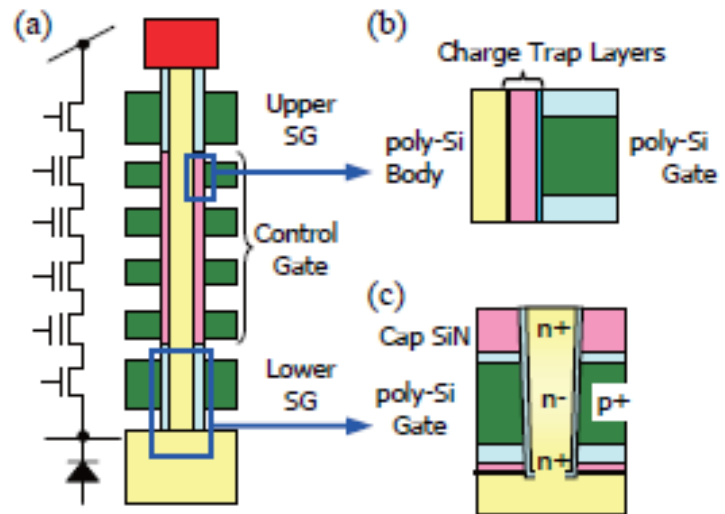


Tanaka – BiCS SONOS NAND

Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory

Abstract

We propose Bit-Cost Scalable (BiCS) technology which realizes a multi-stacked memory array with a few constant lithography steps regardless of number of stacked layer to keep a continuous reduction of bit cost. In this technology, whole stack of electrode plate is punched through and plugged by another electrode material. SONOS type flash technology is successfully applied to achieve BiCS flash memory. Its cell array concept, fabrication process and characteristics of key features are presented.



Jang – TCAT SONOS NAND

Vertical Cell Array using TCAT(Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory

Abstract

Vertical NAND flash memory cell array by TCAT (Terabit Cell Array Transistor) technology is proposed. Damascened metal gate SONOS type cell in the vertical NAND flash string is realized by a unique 'gate replacement' process. Also, conventional bulk erase operation of the cell is successfully demonstrated. All advantages of TCAT flash is achieved without any sacrifice of bit cost scalability.

