



**SDC** 18

September 24-27, 2018  
Santa Clara, CA

[www.storagedeveloper.org](http://www.storagedeveloper.org)

# **Thinking Fast & Slow: Intuition, Reasoning and Emerging Memory**

**Dave Eggleston  
Intuitive Cognition Consulting**

# Abstract

- ❑ Our human brain can be modeled as two distinctly different systems: a real time intuition system, and a background reasoning system.
- ❑ As we move into the AI compute era, Emerging Memory technologies play an increasingly important role in overcoming the limitations of DRAM and NAND.
- ❑ The commercialization of Emerging Memory will therefore accelerate our realization of powerful AI systems.

# THINKING, FAST AND SLOW



DANIEL  
KAHNEMAN

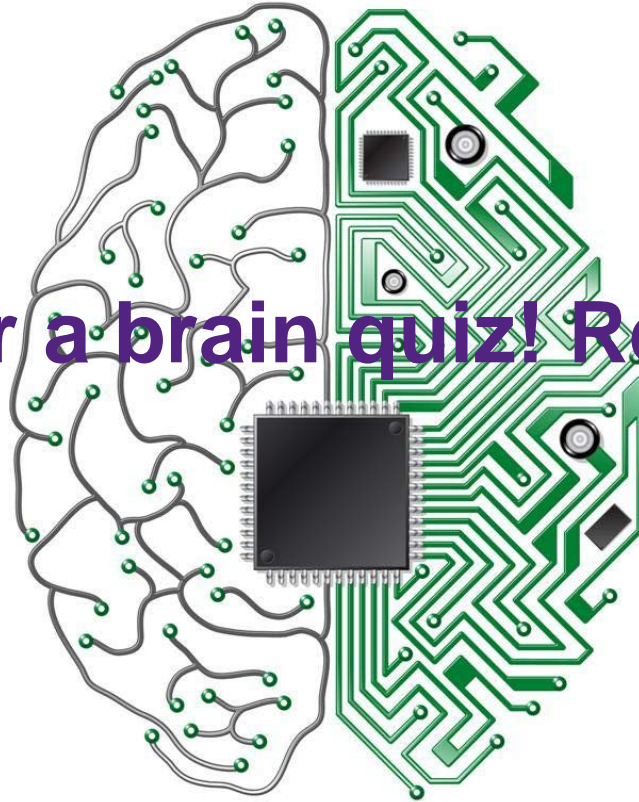
WINNER OF THE NOBEL PRIZE IN ECONOMICS

“A groundbreaking tour of the mind, and explains the two systems that drive the way we think.”

“System 1 is fast, intuitive, and emotional; System 2 is slower, more deliberative, and more logical.”

Daniel Kahneman is professor emeritus of psychology and public affairs at Princeton University.

**Time for a brain quiz! Ready?**






$$17 \times 24 = ?$$







$$17 \times 24 = ?$$

Intuition

**REASONING**





# Intuition

## System 1

- Lightning fast
- Automatic
- Real time
- Effortless
- Approximate

Edge

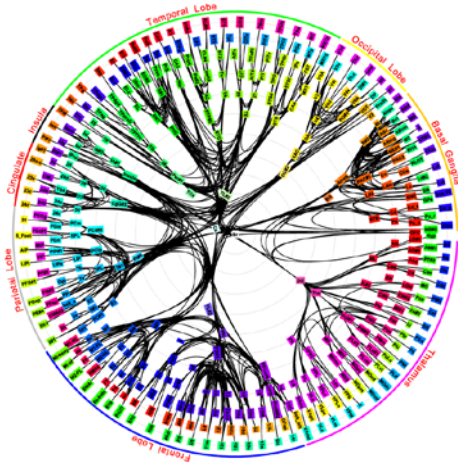
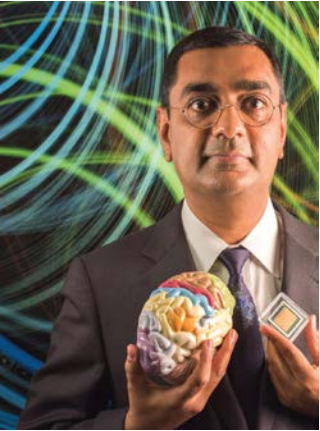
# REASONING

## SYSTEM 2

- Slow
- Interrupt driven
- Background
- Energy inefficient
- Precise

DATA CENTER

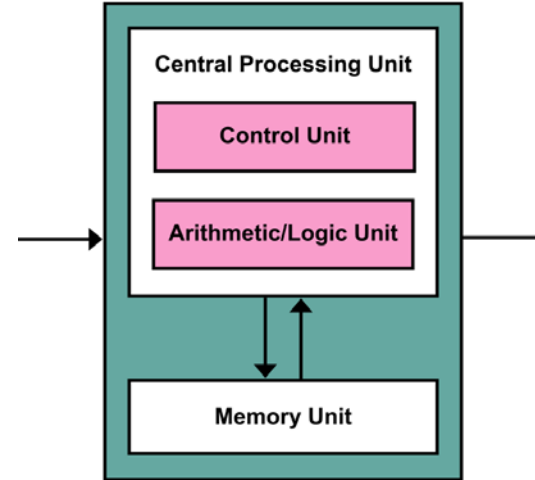
# Edge



- Non-von Neumann architecture

# Intuition

# DATACENTER



- VON NEUMANN ARCHITECTURE

# REASONING

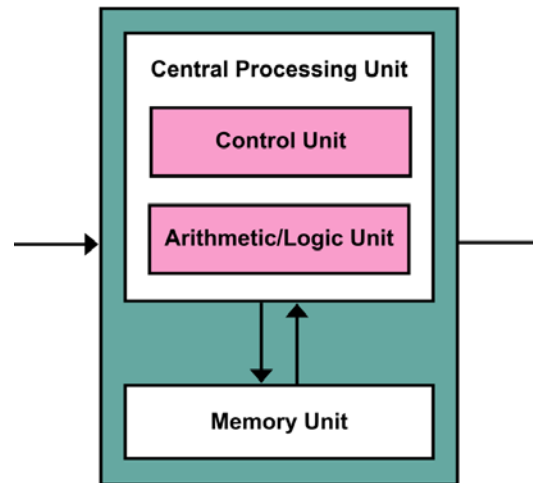
# Edge

Store Dr. Moda for now;  
we'll come back to  
discuss Edge & Intuition

□ Non-von Neumann architecture

# Intuition

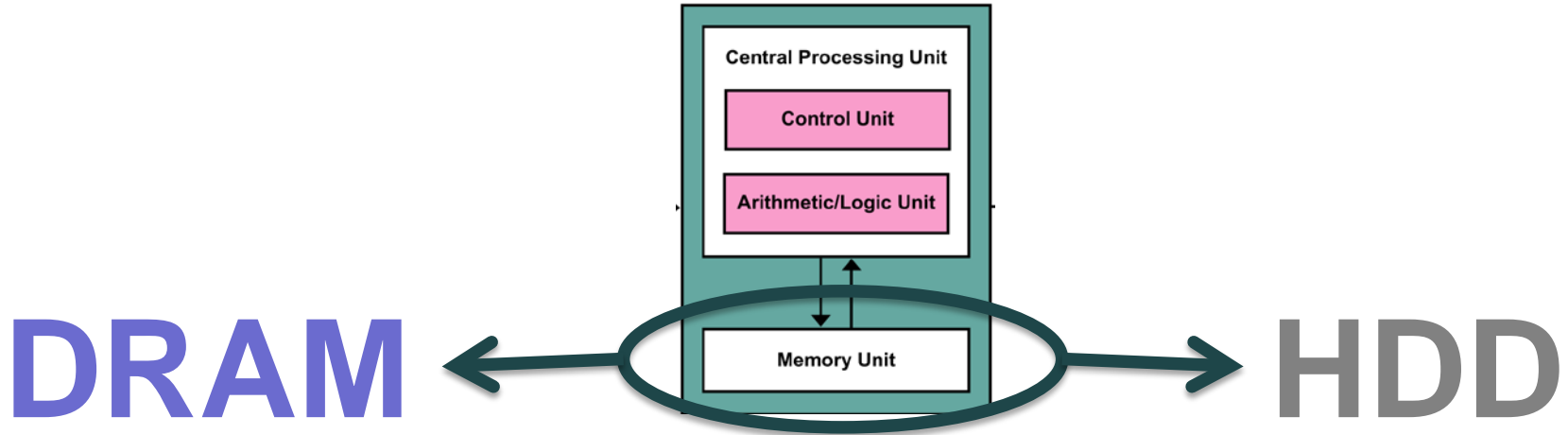
# DATACENTER



□ VON NEUMANN ARCHITECTURE

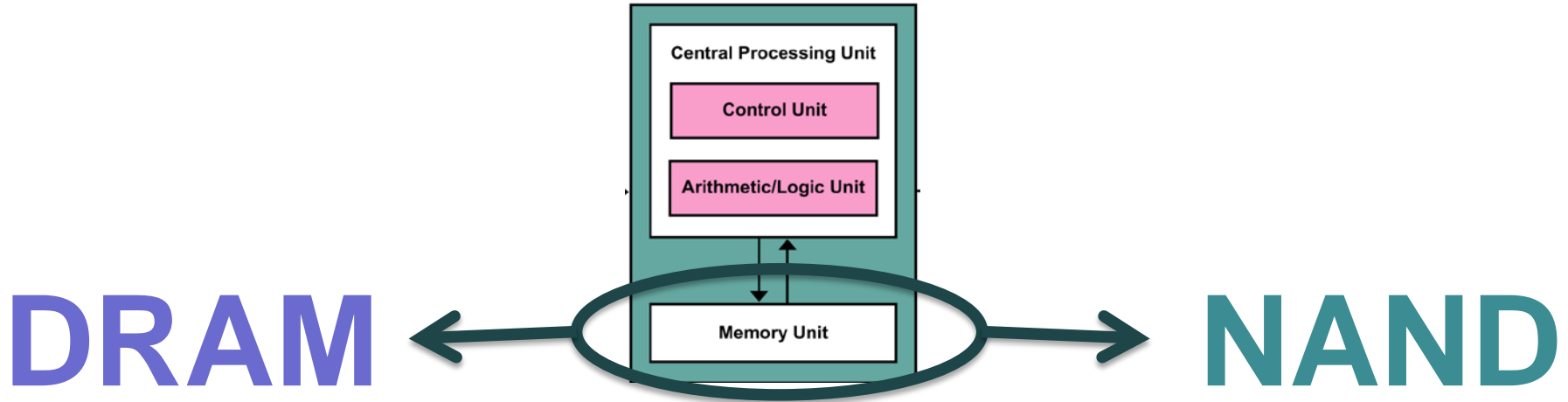
# REASONING

# REASONING



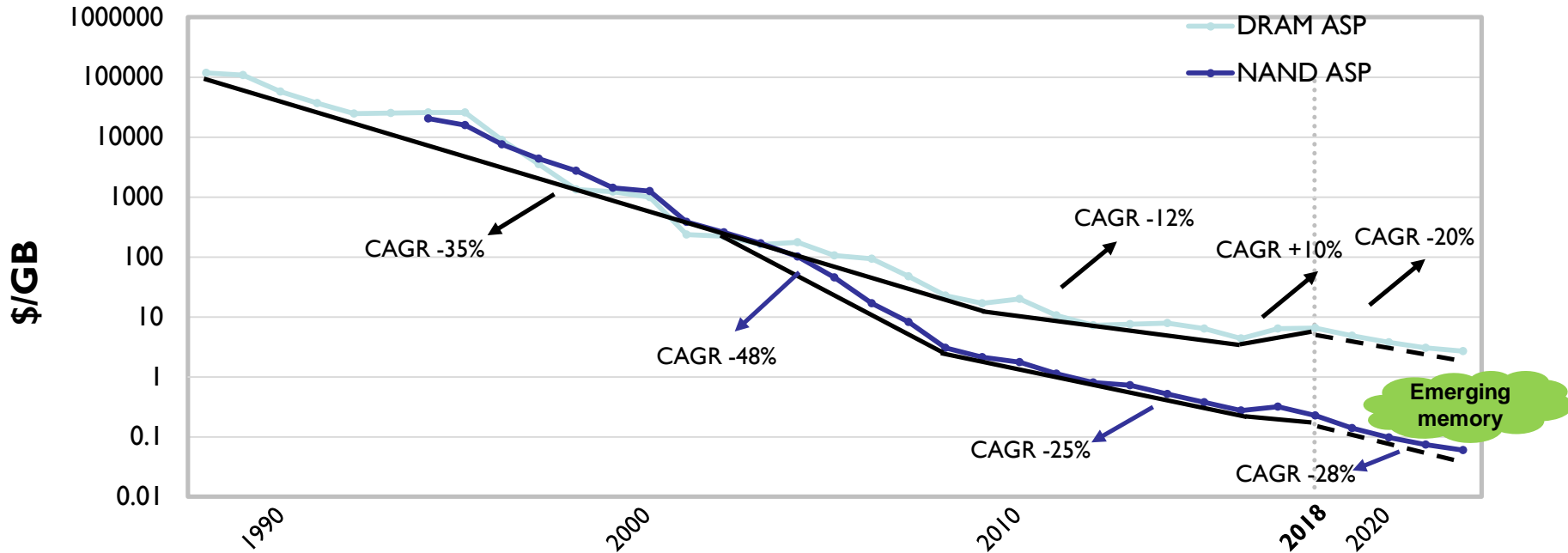
- Once upon a time, long ago...

# REASONING



□ And for a while we were happy! 😊 😊 😊

# Moore's Law is slowing – but still need low cost bits



- Cost gap between DRAM and NAND continues to increase
- Need cost-effective emerging memory to fill this gap
- Trajectory for DRAM prices for the next 5 years uncertain

# Rambus

Source: IDC

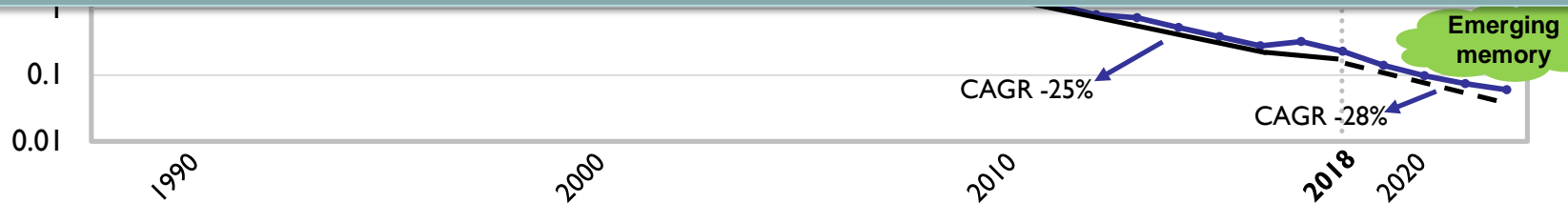


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# Moore's Law is slowing – but still need low cost bits



DRAM costs too much!



- Cost gap between DRAM and NAND continues to increase
- Need cost-effective emerging memory to fill this gap
- Trajectory for DRAM prices for the next 5 years uncertain

**Rambus**

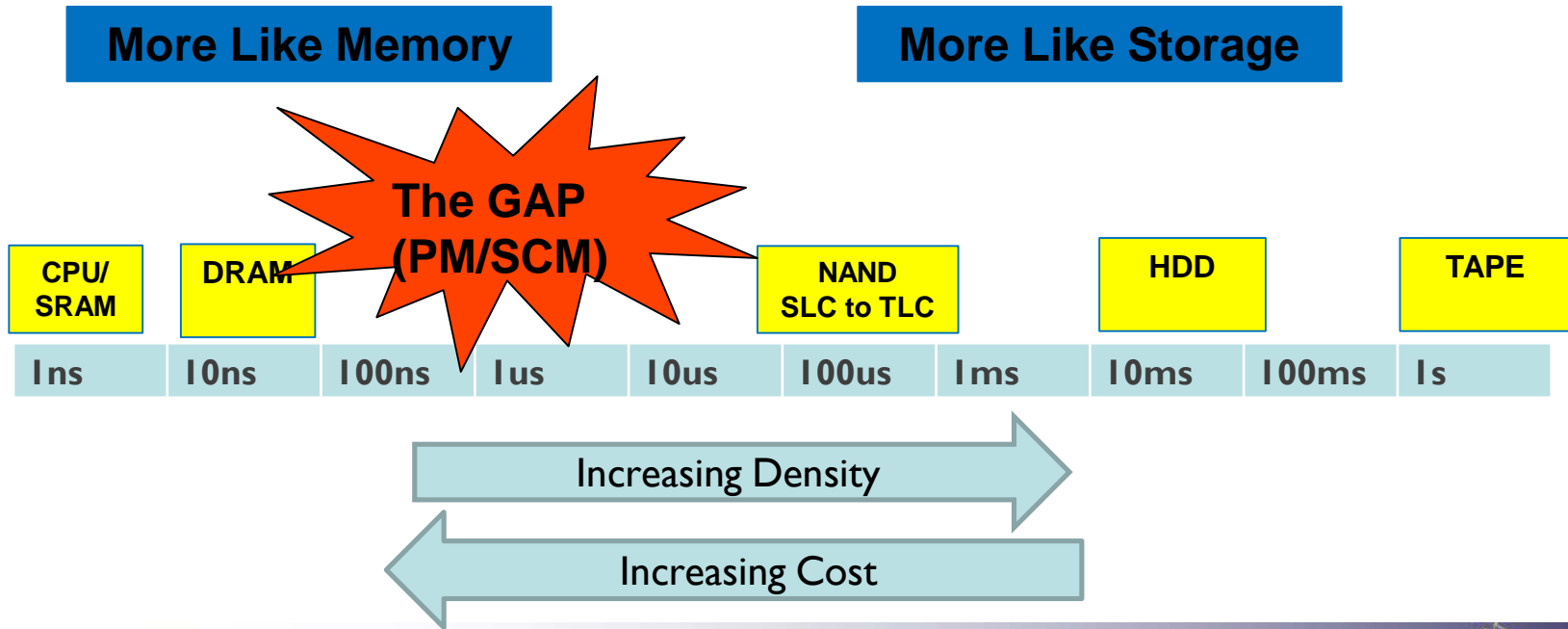
Source: IDC



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# The Latency Spectrum and Gaps ~ 2015

Source: Mark Webb, MKW Ventures Consulting, FMS 2018





# The Latency Spectrum and Gaps ~ 2015

Source: Mark Webb, MKW Ventures Consulting, FMS 2018

More Like Memory

More Like Storage

NAND is too slow!



Increasing Density

Increasing Cost



# Limitations



**DRAM**  
Cost



**NAND**  
Latency

# Emerging Memory Targets



**Cost**  
**1/3<sup>rd</sup> DRAM**



**Latency**  
**Read <1 $\mu$ s**

# Emerging Memory Targets



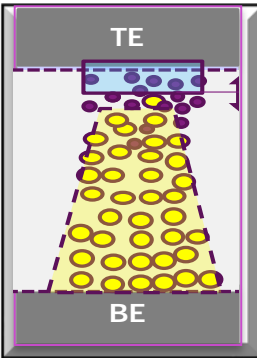

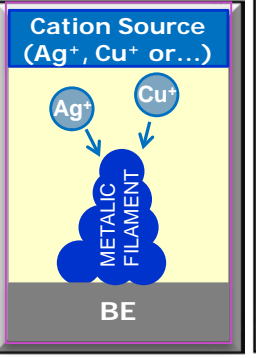
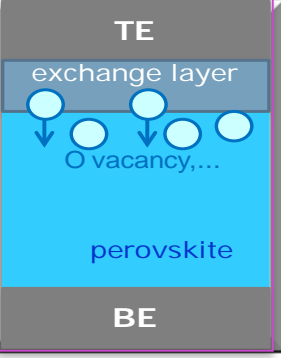
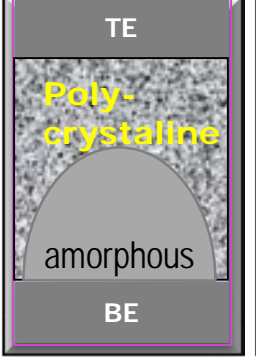

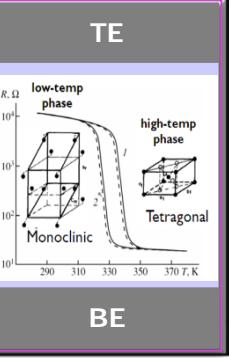
Does such an Emerging Memory even exist?

Cost  
1/3<sup>rd</sup> DRAM

Latency  
Read  $< 1\mu\text{s}$

# Switching Mechanisms

Source: M. Jurczak, imec, ISSCC 2015 Memory Forum

Filamentary ReRAM			Interfacial ReRAM	Bulk Transition		
Oxygen vacancy migration	Thermo-Chemical Fuse/ antifuse	Electro-Chemical ECM	Schottky or Tunnel Barrier	Phase Change PCM	Tunnel Magneto resistance	Electronic MIT (Mott)
						
<b>BIPOLAR</b>	<b>UNIPOLAR</b>	<b>BIPOLAR</b>	<b>BIPOLAR</b>	<b>UNIPOLAR</b>	<b>BIPOLAR</b>	<b>UNIPOLAR</b>
TMO: HfO <sub>2</sub> , TaO <sub>2</sub>	TMO: NiO <sub>2</sub>	CBRAM: Cu, Ag based	Memristor VMCO, PCMO, TiO <sub>2</sub>	Chalcogenide alloys: GST	STT RAM (CoFeB, MgO)	VO <sub>2</sub> , NbO <sub>2</sub>

# Switching Mechanisms

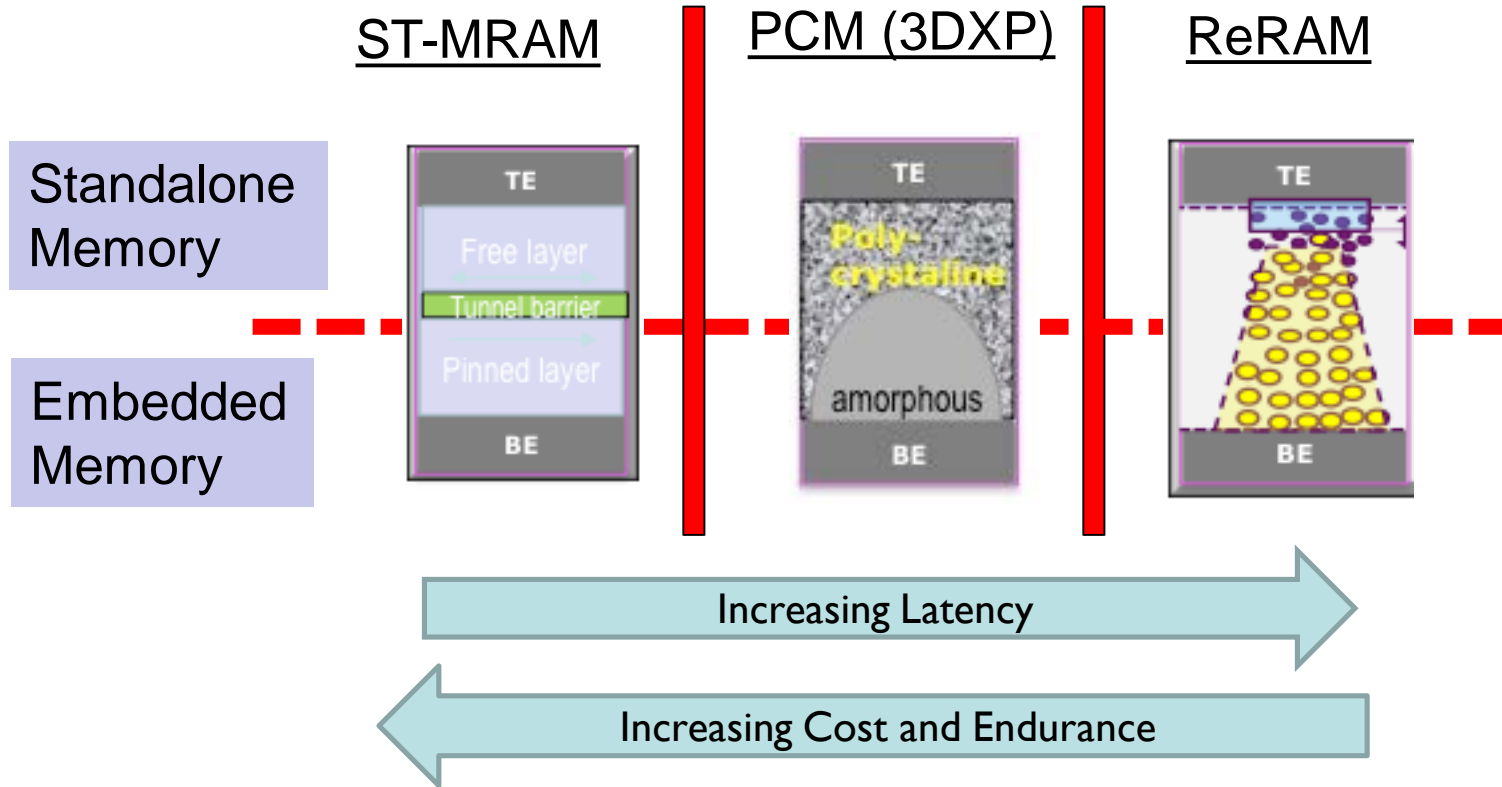
Source: M. Jurczak, imec, ISSCC 2015 Memory Forum

Filamentary ReRAM			Interfacial ReRAM	Bulk Transition		
Oxygen vacancy	Thermo-Chemical	Electro-Chemical	Schottky or Tunnel	Phase Change	Tunnel Magneto	Electronic MIT

(Too) many switching mechanisms!

<b>BIPOLAR</b>	<b>UNIPOLAR</b>	<b>BIPOLAR</b>	<b>BIPOLAR</b>	<b>UNIPOLAR</b>	<b>BIPOLAR</b>	<b>UNIPOLAR</b>
TMO: HfO2, TaO2	TMO: NiO2	CBRAM: Cu, Ag based	Memristor VMCO, PCMO, TiO2	Chalcogenide alloys: GST	STT RAM (CoFeB, MgO)	VO2, NbO2

# Classifying the What



# WHO is doing what?

## ST-MRAM



Standalone

Embedded



## PCM (3DXP)



## ReRAM

**SONY**



**Panasonic**



# Let's focus on the two shipping technologies!

## ST-MRAM



Standalone

Embedded



## PCM (3DXP)



## ReRAM

SONY



Panasonic

# WHO is doing what?

ST-M

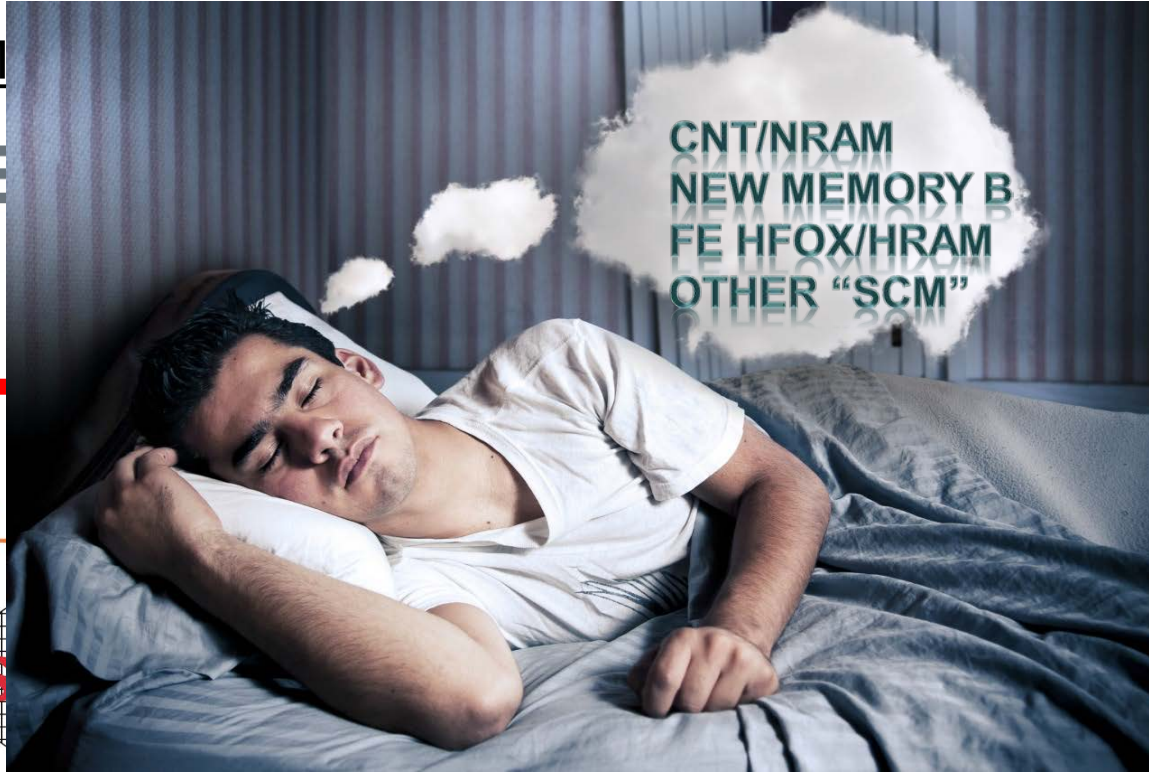


Standalone

Embedded



SAMSUNG



ReRAM

ONY



CROSSBAR

anasonic

SDC 18

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# Does such an Emerging Memory even exist?

	<b>Cost</b> 1/3 <sup>rd</sup> of DRAM	<b>Latency</b> Read < 1us
PCM (3DXP)		
ST-MRAM		



Uh oh...





That's not good.

# A Word to the Wise: ~~Replacements~~

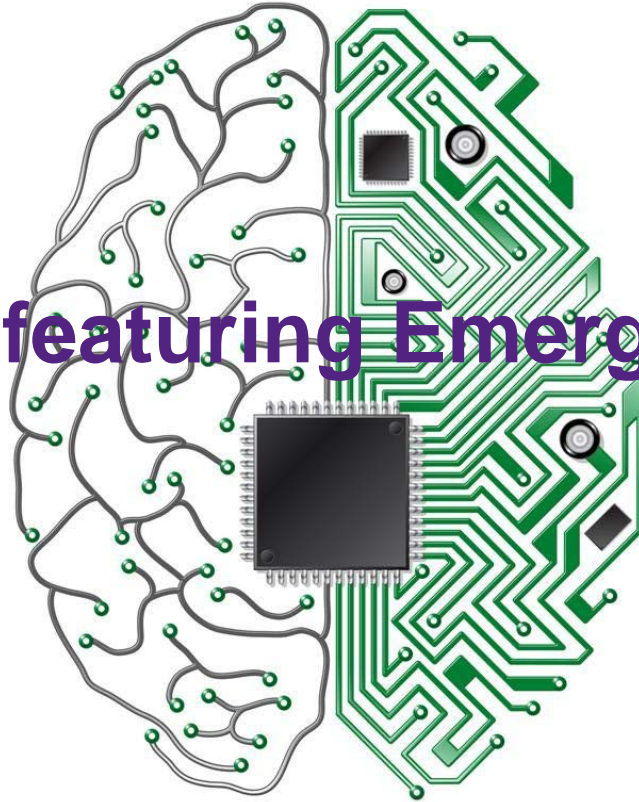
- There are no 1:1 memory replacements.
- Stop. looking. for. Them.
- Moving from DRAM+NAND world into one with Combinations of memory.



# Let's use memory combinations!

	<b>Cost</b> 1/3 <sup>rd</sup> of DRAM	<b>Latency</b> Read < 1us	<b>Winning</b> <b>Combination</b>
PCM (3DXP)			+DRAM DIMMs for reduced latency!
ST-MRAM			+NAND for reduced SSD cost!

# 2018 products featuring Emerging Memory



# FMS18: Intel Optane DIMM (3DXP on DRAM bus)

Source: Mark W. Henderson, Intel, FMS 2018



Big and Affordable Memory

128, 256, 512GB

High Performance Storage

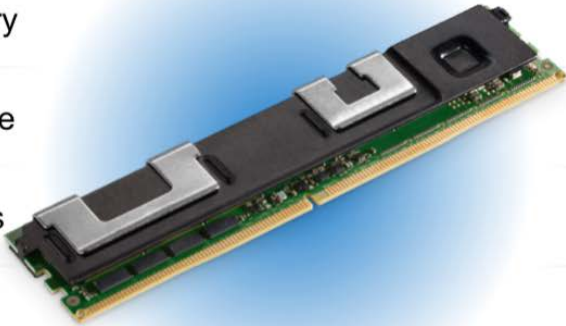
DDR4 Pin Compatible

Direct Load/Store Access

Hardware Encryption

Native Persistence

High Reliability



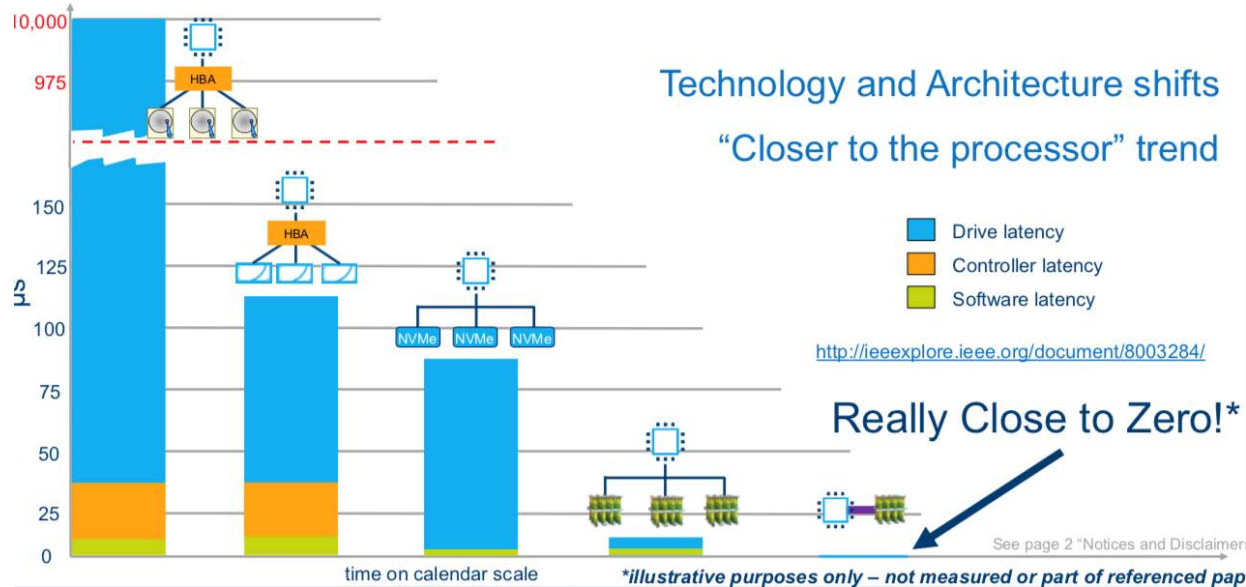
**Now shipping samples  
broad developer engagement**



# FMS18: Intel Optane DIMM (3DXP on DRAM bus)

Source: Mark W. Henderson, Intel, FMS 2018

## Technology and Architecture and Latency



- ❑ Arch, software, hardware total effort
- ❑ Reduces Optane read latency to a few  $\mu$ s
- ❑ DRAM operates as “near memory”, Optane operates as “far memory”
- ❑ Intel controlled





# FMS18: IBM Flash Core Module (MRAM+NAND)



Flash Memory Summit

## Introducing The IBM FlashCore Module

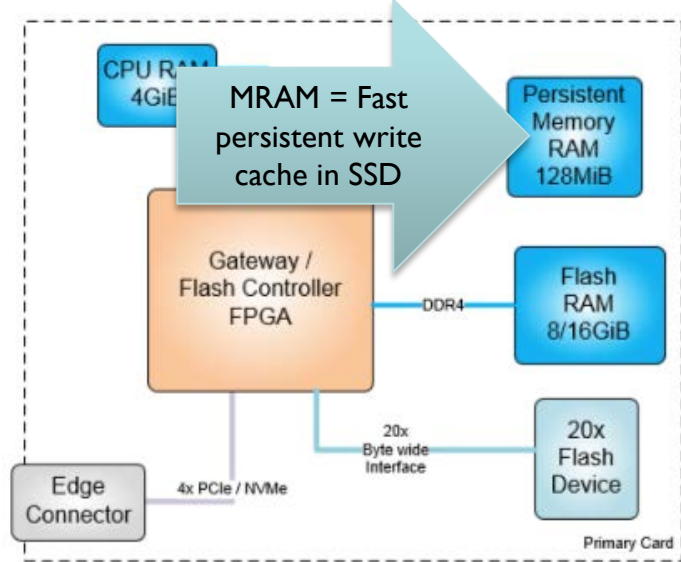
IBM FlashCore™ technology delivers key differentiators

- Built in, performance neutral **hardware compression** and **encryption**
- Using **64 layer 3DTLC NAND**
- Enterprise data **reliability**
- Cognitive Algorithms for **Wear Levelling, Health binning, Heat segregation** and media management
- Intelligent media management that **keeps settings ideal** to keep performance consistent.
- **Endurance** without latency penalty
- **FIPS 140** certification



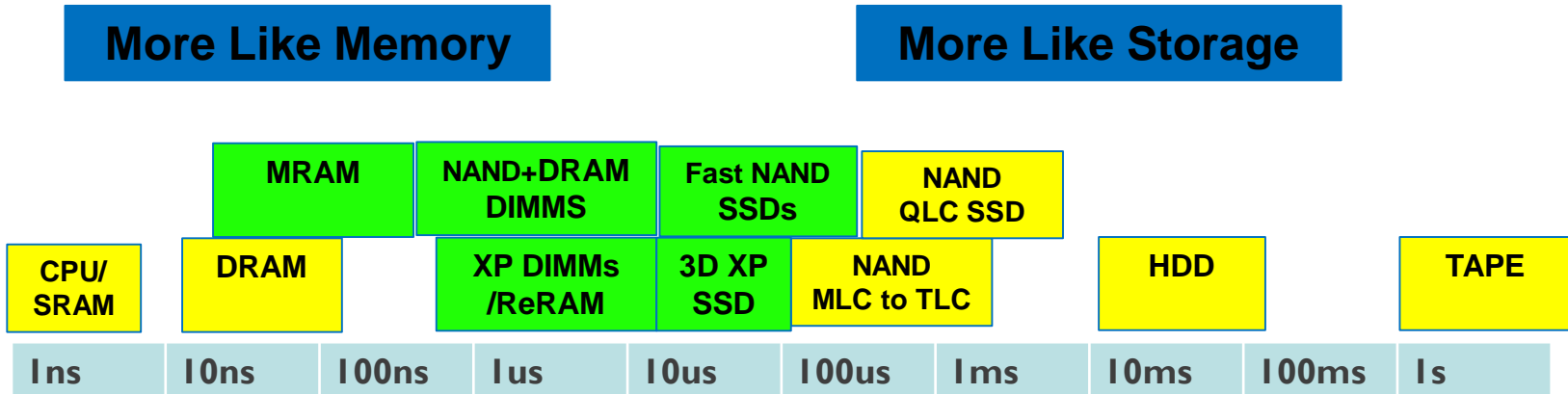
4.8TBu, 9.6TBu, 19.2TBu capacity options with up to 3:1 compression

Source: Brent Yardley, IBM, FMS 2018



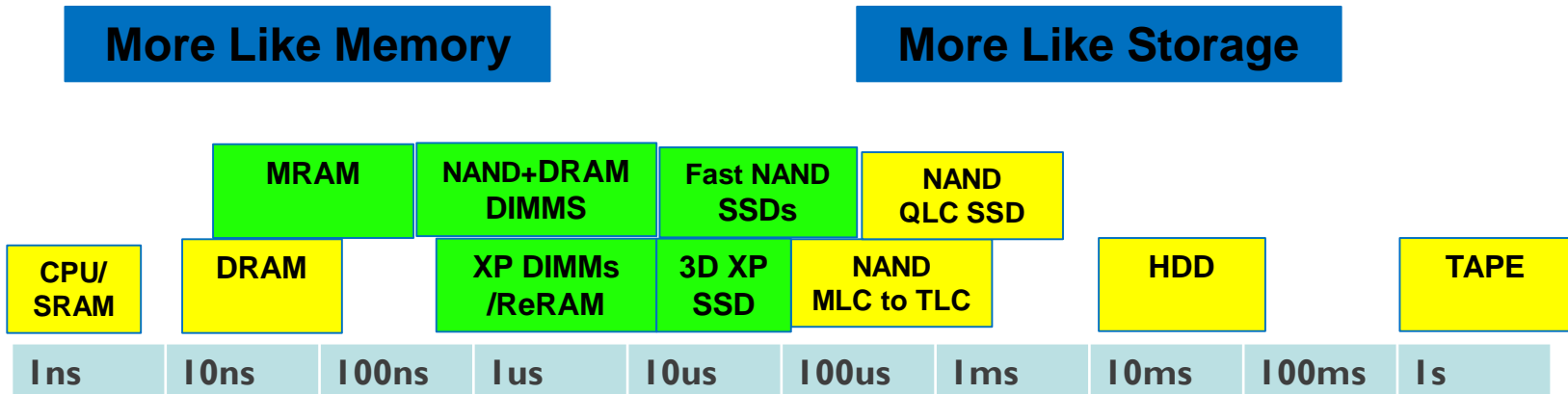
# The Latency Spectrum and Gaps ~ Now

Source: Mark Webb, MKW Ventures Consulting, FMS 2018



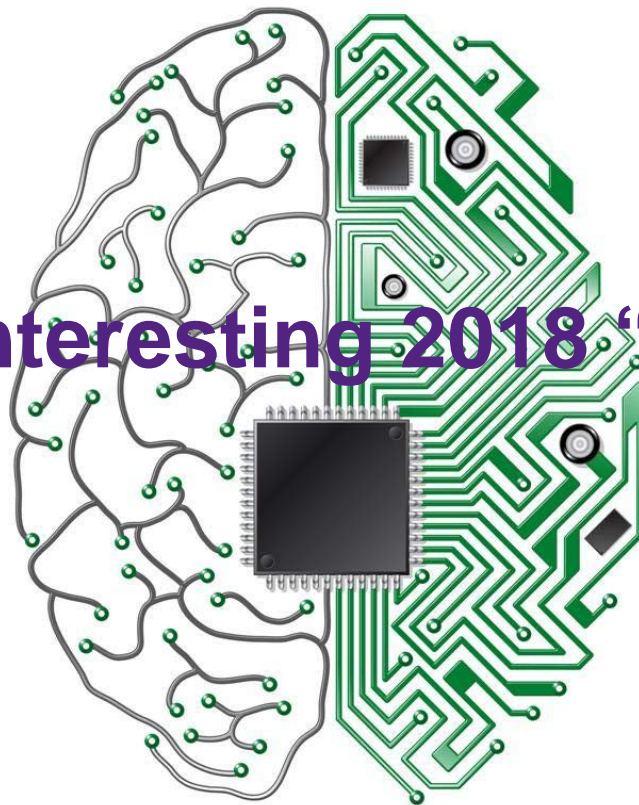
# The Latency Spectrum and Gaps ~ Now

Source: Mark Webb, MKW Ventures Consulting, FMS 2018



Several memory combinations reduce latency!

# Other interesting 2018 “stuff”



# FMS18: Toshiba XL-Flash (Low Latency SSD)

Source: Jeff Oshima, Toshiba, FMS 2018



**XL-FLASH™ from Toshiba Memory; it's COMING!**

Toshiba Memory's BiCS FLASH™ based Low Latency SLC device

- 1/10 Read latency of TLC device
- Based on proven and scalable Flash Technology
  - Better "scalability" compared to new-material NVM type memory
  - Enable optimization for various architectures (SLC/MLC, # of planes)
- Good for random IOPS and better QoS at shallow QD in an SSD

**Conventional**

**XL-FLASH™**

**TOSHIBA** **BICS FLASH™**

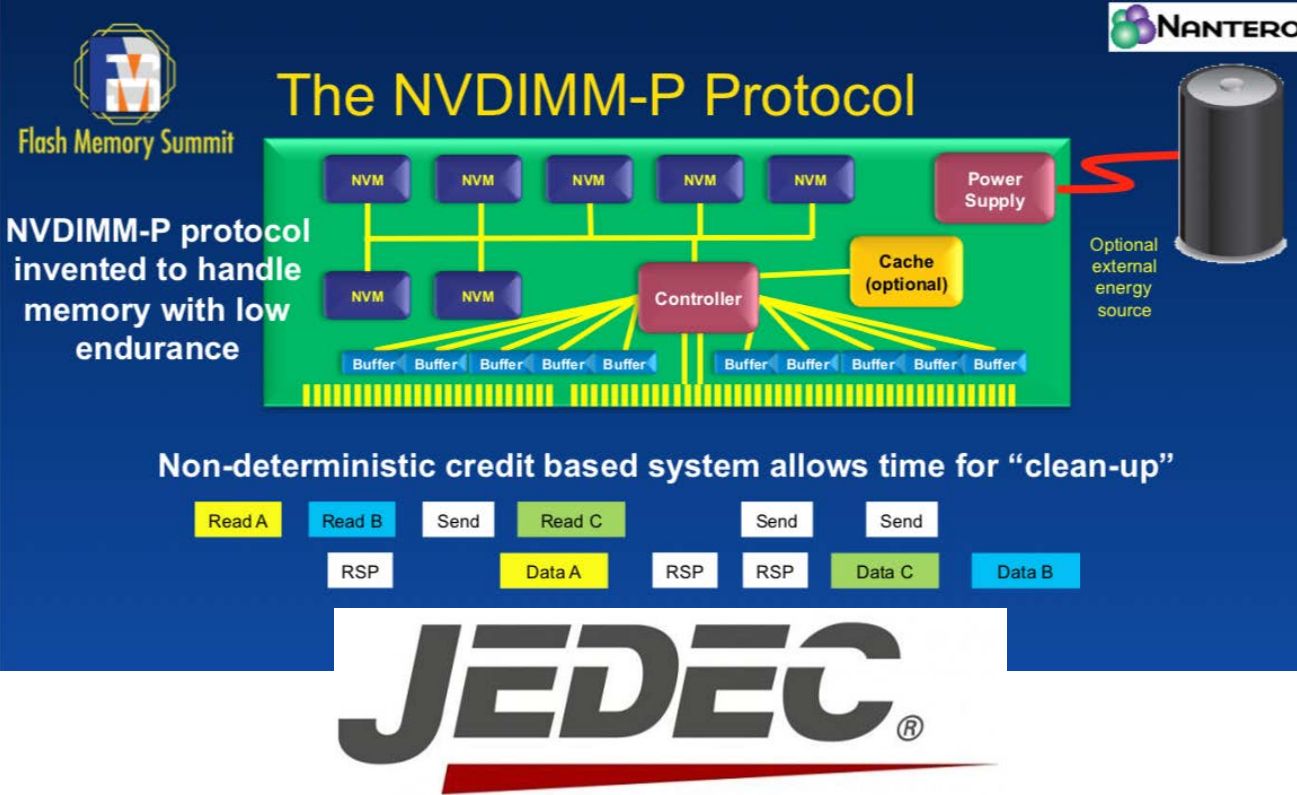
The slide features a comparison diagram between 'Conventional' and 'XL-FLASH™'. The 'Conventional' diagram shows two vertical columns representing memory planes, each with a 'WL' (word line) label at the top and a 'BL' (bit line) label on the left. The 'XL-FLASH™' diagram shows a more complex, multi-layered structure with multiple 'WL' labels and a 'BL' label, indicating a higher density of memory cells. The slide also includes icons for 'PERFORMANCE' (upward arrows) and 'EFFICIENCY' (gears), and the Toshiba logo is visible at the bottom left.

# TOSHIBA

- ❑ 10x reduced latency vs. TLC
- ❑ Still not 1us ☹️
- ❑ For low latency SSDs, attached to compute nodes
- ❑ Samsung Z-NAND, Intel Optane SSDs are competitors

# FMS18: JEDEC NVDIMM-P

Source: Bill Gervasi, Nantero, FMS 2018



- ❑ Emerging memory and DRAM on the same DDR bus
- ❑ Open standard
- ❑ Non-deterministic behavior allowed
- ❑ Will compete with Intel Optane DIMMs
- ❑ Backed by all major memory companies

# Summary: Your 2018 SSD/DIMM Watch List

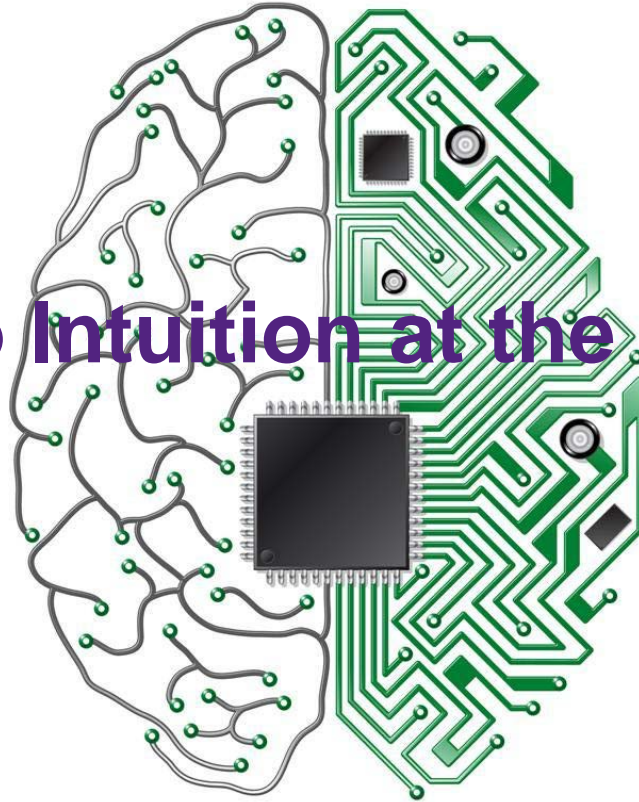
- ❑ Everspin MRAM in low latency SSDs
- ❑ Intel 3DXP in lower cost server Optane DIMMs
- ❑ Toshiba XL NAND in lower latency SSDs
- ❑ JEDEC NVDIMM-P in open standard DIMMs



**TOSHIBA**

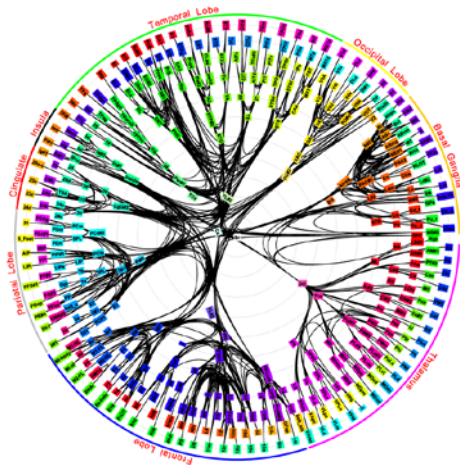
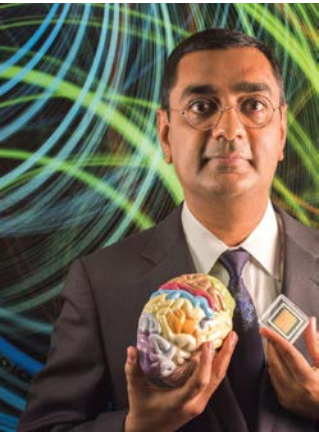


# Back to Intuition at the Edge!





# Edge



- ❑ Non-von Neumann architecture

## Intuition

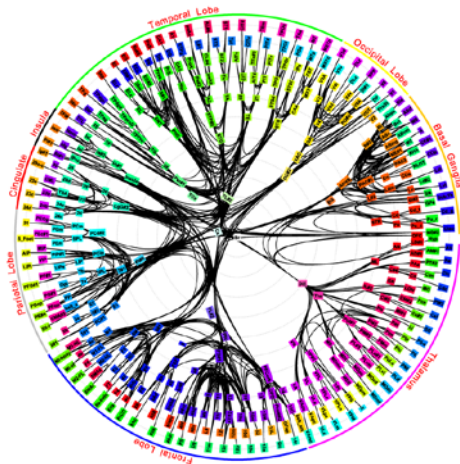
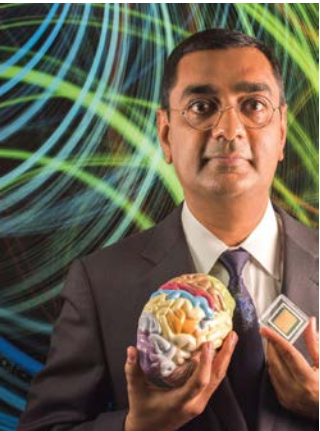
# DATACENTER

Let's talk about Intuition  
at the Edge now!

- ❑ VON NEUMANN ARCHITECTURE

## REASONING

# Edge



- Intuition system in the human brains use <20 watts of power
- Using von-Neumann architecture for Intuition >20 Gigawatts!
- Highly networked, local compute nodes
- Trained neural nets (NN) perform lightning fast intuition
- Embedded Emerging Memory used to hold weights inside NN
- Sum the weights using analog combine
- Most efficient implementation is analog memory (6+ levels per cell)
- Doesn't require 7nm/5nm process!

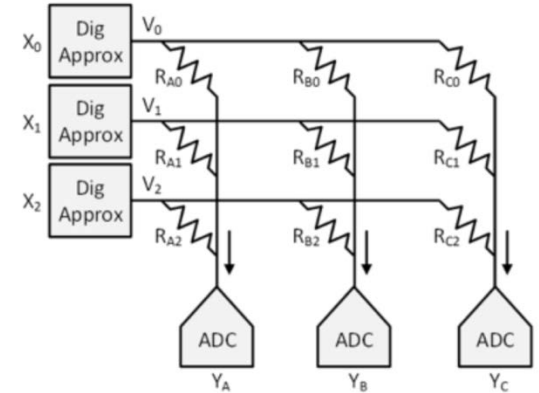
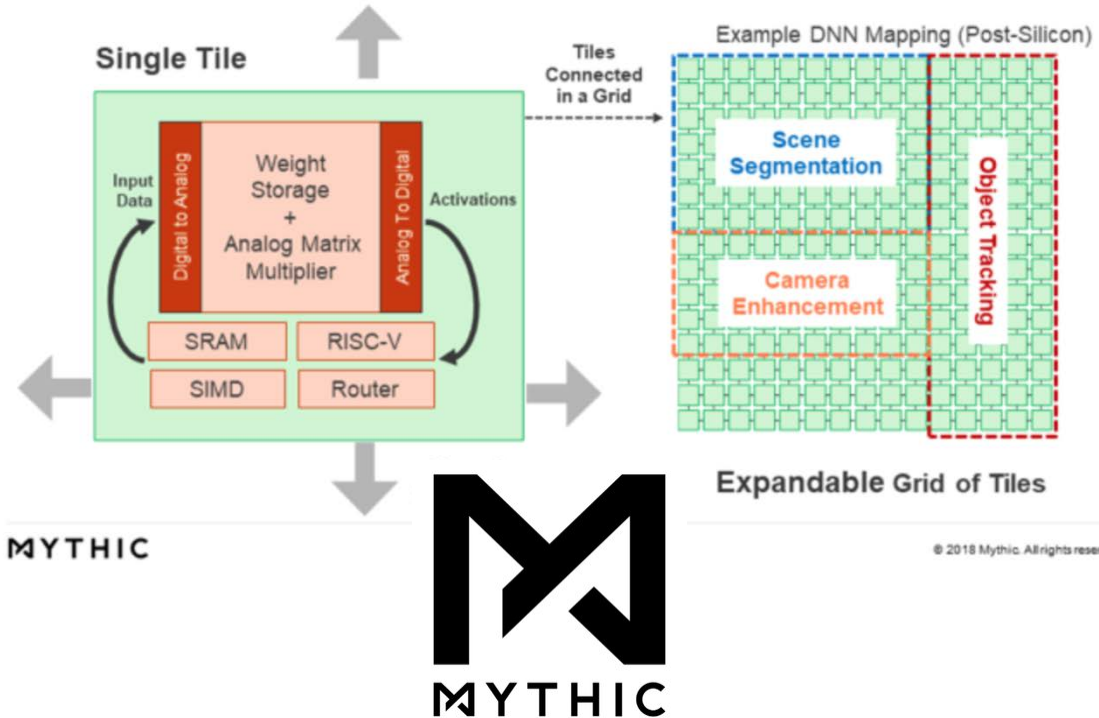
- Non-von Neumann architecture

# Intuition

# Hot Chips 2018: Edge Intuition SoC

Source: Dave Fick, Mythic, Hot Chips 2018

## Mythic Mixed-Signal Computing

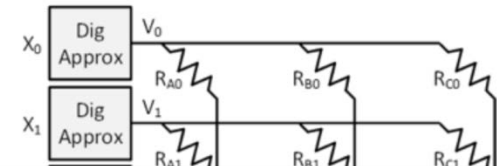
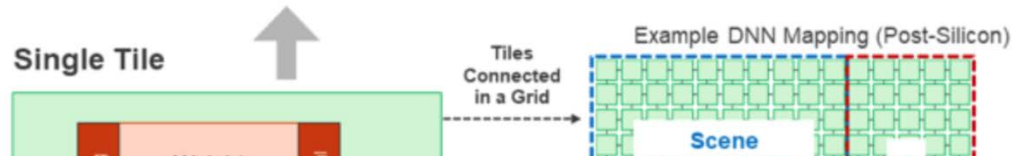


- Mythic currently uses embedded NOR Flash in analog mode to hold weights

# Hot Chips 2018: Edge Intuition SoC

Source: Dave Fick, Mythic, Hot Chips 2018

## Mythic Mixed-Signal Computing



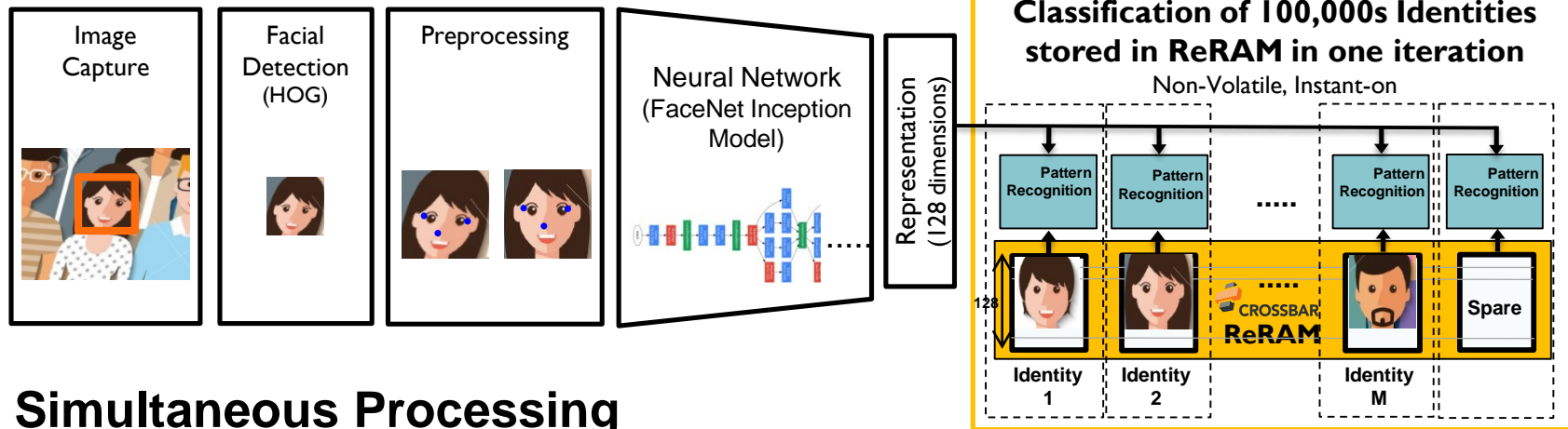
Lightning fast, low power, trained NN, analog memory



- Mythic currently uses embedded NOR Flash in analog mode to hold weights

# FMS18: Future Edge Intuition SoCs use ReRAM?

Source: Hagop Nazarian, Crossbar, FMS 2018



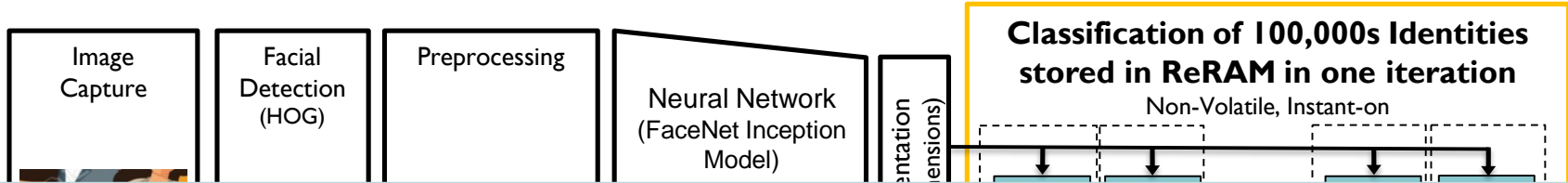
## Simultaneous Processing with Deterministic Performance

- Parallel comparison against all identities
- If no match, new identity created (learning)
- Classification performed in one cycle independent of number of identities



# FMS18: Future Edge Intuition SoCs use ReRAM?

Source: Hagop Nazarian, Crossbar, FMS 2018



## Embedded ReRAM as analog memory in NN

### Simultaneous Processing with Deterministic Performance

- Parallel comparison against all identities
- If no match, new identity created (learning)
- Classification performed in one cycle independent of number of identities

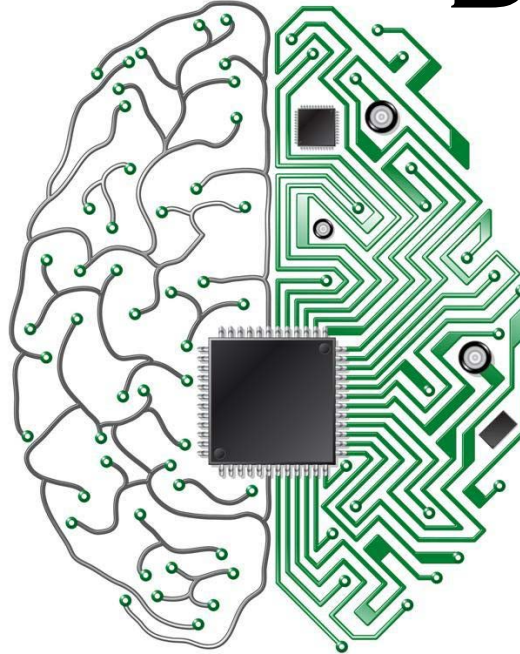


**CROSSBAR**

# Why do I care? What is Emerging Memory enabling for AI?

## Edge

- ❑ Analog memory in NN
- ❑ Lightning fast intuition at low power



## DATACENTER

- ❑ TBs of memory
- ❑ Better reasoning, based on more data

# Why do I care? What is Emerging Memory enabling for AI?

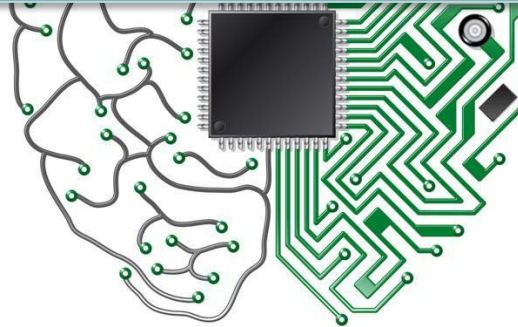
## Edge

## DATACENTER



## Emerging Memory accelerates AI!

- Lightning fast intuition at low power



- Faster reasoning, based on more data



# Take-away points:

- ❑ Your brain has two distinct systems
- ❑ Reasoning system needs reduced latency and cost
- ❑ There are NO 1:1 memory replacements
- ❑ Emerging memory combos with NAND and DRAM
- ❑ Intuition system needs new architecture and low power
- ❑ Emerging memory utilized as analog weight in neural nets
- ❑ Emerging memory accelerates AI systems

# Register NOW for SNIA 2019 PM Summit!



<https://www.snia.org/events/persistent-memory-summit/persistent-memory-summit-2019-registration>

The logo for SDC 18, featuring the letters 'SDC' in a large, bold, white font, with the number '18' inside a white circle to the right. The background is dark blue with a white geometric line pattern on the left side.

SDC 18

September 24-27, 2018  
Santa Clara, CA

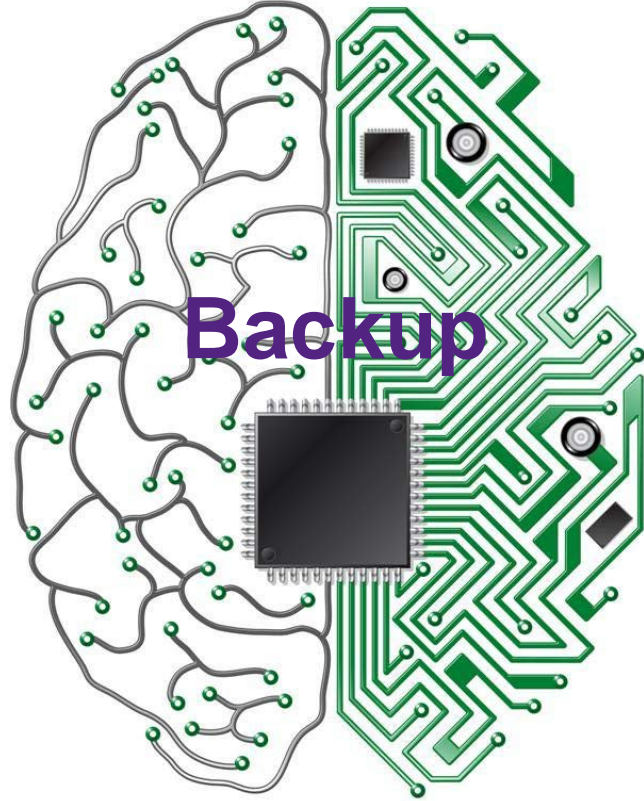
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LinkedIn:  
[linkedin.com/in/deggleston/](https://www.linkedin.com/in/deggleston/)





Backup



# Talk Outline

1. Demonstrate the human brain has two distinct systems
2. Discuss the best fit compute architecture to model each AI system
3. Articulate how DRAM and NAND are applied to the compute architectures
4. Identify the key limitations of DRAM and NAND
5. Present and classify some Emerging Memory alternatives
6. Discuss the Emerging Memory system enhancements
7. Identify who is doing what (by when) in the Emerging Memory landscape
8. Articulate the unique challenges in realizing an AI intuition system
9. Propose how Emerging Memory may solve some intuition problems
10. Point to the future of AI systems based on Emerging Memory