Emerging Trends in Computer Architecture

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A Leading Data Infrastructure Company

PORTFOLIO BREADTH

TECHNOLOGY ENGINE
~14K active patents

GLOBAL SCALE
~62K employees worldwide

CUSTOMER VALUE

Silicon-to-System Innovation and Engineering

3D NAND, Head & Media, Test and Packaging

Storage Devices
(controllers, firmware, mechanical, packaging, testing)

Storage Platforms
(electrical and mechanical, firmware and diagnostics)

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Data Creation Growing Exponentially

By 2023, >90% of Data Created will be Generated by Machines

Insatiable Growth in Data
Driven By Explosion in Big Data Analytics & Machine-Learning

Total Stored Data (EB)

- Flash SSD
- HDD

Data Center Only (EB)

- HDD

70% HDD

Exabyte = 1,000,000,000,000,000,000 Bytes

Source: WDC Analysis

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Hard Disk Drive Technology

Recording Head
- Ceramic Wafer
- Head Wafer
- Row
- Slider
- Air-Bearing Surface (ABS)

Recording Media
- Metal or Glass Disk Substrates
- Media Deposition
- Finished Platter

Mechanical Components
- Mechanical Base
- Head-Gimbal Assembly (HGA)
- Head-Stack Assembly (HSA)
**Conventional Perpendicular Recording**

**Diagram Description:**
- **Read Head:** Points towards the recording media.
- **Write Head:** Points away from the recording media.
- **Recording Media:** Composed of layers:
  - Hard Magnetic Recording Layer
  - Exchange Break Layer
  - Soft Underlayer
- **Old Data** and **New Data** areas are indicated.
- **Magnetization:**
  - into the plane
  - out of the plane
- **Readback Signal Voltage:**
  - Detected Data: 1 0 1 1 1 0 0 1 1 0 1 0 0 1 1 0
- **Energy Barrier:**
  - Magnetostatic Energy
  - Single Grain
- **Magnetization Angle:**
  - Range from -90 to 90 degrees

**Graphical Elements:**
- Track Width
- Fly Height
- Magnetostatic Energy vs. Magnetization Angle
- Single Grain Energy Barrier

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Energy-Assisted Magnetic Recording

Heat-Assisted Magnetic Recording (HAMR)

- Read Head
- Write Head
- Near-Field Transducer (NFT)
- Ordered L10 FePt
- Recording Media

Microwave-Assisted Magnetic Recording (MAMR)

- Read Head
- Write Head
- Spin-Torque Oscillator (STO)

Graph:
- Coercivity vs. Temperature
  - Heating
  - Cooling
  - Head Field
  - Write

Layers:
- Perpendicularly Magnetized Layer
- Field Generation Layer (FGL)
- Layer with Perpendicular Anisotropy

Recording Media:
- Ordered L10 FePt

Heating-Assisted Magnetic Recording
- Microwave-Assisted Magnetic Recording (MAMR)
Shingled Magnetic Recording

• Write overlapping tracks like shingles on a roof.
• Requires an indirection system to manage data placement.
• Introduced in 2015.
• Linux® Kernel modified to support.
3D NAND Flash

Industry trend: more layers, more bits per cell, optimization for either speed or cost.
SMR HDDs consist of regions (zones) in which the tracks are overlapped.
Within each zone, you can only write sequentially.

NAND die are composed of erase blocks, consisting of many pages.
Within each erase block, pages are usually written sequentially.
Zoned Data Access Architecture

Zoned Architecture

Interface Standards

SMR HDDs
Zoned Block Commands (ZBC) interface in SAS and Zoned ATA Commands (ZAC) interface for SATA.

SSDs
Zones Namespaces (ZNS) defined in NVMe TP4053, expected to be finalized later this year.
Emerging Non-Volatile Memories

- PCM (Phase Change and OTS)
- MRAM (Magnetic Tunnel Junction)
- CBRAM (Cation (Cu, Ag Ion) Filament)
- OxRAM (Anion (Oxygen Ion) Filament)
- PCMO (Anion (Oxygen Ion) Migration)
- CERAM (Electronic State (Mott) Transition)
- CNT (Carbon Nanotubes)

Flash Memory
Three-Terminal Variable Threshold Switch

Dynamic RAM
Charge Stored on Capacitor

Emerging Non-Volatile Memories
Two-Terminal Variable Resistor
Persistent Memory Programming Model

SNIA persistent memory programming model enables OS support for use of persistent memory.

- Operating system uses standard file semantics to provide naming, permissions.
- Use mmap on Linux to map contents of a file directly to memory.
- Direct Access (DAX) file system provides direct access to NV memory without using the system page cache as it would for normal files.
- Enables byte-addressable access to an NVDIMM.

SNIA Persistent Memory Programming Model: https://www.snia.org/forums/sssi/persistent-memory
Crosspoint Memory

Memory Element
- Current I vs Voltage V
- Low resistance state
- SET high resistance state
- RESET

Selector
- Current I vs Voltage V
- Voltage V/3
- Voltage V

Crosspoint Memory Cell
- Selected Cell Current (R/W)
- Leakage Current (Write)
- Sneak Current (Read)

Memory Element Selector
- Blocks current
Need For New Memory Interface Standard

**DRAM**

- Standard DDR interface built around Activate/RW/Precharge sequence.
- Device responds to R/W commands within a predictable number of clock cycles.

**Crosspoint Memory**

- Generally one bit read/written at a time on each tile.
  DRAM row buffer architecture not a natural choice.
- Need for non-deterministic timing and/or out-of-order response due to ECC & wear-level (e.g. NVDIMM-P).

New open standard interface required for emerging NV memories.
Memory Coherency and Fabrics

Memory

- Need Open Interfaces for Emerging NVM
  - Die-level interface
  - DIMM-level interface

Coherency

- Need Open Interfaces for Memory Coherency
  - Shared memory for different types of compute engines within the same system

Memory Fabric

- Need Open Memory Fabrics for Memory Disaggregation
  - Shared memory between different systems
RISC-V Open Instruction Set Architecture

Open
• Completely open source ISA that can be applied for any modern computing devices

Free
• Develop independent IP
• RISC-V Foundation does not charge authorization fee
• BSD license allows developers to decide if they want to share their own work

Safe
• Clear separation between user and privileged ISA
• No known hardware-level security flaws like Spectre and Meltdown; open nature reduces potential security threats

Regulation
• Prevent fragmentation of RISC-V in China
• Small standard base ISA with only 40+ base instructions

Extensibility/Specialization
• Variable-length instruction encoding
• Vast opcode space available for instruction-set extensions

Stable
• Base and standard extensions are frozen
• Additions via optional extensions, not new versions
Western Digital SweRV Core™

• First production-grade open source RISC-V core.
• 2-way, superscalar, in-order core with 9 stage pipeline.
• 1 GHz operation @ 28nm.
• Support for RV32IMC.
• Ideal for high-performance embedded applications
• Western Digital RISC-V SweRV cores available: https://github.com/westerndigitalcorporation/swerv_eh1

Western Digital ships in excess of 1 Billion cores per year ...and we expect to double that.
OmniXtend™: An Open Coherent Memory Fabric

- Cache coherency over ethernet
- Specification available [https://github.com/westerndigitalcorporation/omnixtend](https://github.com/westerndigitalcorporation/omnixtend)
Conclusions

• Massive proliferation of data driven by new applications and by new methods for extracting value from data.

• Storage technology evolution continues for both HDD and NAND Flash, driven by invention of new technologies, processes and materials.

• Fundamental changes to both storage and memory technologies, as well as new open interface standards, will drive changes in the software stack, and enable new applications.

• RISC-V offers an open platform for innovation in memory, storage and compute architecture. Please join us in supporting RISC-V.
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We create environments for data to thrive