SDC 20

BY Developers FOR Developers

Storage Developer Conference
September 22-23, 2020

Update on the JEDEC DDR5 NVRAM Specification

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Agenda

- Volatility and non-volatility in the memory hierarchy
- How non-volatility for main memory changes things
- NVRAM: the coming standard for main memory
- Nantero NRAM™
- Changing system architectures
- Call to Action

The traditional memory hierarchy

The game we play to trade off performance, capacity, and cost

FEAR

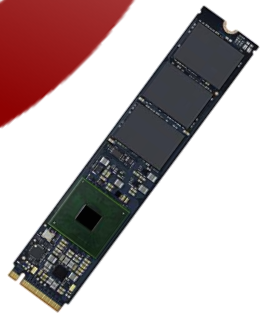
...of power failure

FEAR

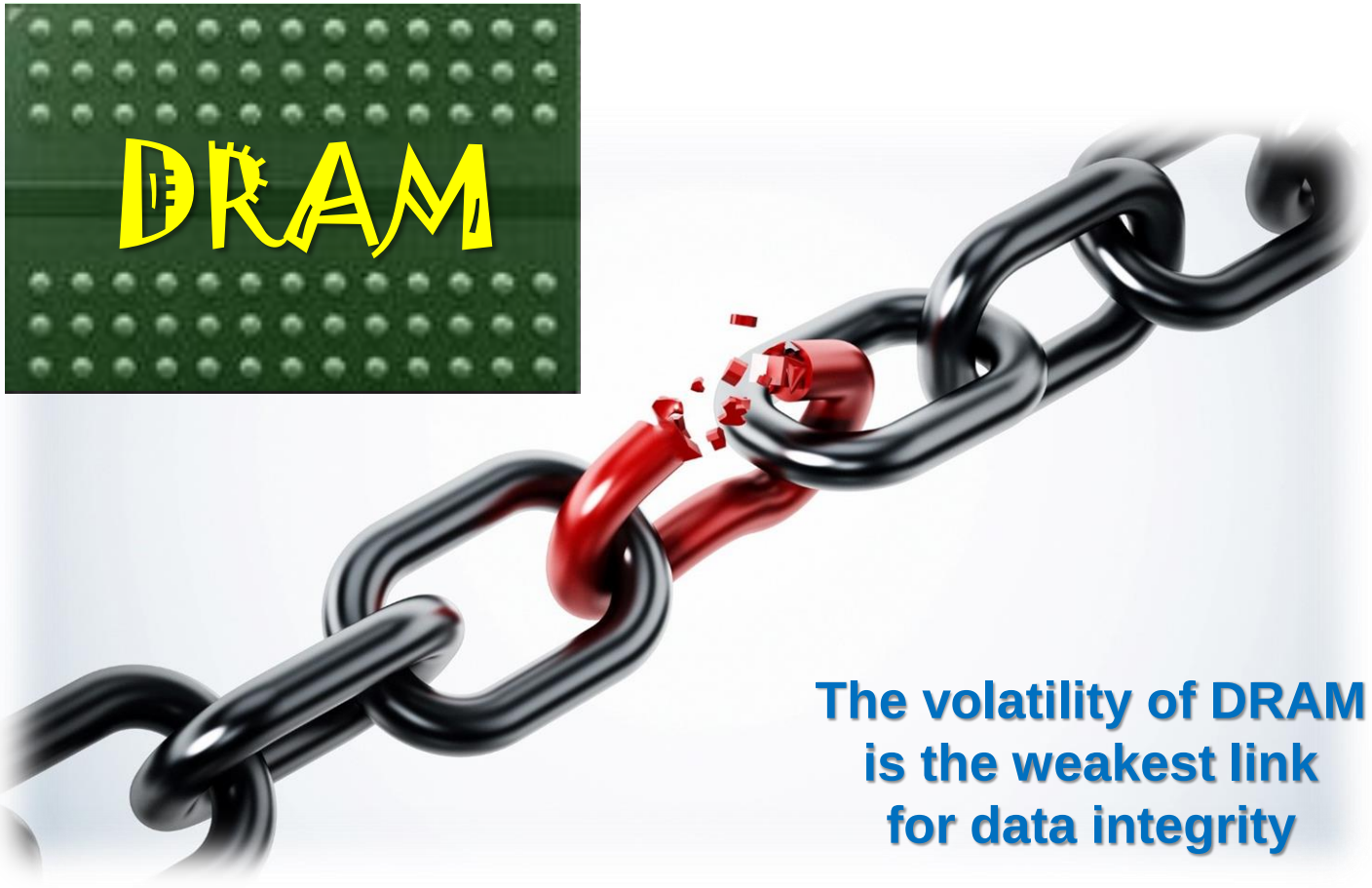
...of data loss

Decades of progress made

To bring non-volatile memory closer to the CPU

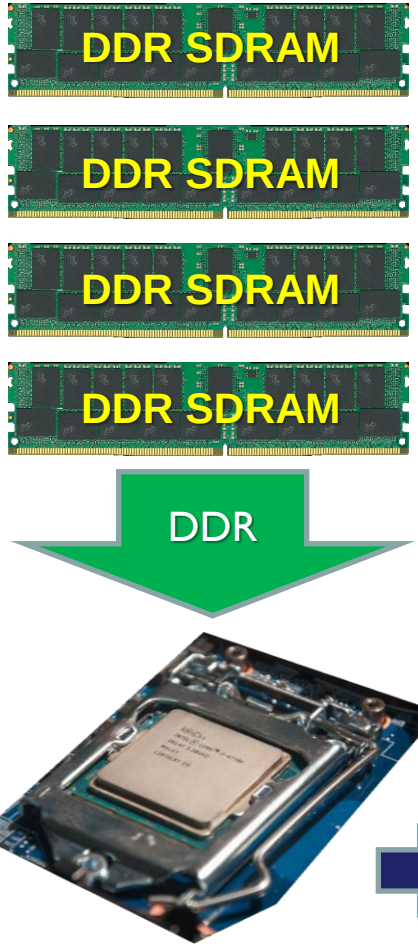


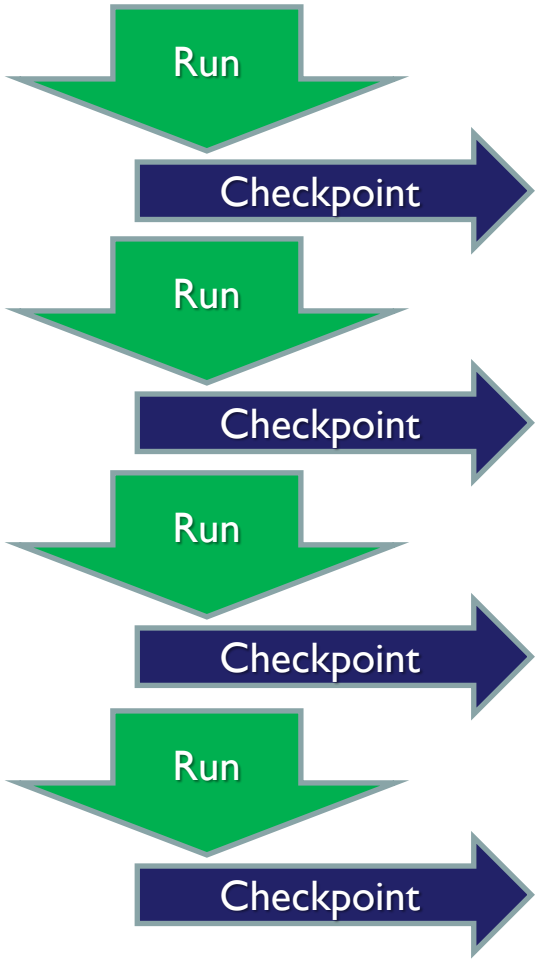
Yet a chasm remains



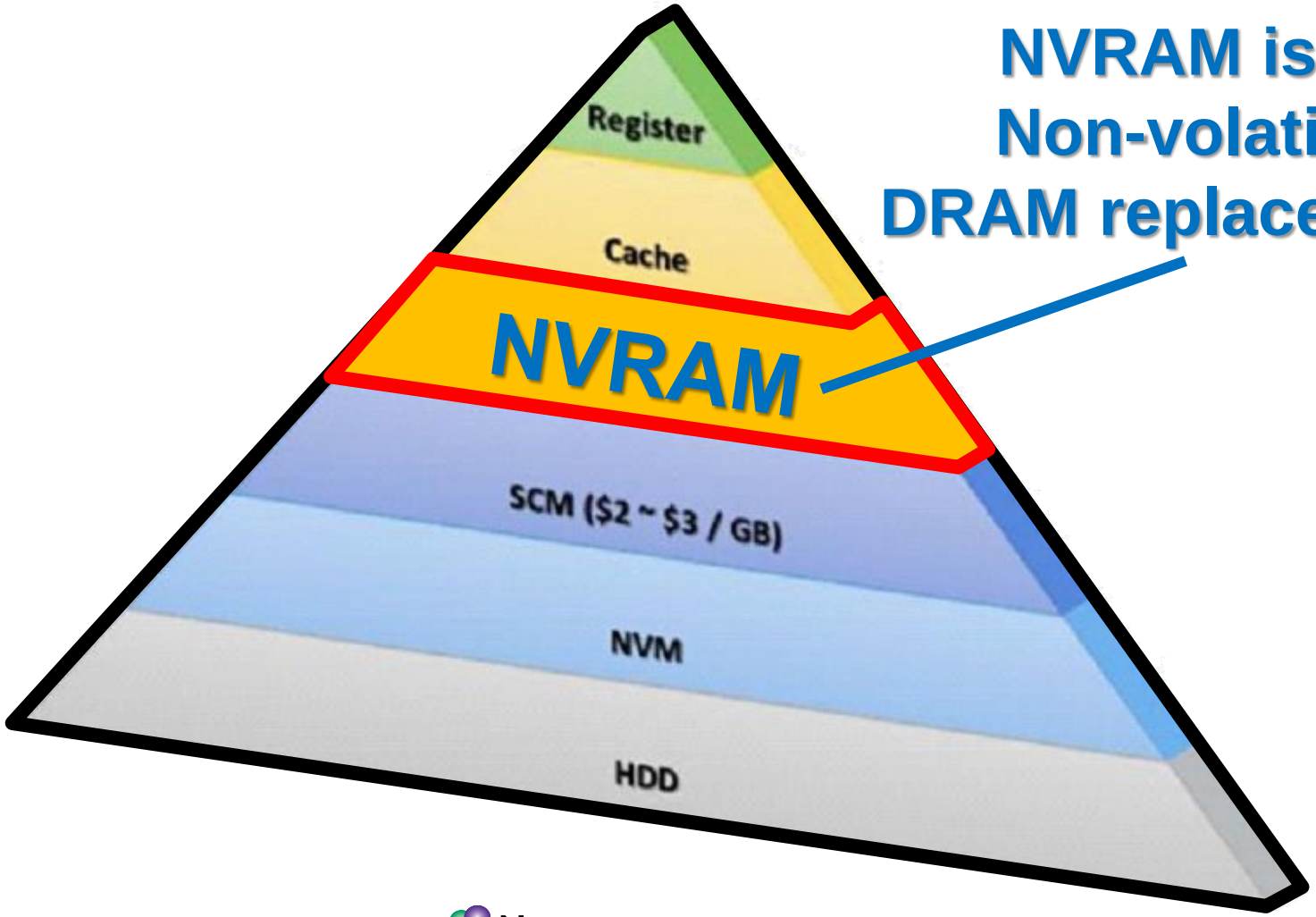
The volatility of DRAM is the weakest link for data integrity

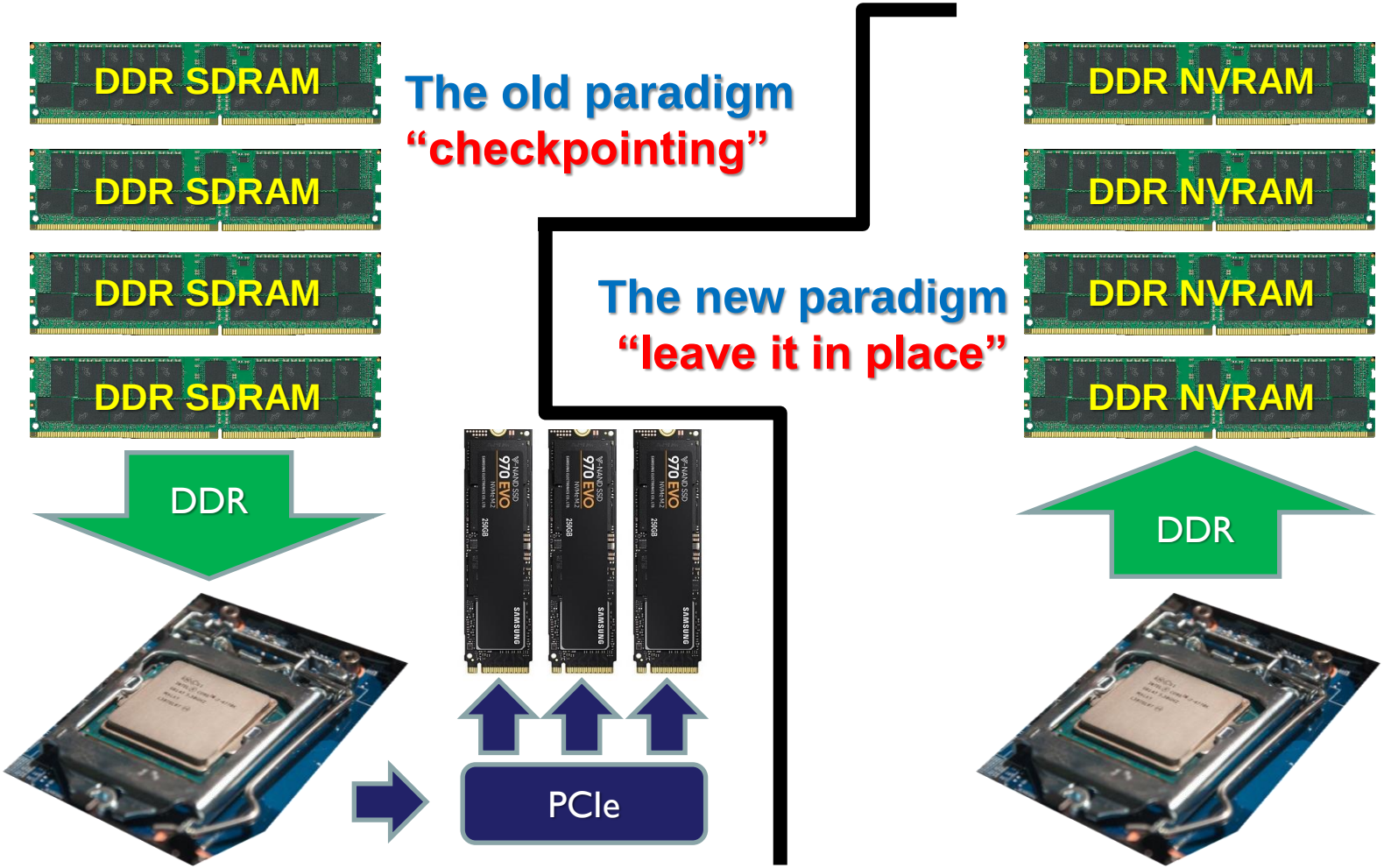
Data integrity paradigm
"checkpointing"





NVRAM is a Non-volatile DRAM replacement





Obviously not all storage goes away

What storage is used for can change

There are data sets that don't fit in memory

Data set size is, however, application dependent

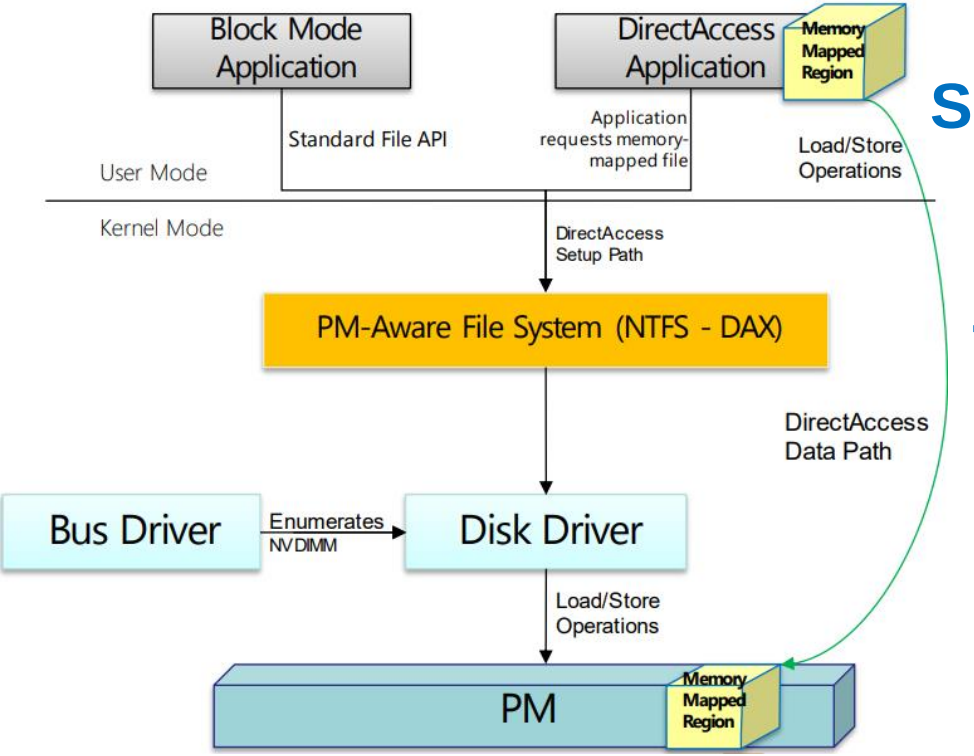
There are system failures besides power fail

The time between checkpoints is vastly different

Awesome Hardware Is COOL

but software is the tail that wags this dog

Helping software migrate



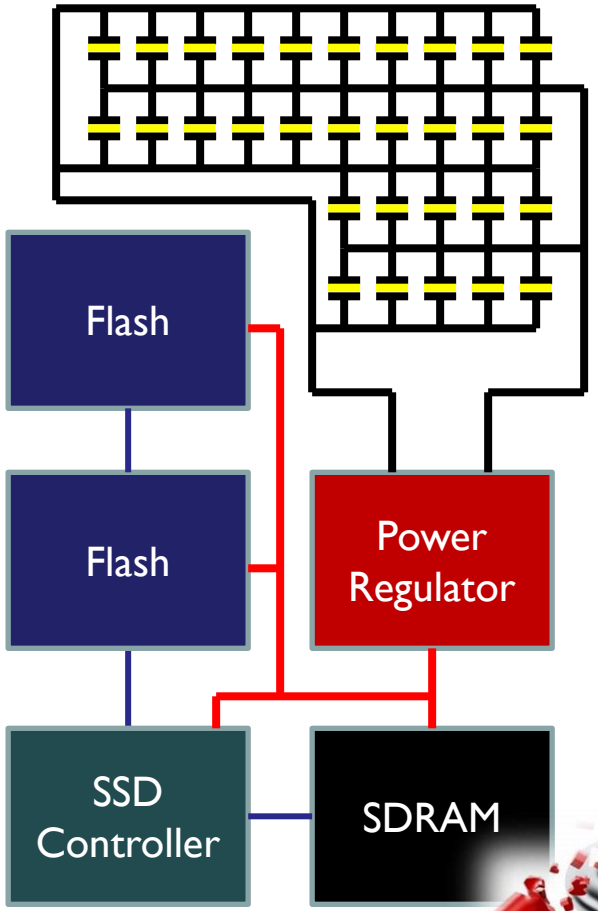
Software support via DAX assists in moving…

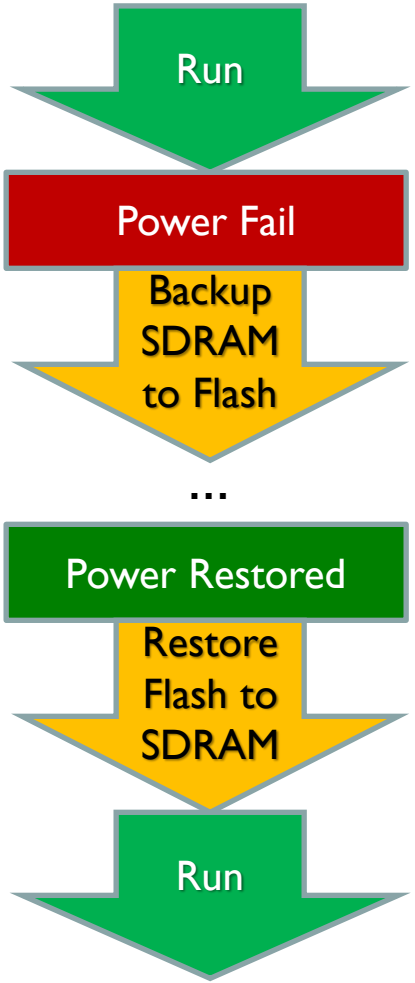
from mounted drives…

…to RAM drive…

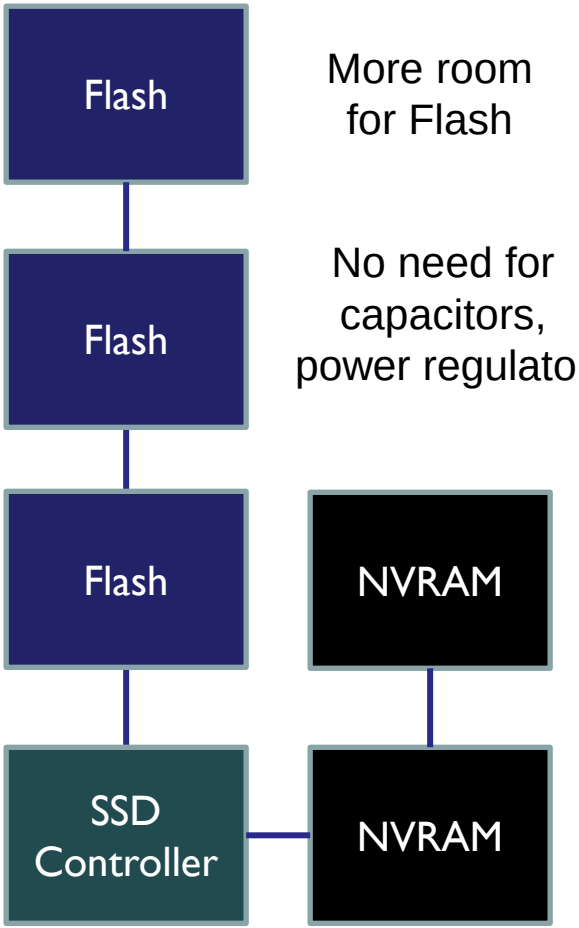
…to direct access mode

SSDs have the same problem



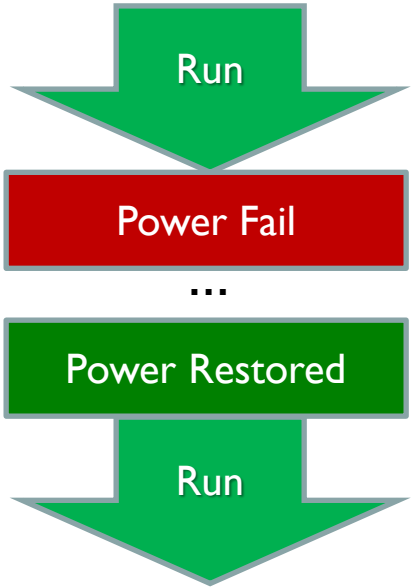


SSDs love NVRAM



More room for Flash

No need for capacitors, power regulator



Cache size decoupled from energy store

To Replace DRAM, NVRAM MUST HAVE

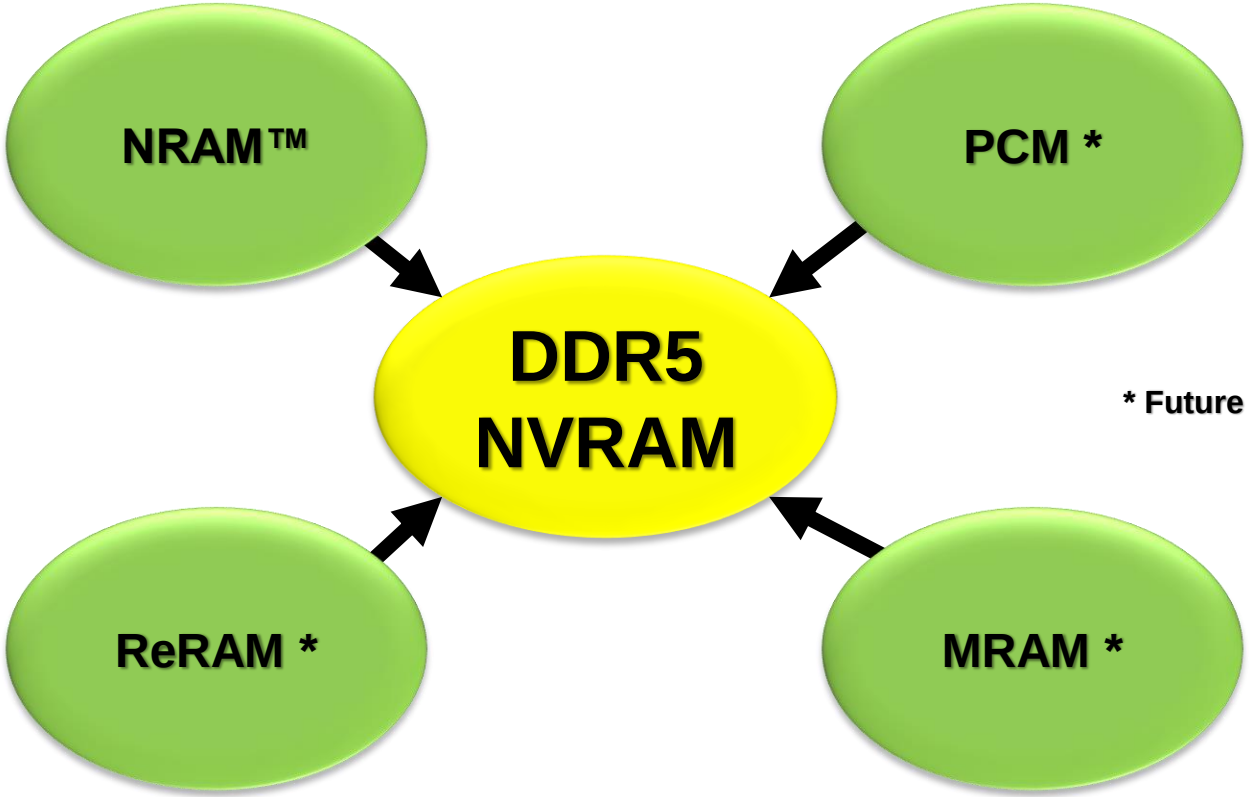
Full DRAM speed

No wear-out

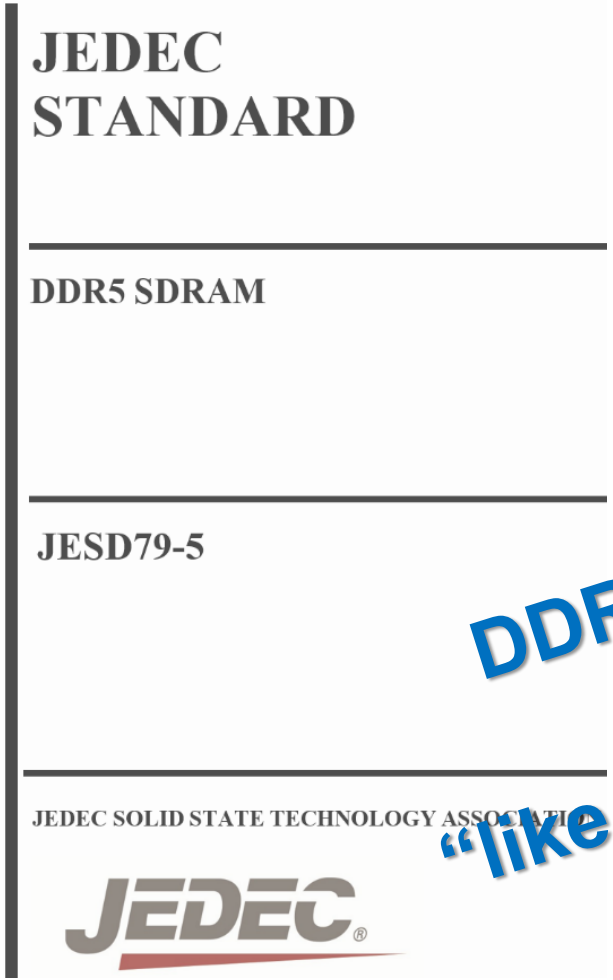
DRAM capacity or greater

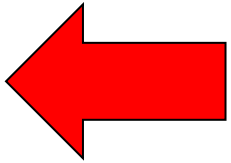
DRAM price

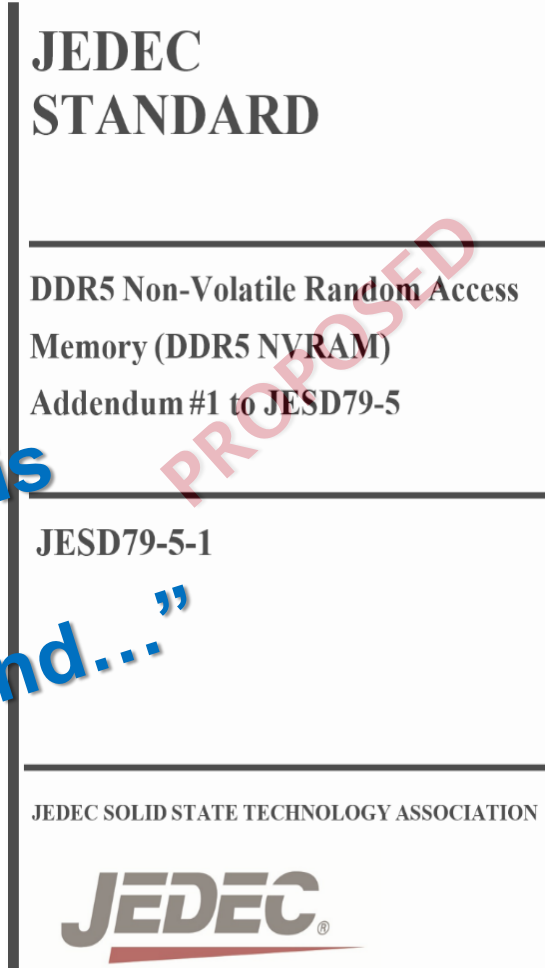
to be the ultimate Persistent Memory



* Future generation devices







DDR5 NVRAM is
"like a DRAM, and…"

Comparing DRAM & NVRAM

No refresh is required

"Self refresh" can be power OFF

Timing compatible

New: data persistence definitions

Greater per-die capacity

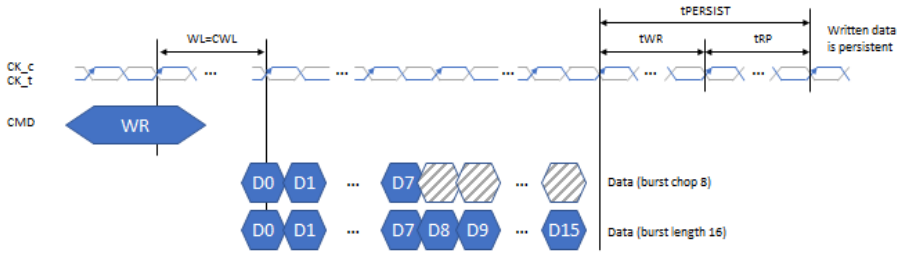
Differences between media types represented as "Profiles"

Command needed for "housekeeping"?

Do pages remain open or need to be closed?

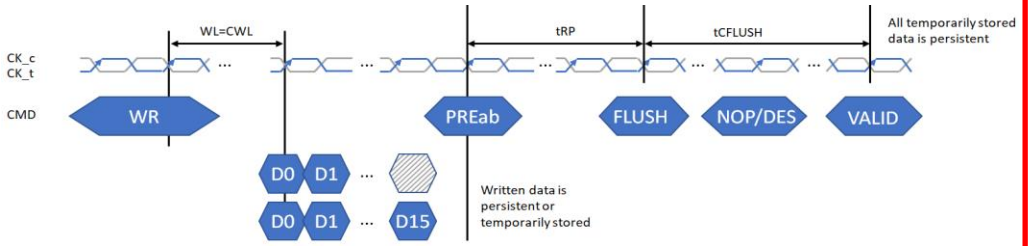
Is some kind of flush needed for internal buffering?

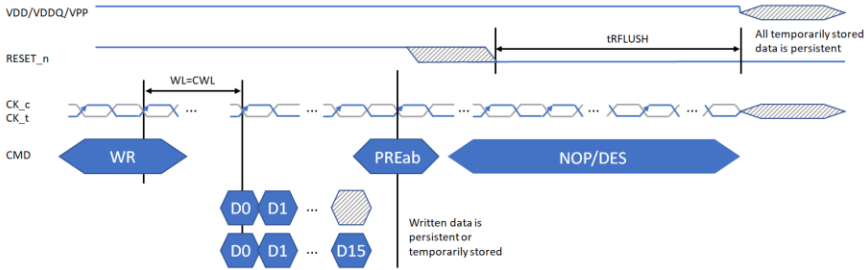
Organization of pages, banks, bank groups



Intrinsic Persistence

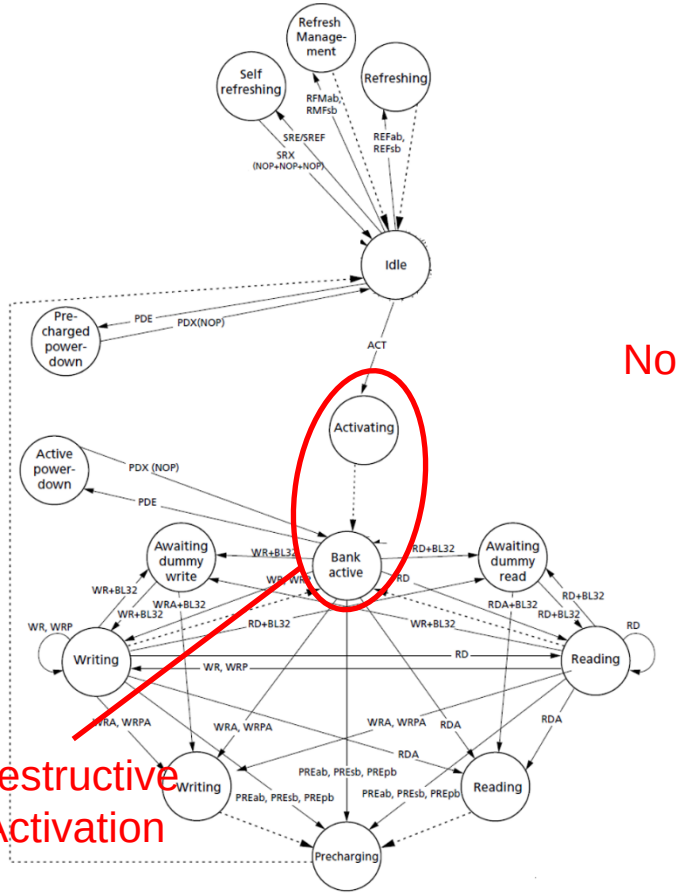
Extrinsic Persistence





Runtime RESET Persistence

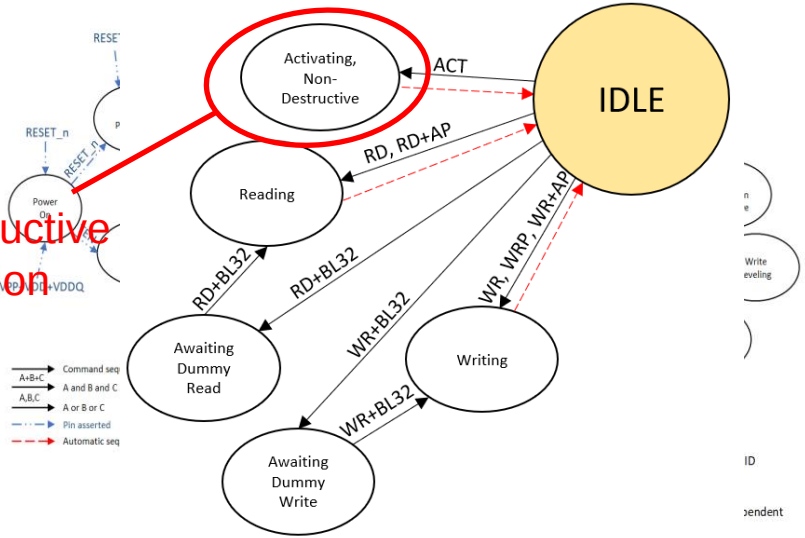
DDR5 SDRAM State Diagram



Destructive Activation

Non-Destructive Activation

DDR5 NVRAM State Diagram



Compatible, but simplified
Closer to a load/store memory

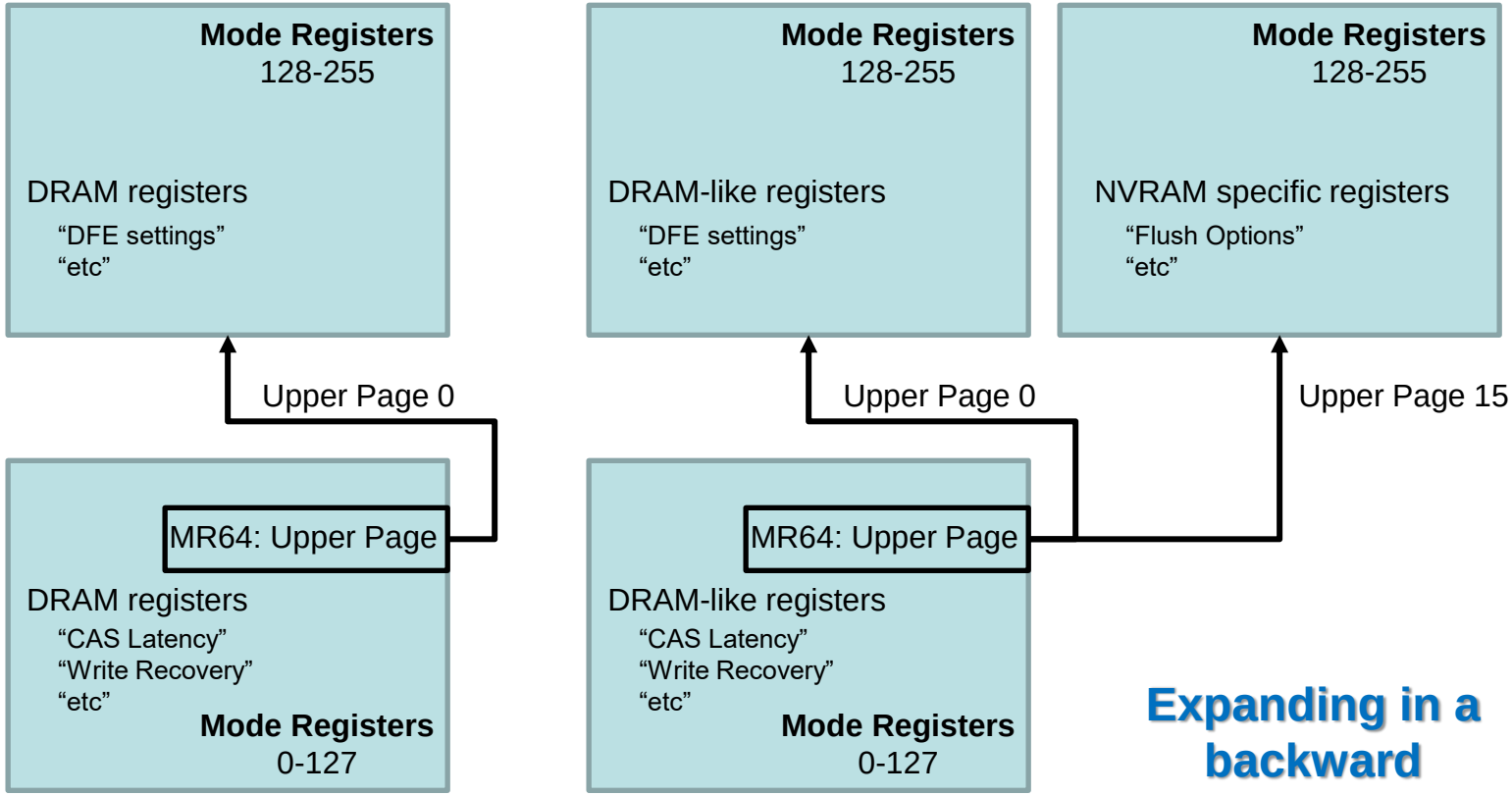
DDR5 SDRAM

33 address bits → Maximum density of 32 Gb per die

DDR5 NVRAM

Row Extension adds 12 more bits of addressing
Enables density up to 128 Tb per die

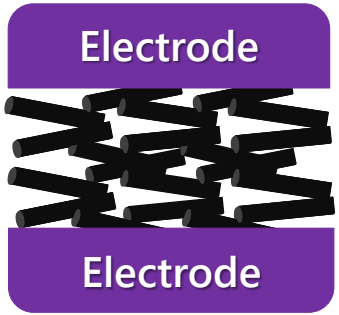
New: Mode Register Expansion



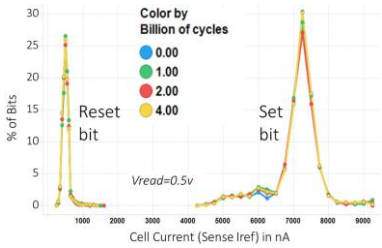
Expanding in a backward compatible way

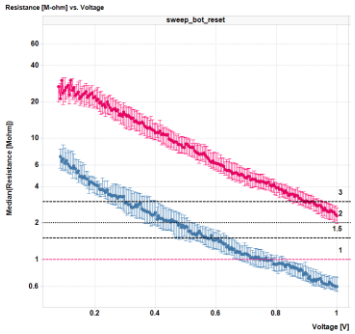
And now, a plug from our sponsor…

NANTERO



Maintained by Van der Waals barrier

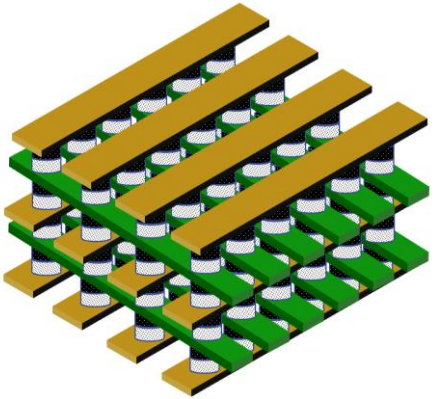


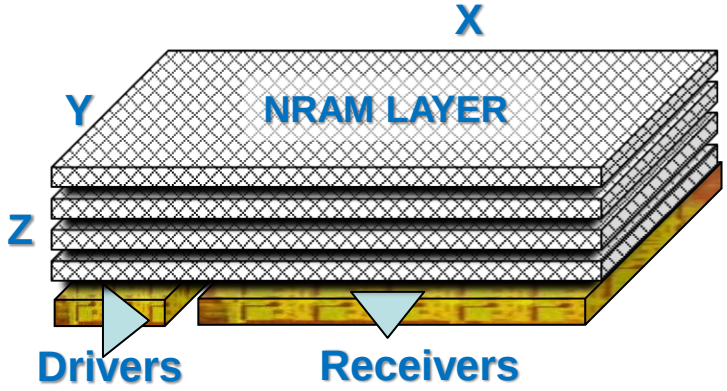


Carbon nanotubes (CNTs) switch freely in a dielectric-free space…

…in 5ns (Write or Read)…

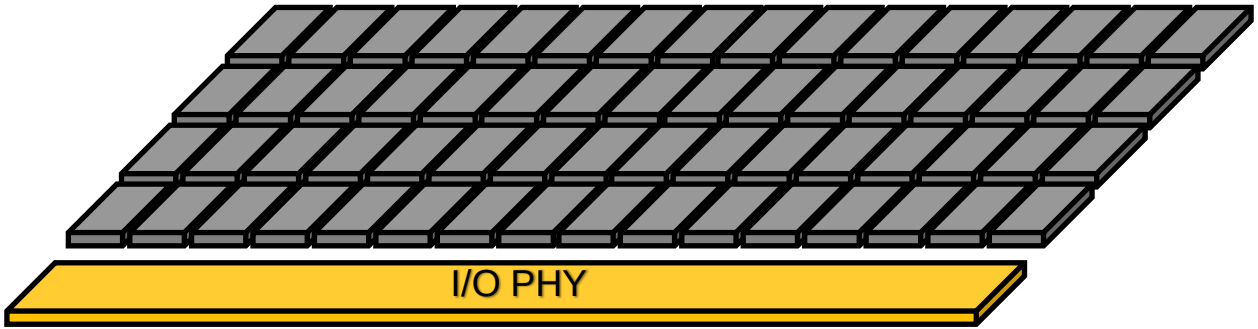
…resulting in a permanent cell resistance change

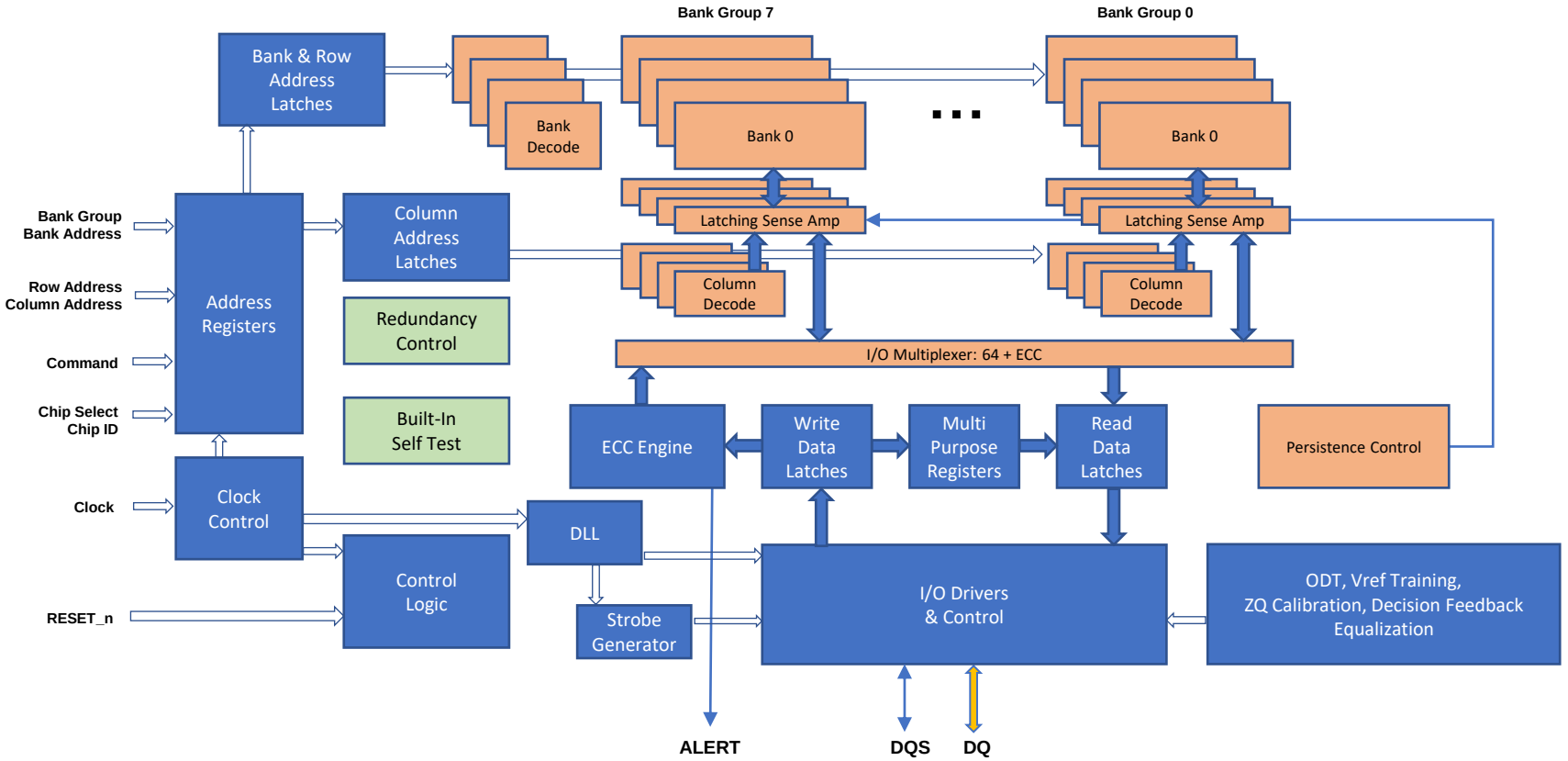




Tune the array size to the size of drivers & receivers
Core-level timing is dominated by word & bit line flight times
Replicate this “tile” as needed for device capacity
Add I/O drivers to emulate any PHY needed & meet chip timing

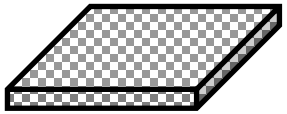
64 Kb tile
X 256K tiles
= 16 Gb





DDR5 NVRAM Reference Design

~100 mm^2



Baseline

16 Gb
28 nm
4 layers CNT

16 GB

Add layers

8 Gb
28 nm
2 layers CNT

8 GB

New process

64 Gb
14 nm
4 layers CNT

128 GB

Add layers

128 Gb
14 nm
8 layers CNT

256 GB

New process

256 Gb
7 nm
4 layers CNT

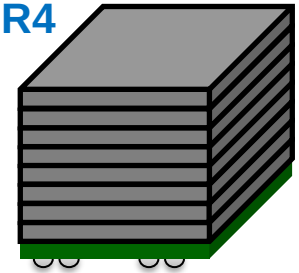
512 GB

Add layers

512 Gb
7 nm
8 layers CNT

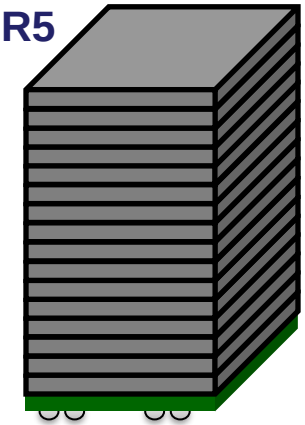
1 TB

DDR4



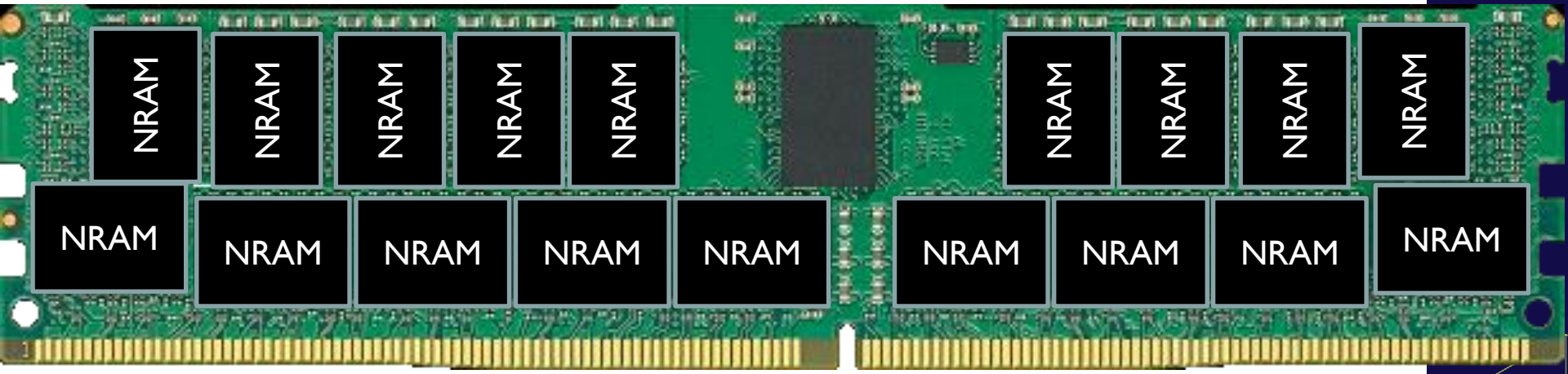
8-die stacks

DDR5



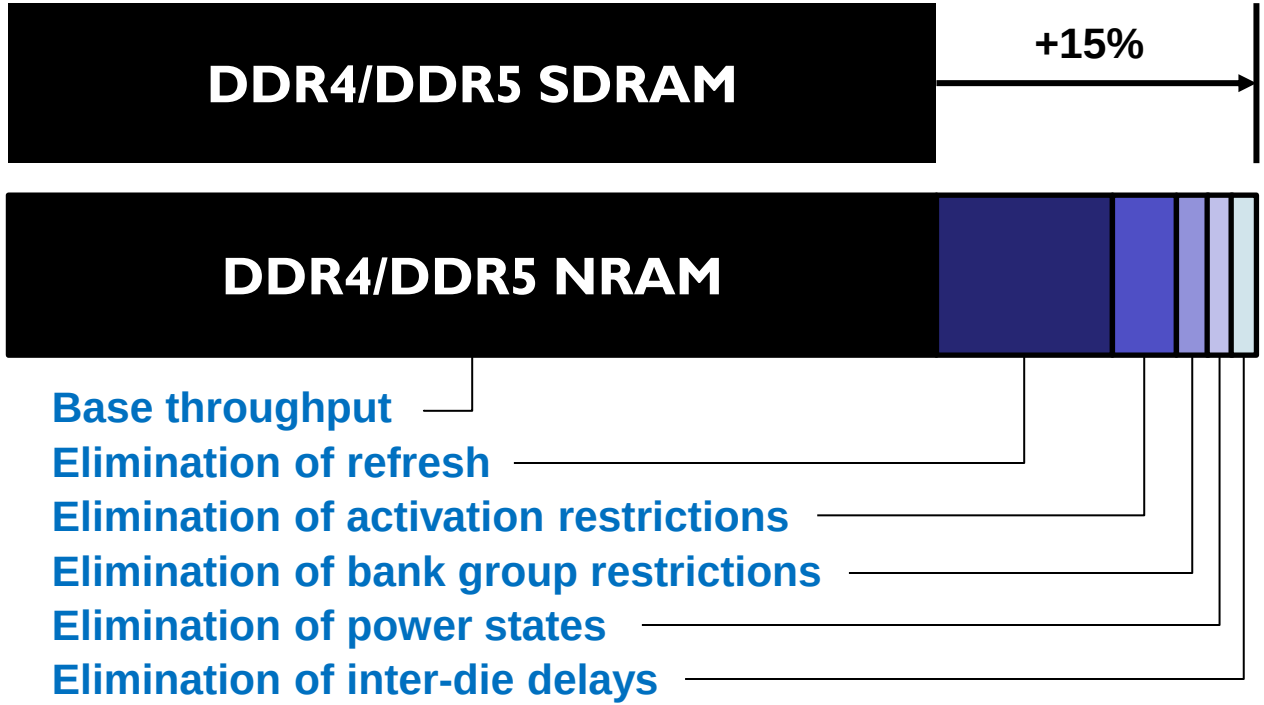
16-die stacks

NVRAM
Memory Class Storage



Plugs into an RDIMM slot
Appears to the CPU as DRAM
Memory controller may optionally be tuned for NVRAM

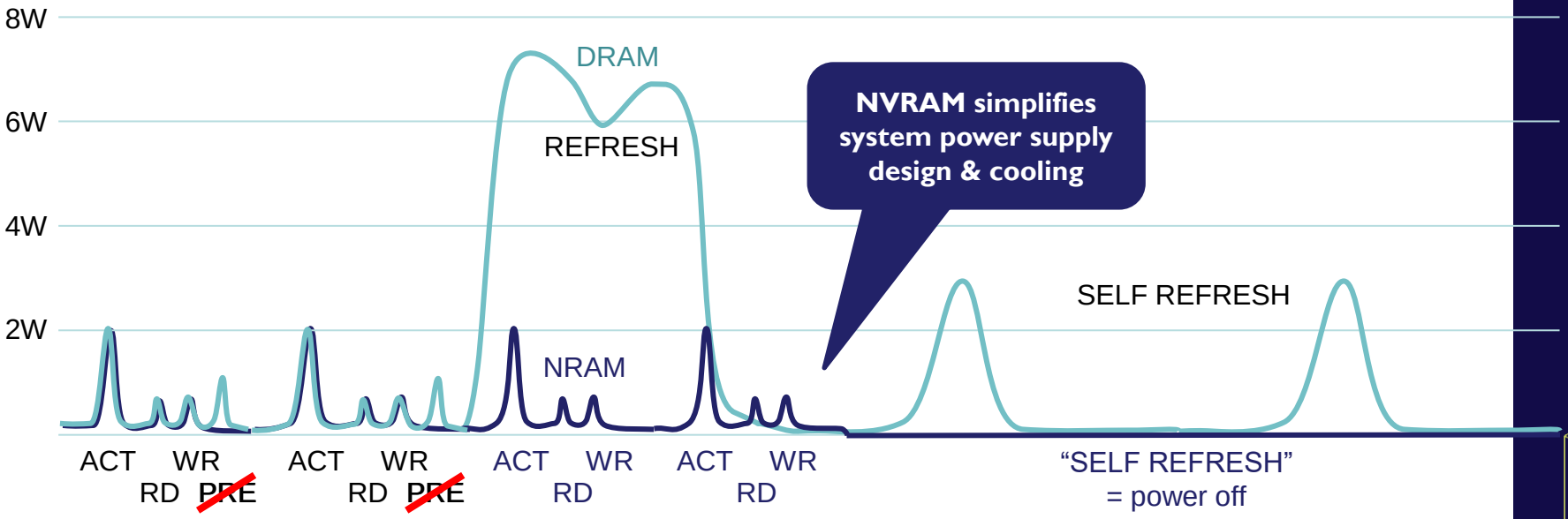
512 Gb per die → 16 TB per DIMM



+15% higher throughput at the same clock frequency

Bandwidth: larger is better

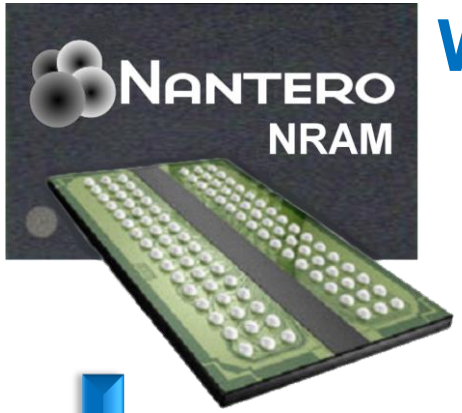
72-bit DDR4 Memory Module Active Power Profile *



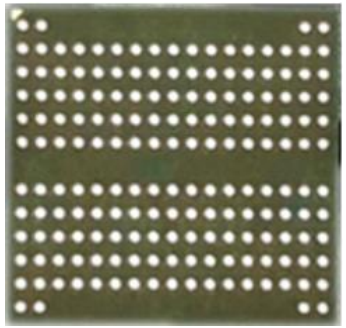
Per rank…

8 or 16-rank DRAM modules must accommodate multiple ranks with overlapping refresh

* Abstracted from an actual DRAM vendor data sheet

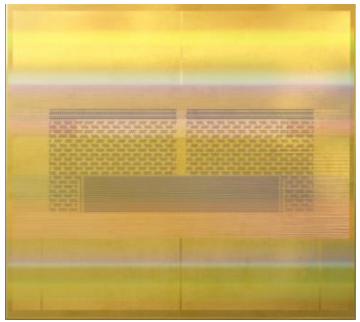


What's next?

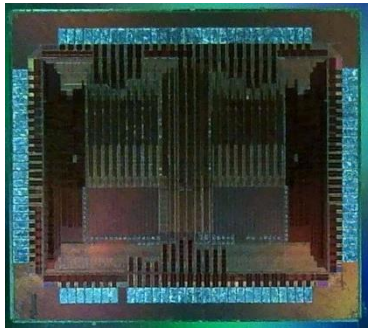


LPDDR NVRAM
Mobile, Automotive

HBM NVRAM
Artificial
Intelligence

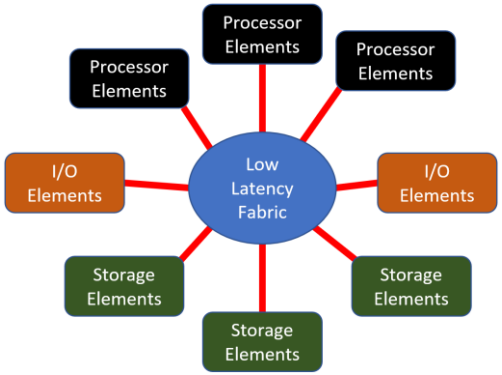


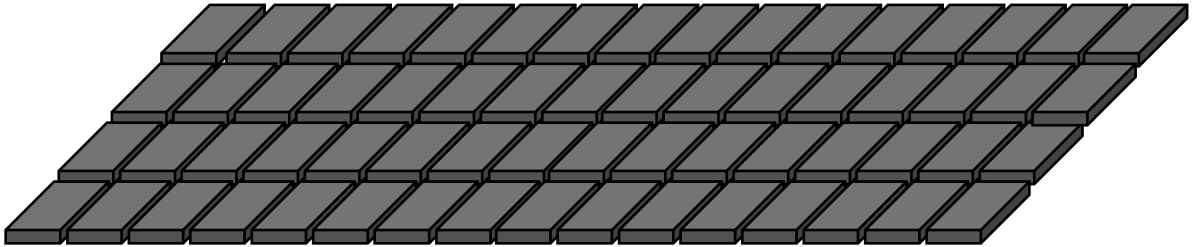
Embedded NVRAM
IoT, AI, FPGA, µC



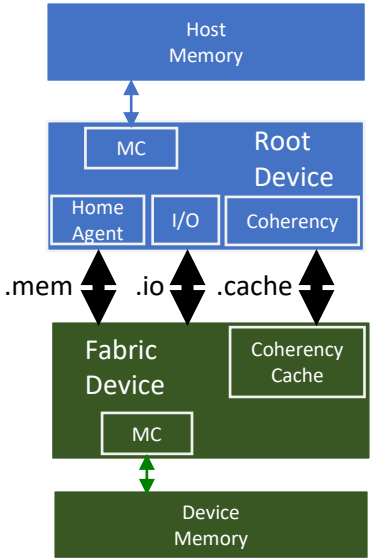
NVRAM will emerge as the universal memory

Beyond NVRAM?





Media Access Layer – Raw Media Exposed



Fabric Translation Layer

Authentication Encryption

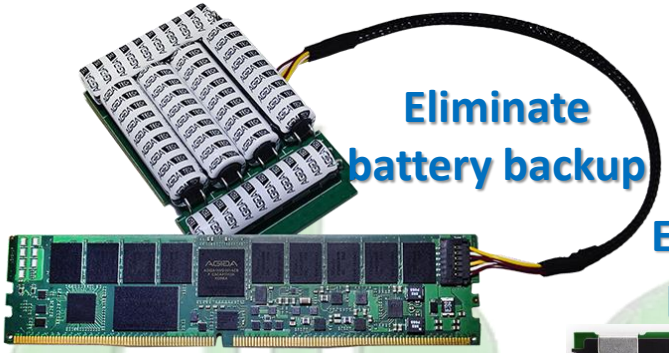
Error handling Striping & redundancy

Processing In Memory

Cache Cache management Coherency

Protocol

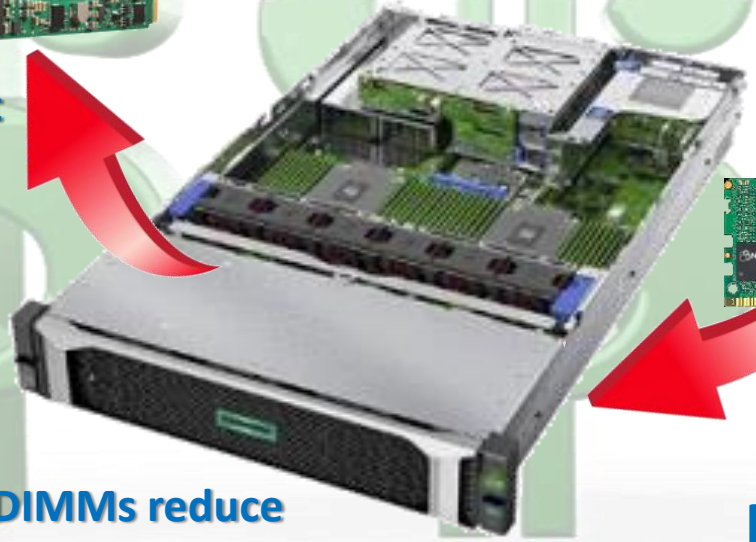
Total Cost of Ownership



Eliminate battery backup

Mass storage not needed for checkpoints

Eliminate redundant persistent memory

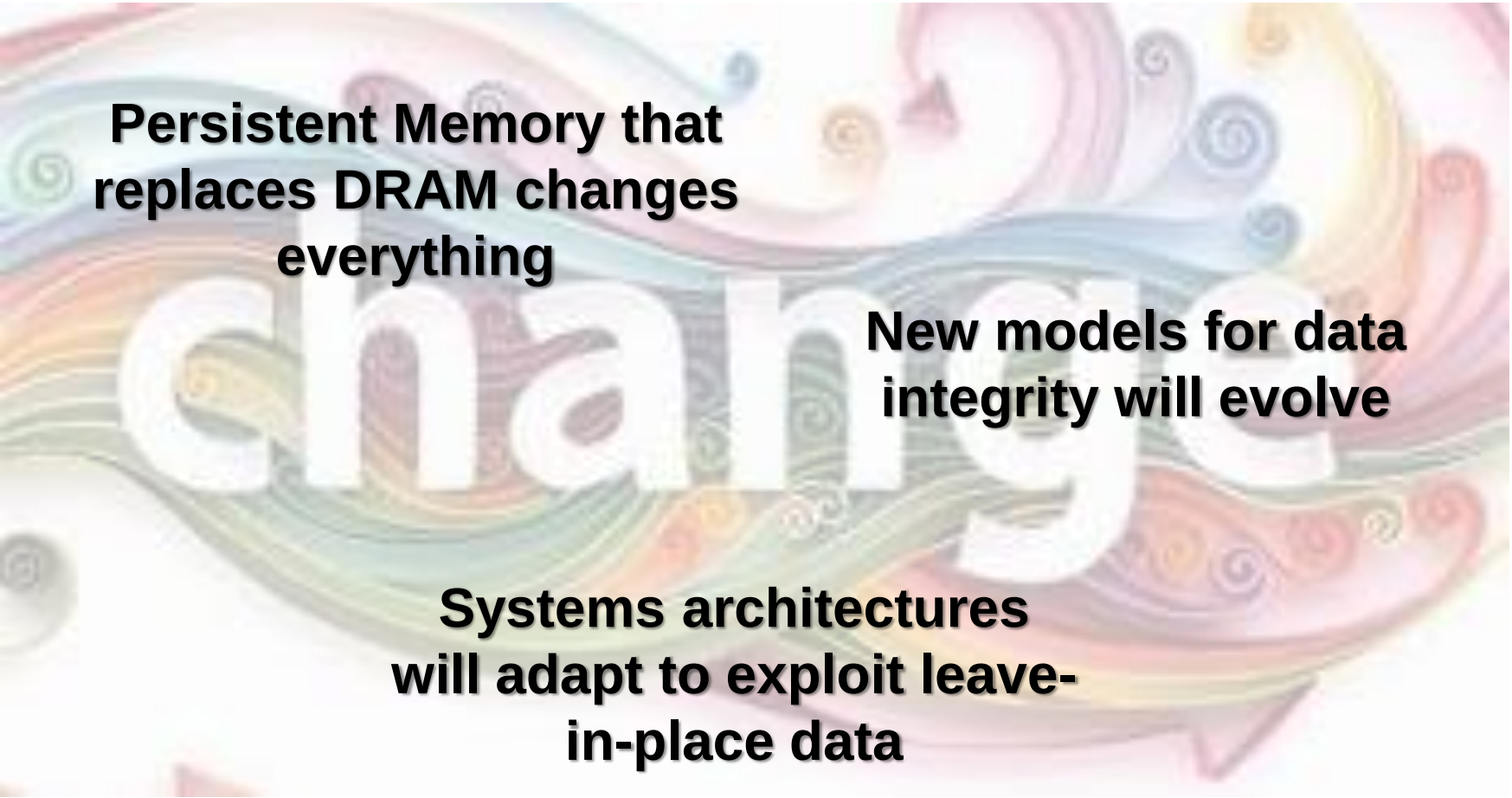


Eliminate data loss on power failure

TB DIMMs reduce # systems needed

Reduce cooling requirements

NVRAM lowers TCO

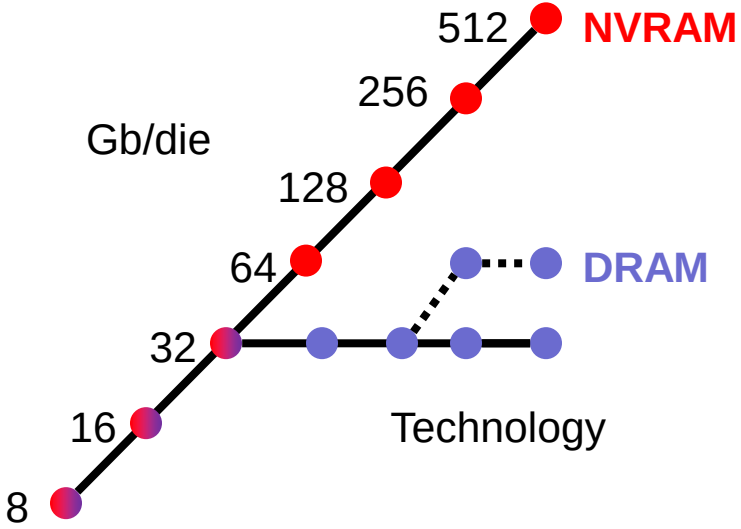


Persistent Memory that replaces DRAM changes everything

New models for data integrity will evolve

Systems architectures will adapt to exploit leave-in-place data

When?



With DRAM hitting a plateau
we all need this in the DDR5 life cycle

CALL TO ACTION

Join the JEDEC
Future Memory Task Group
jedec.org

Contact: bilge@Nantero.com

Fear of power failure drives architectures

Non-volatility removes that fear factor

NVRAM defines a non-volatile DRAM replacement

Summary

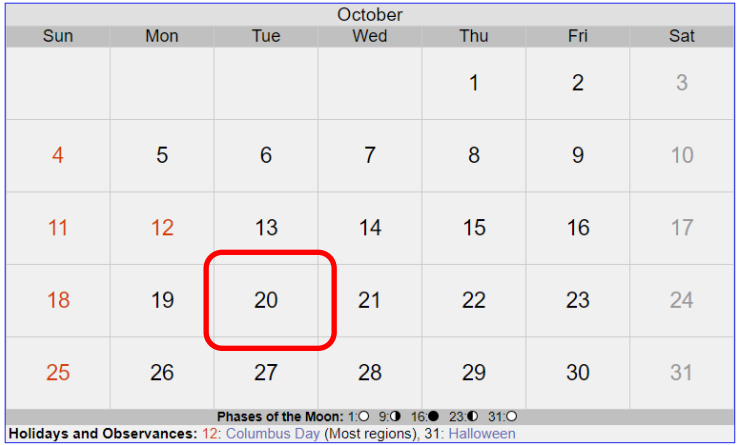
Call to Action: get involved!

System architectures are evolving

Nantero NRAM™, the best DRAM replacement

https://www.bridge-to-connect.com

BRDG is a non-profit that mentors university students in STEM fields



October

Sun	Mon	Tue	Wed	Thu	Fri	Sat
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

Phases of the Moon: 1○ 9◑ 16● 23◐ 31○

Holidays and Observances: 12: Columbus Day (Most regions), 31: Halloween

Twice a year, BRDG sponsors a technology education event for Southern California educators and technology CEOs

“Directions, Applications, and the Future of Artificial Intelligence”

Michael Giering, Research Fellow
Raytheon Technologies Research Center

Tuesday, October 20, 2020
4 – 6 PM PDT