STORAGE DEVELOPER CONFERENCE
SDC 21
BY Developers FOR Developers
Virtual Conference
September 28-29, 2021
A SNIA Event

Emerging Computer Architectures Powered by Emerging Memories

Change Is Upon Us!

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Outline

- Emerging Memory Status
- Using Emerging Memories in Computing
- Changes to Computer Architecture
- A Path to the Future
- Q & A

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Emerging Memory Status

What's Here Now, and What's Coming

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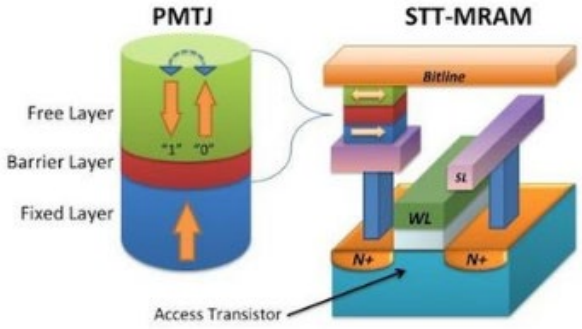
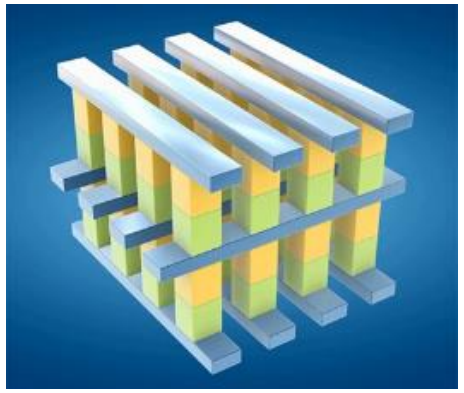
Emerging Memory Cast of Characters

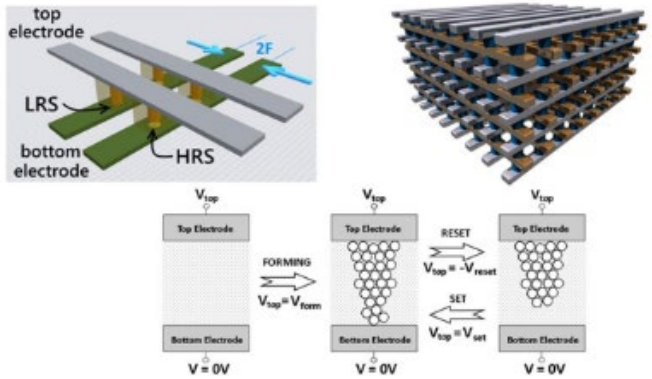
MRAM



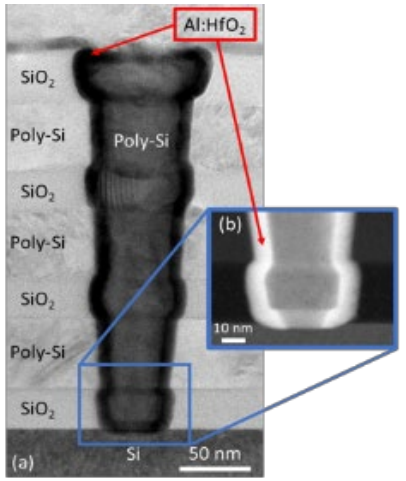
PCM/XPoint



ReRAM



FRAM



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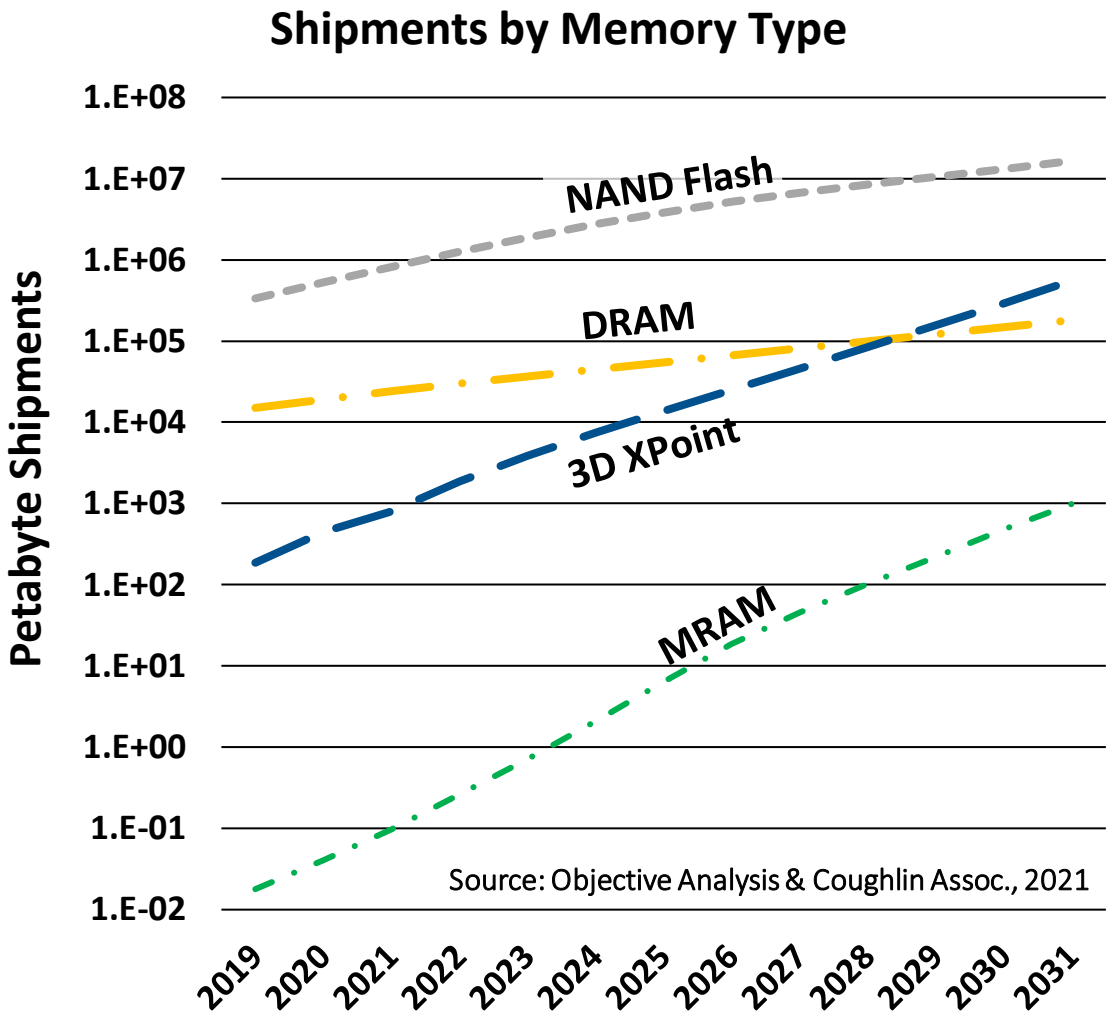
PM Is Real, and Getting Realer!



- DRAM & NAND have staying power
- 3D XPoint poised to make serious inroads
- MRAM is doing well today
  - Also gaining acceptance as embedded memory in SoCs
- This outlook is anything but certain!

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All Emerging Memories Have Similarities

- Persistent
- Slower than DRAM, faster than NAND Flash
  - No erase-before-write
  - Read & write speeds much more similar than in NAND
- Promise to scale beyond DRAM & NAND flash
  - Will extend Moore's Law price reductions
- Suffer from economies of scale disadvantage
  - If it's cheap it will sell in volume
  - If it sells in volume it will become cheap

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New Report: Emerging Memories Take Off!

OBJECTIVE ANALYSIS
Semiconductor Market Research

Coughlin Associates

Now Available!

https://Objective-Analysis.com/reports/#Emerging
http://www.tomcoughlin.com/techpapers.htm

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Using Emerging Memories in Computing

Are We Causing Problems for Ourselves?

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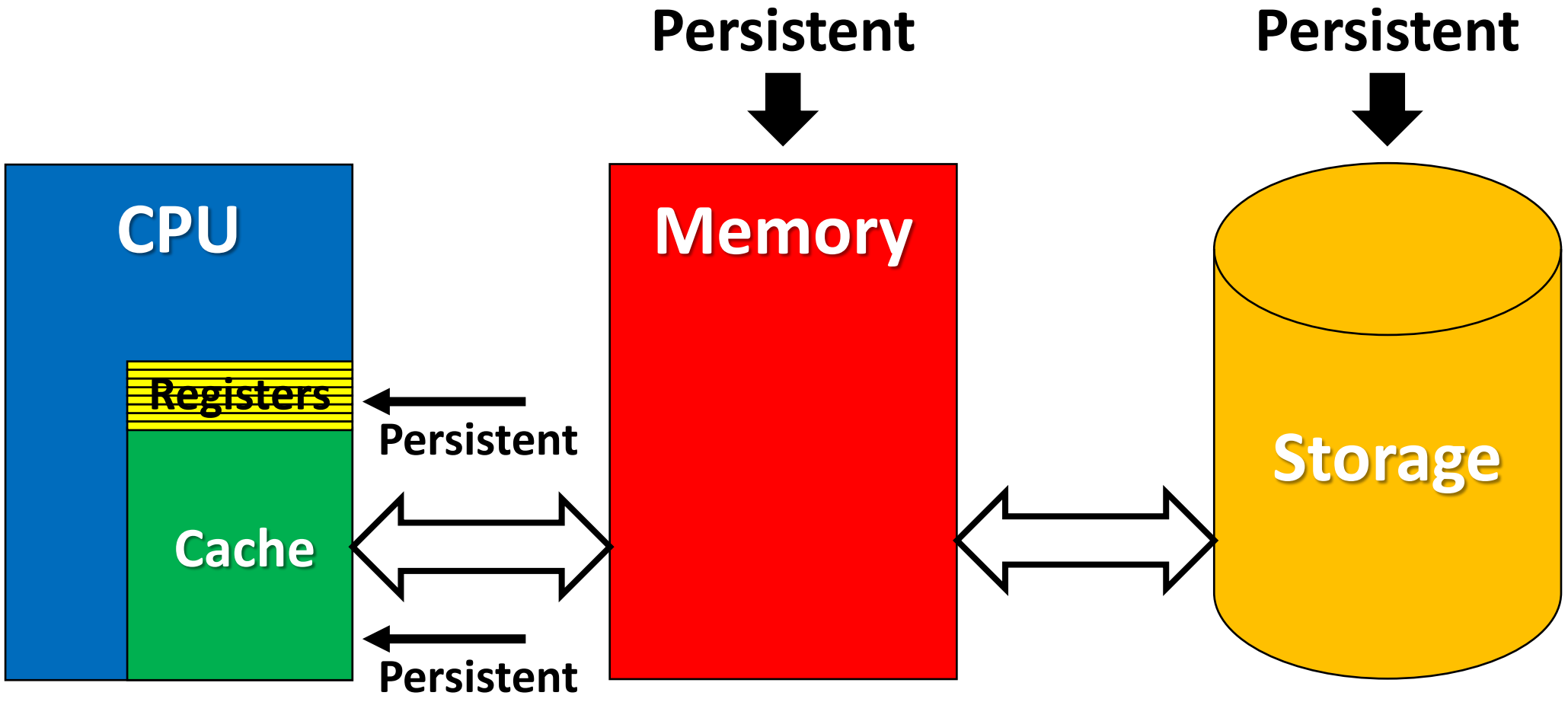
Eventually, Persistence Will Be Everywhere!



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DDR Issues

- Doesn’t support mixed memory speeds
  - XPoint slower than DRAM
    - Writes slower than reads
- The DRAM controller is within the CPU
  - The most expensive real estate in the world
  - Persistence complicates it
- Decreasing number of DIMMs per channel
  - Capacitance issues
  - Undermines bandwidth & capacity needs
- Consumes massive power & pins

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Software Issues

- Memory is Memory & Storage is Storage
  - …and never the twain shall meet!
  - Code must be rewritten to gain most of the advantage
    - This takes time
- Cache considerations
  - Persistent & non-persistent flushes
- Security needs to be thought through
  - Power-off doesn't mean data is lost
  - New path to physical data theft

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Changes to Computer Architecture

Solving Those Problems

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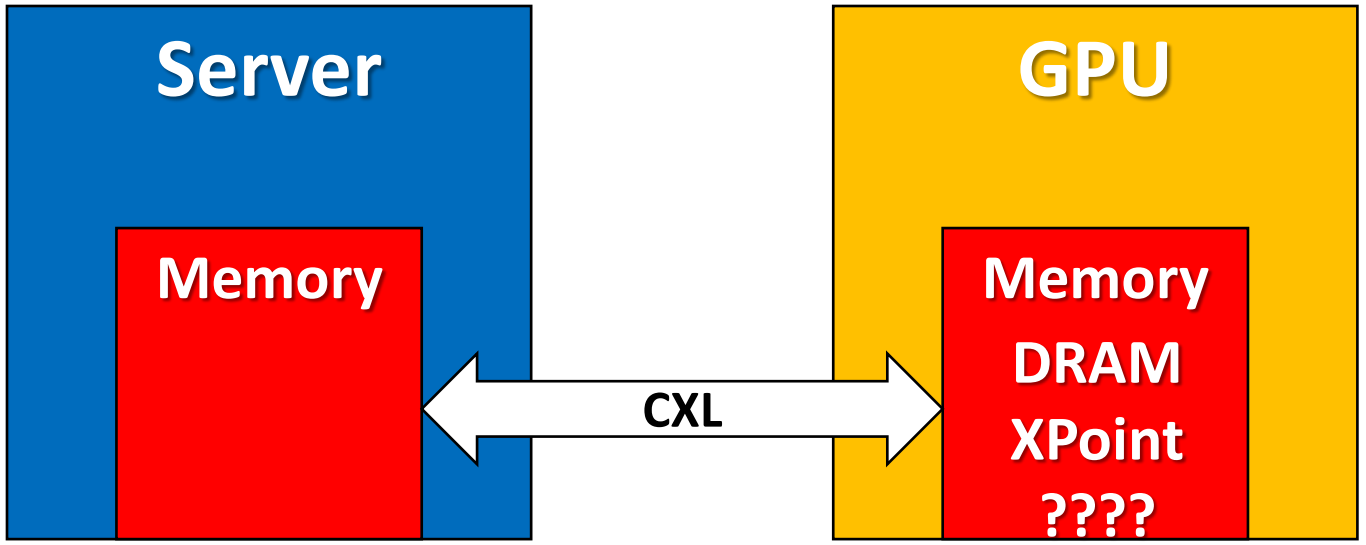
Far Memory Supports Mixed Access Speeds

- I look at yours, you look at mine
- Yours is slow to me, mine is slow to you
- Data sharing is enormously fast!



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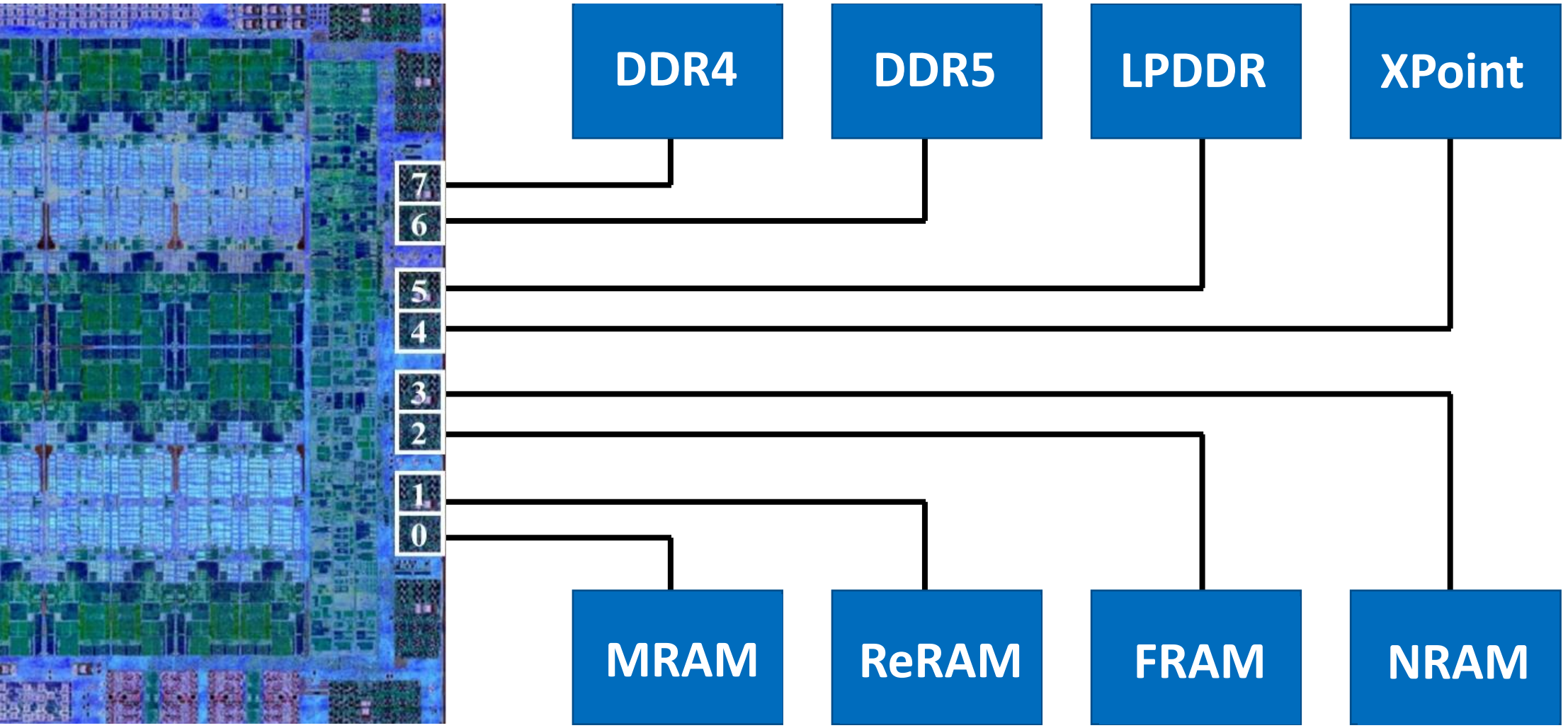
OMI Brings That Concept to Near Memory



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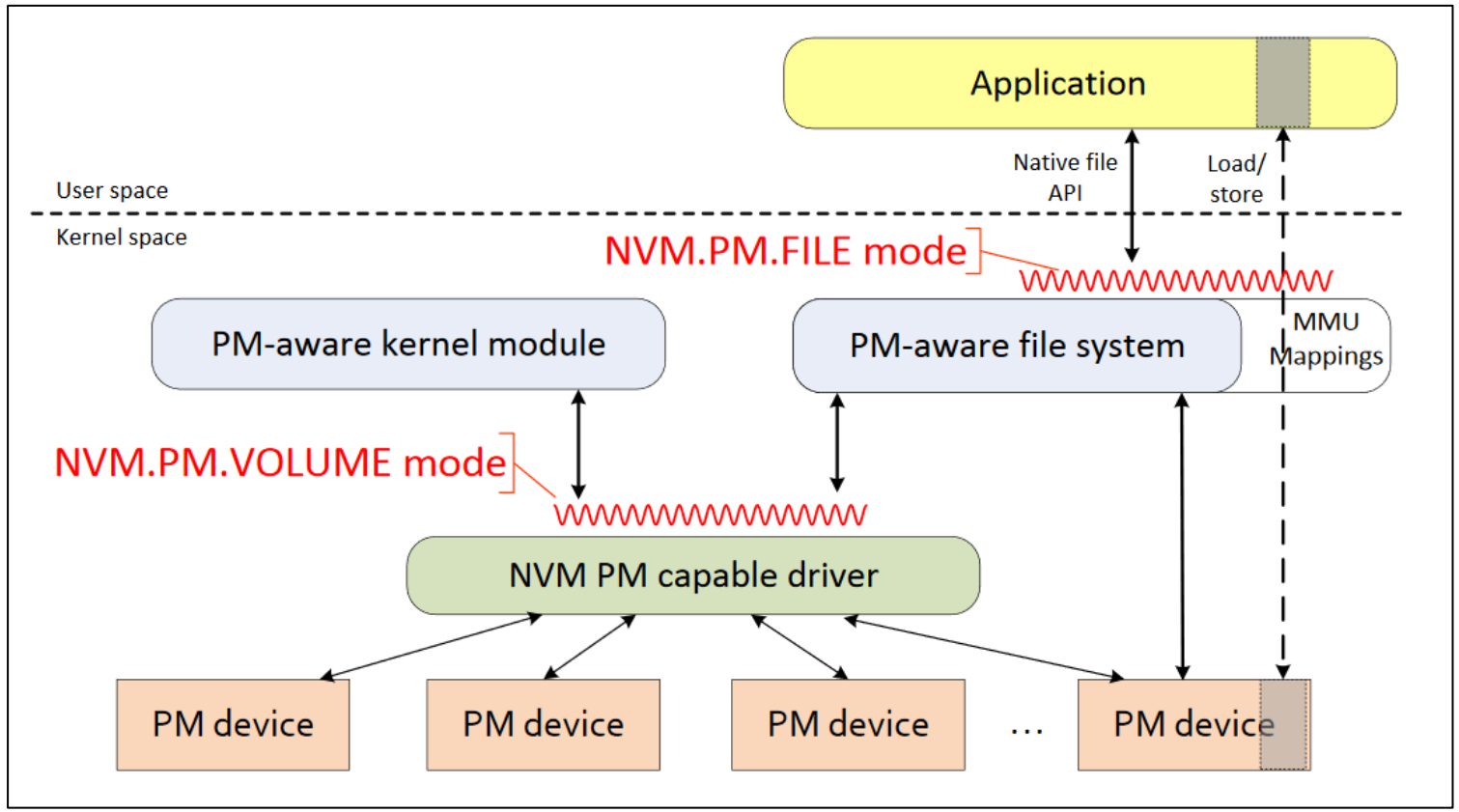
SNIA NVM Programming Model



- Supporting software now available
  - Intel, SAP, Oracle, who else?

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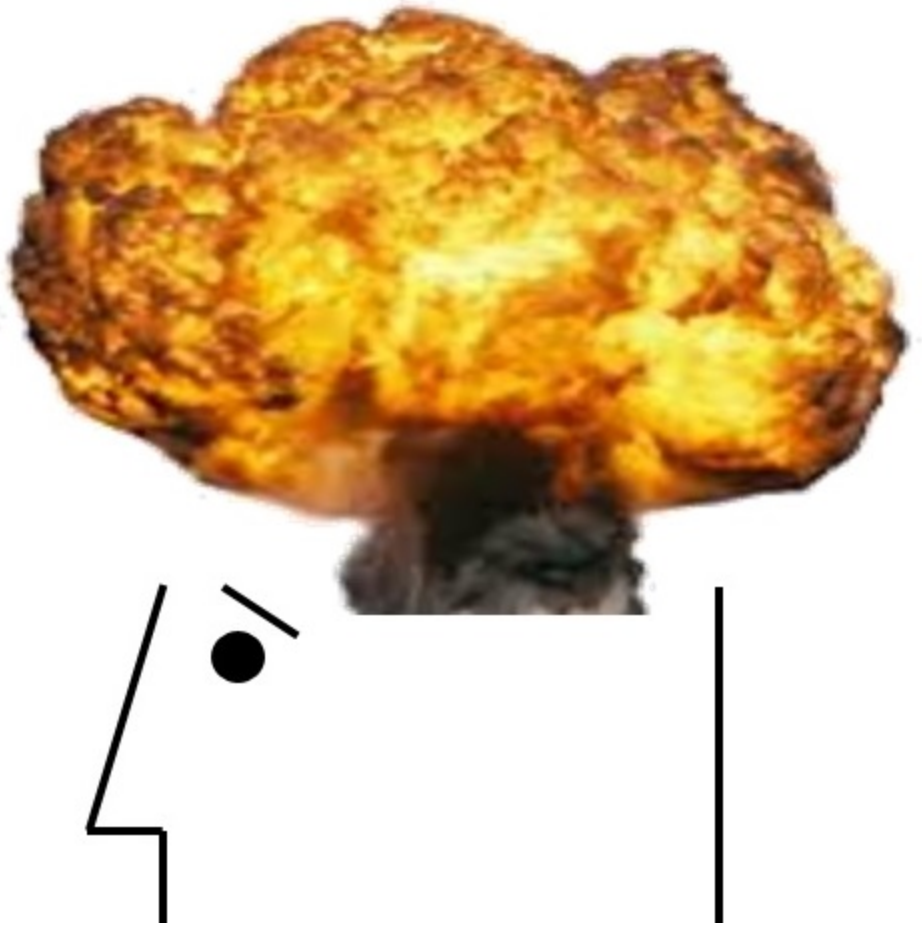
Intel Support

- App Direct Mode
  - Harnesses Optane's persistence
  - Uses SNIA NVM Programming Model
- Memory Mode
  - Not persistent
  - Just like a big huge DRAM
- Special IA instructions
  - Manages cache into PM



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A Path to the Future

Tomorrow's Computing Architectures

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Putting Together the Pieces

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Q & A

Who’s Still Awake?

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