Future of Storage Platform Architecture

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Agenda

- CXL Overview
- CXL for Memory/Storage converged architecture
- Future Storage Architecture
- Summary & Next Steps
CXL Overview

- Open industry standard processor interconnect
- Alternate protocol that runs on standard PCIe PHY
- 3 sub-protocols multiplexed on single link
- High-bandwidth, low-latency
- Coherent interface

Source: Compute Express Link™ (CXL™) specification
CXL for Memory/Storage Converged Architecture

**Type1: Caching Devices/Accelerators**

- CPU
- Accelerator
- Cache
- CXL.io
- CXL.cache
- CXL.memory

**Type2: Accelerators with Memory**

- CPU
- Accelerator
- Cache
- CXL.io
- CXL.cache
- CXL.memory
- Mem

**Type3: Memory Buffers**

- CPU
- Memory Buffer
- CXL.io
- CXL.memory

- Memory Bandwidth/Capacity expansion
- Resource Pooling - Memory/Accelerator
- Disaggregation
- Computational Offloads
  - AI, HPC, Comms
Storage Platform Architecture Opportunities

- High Available architecture for scale out storage using CXL
- Easier Memory persistence to speed up SDS meta-data operations
- Storage/Memory converged device unlocks potential for memory centric usages
- CXL accelerators provide computational offload architecture for storage
Storage Architecture – SDS High Availability

- SDS - shared nothing architecture
- Any node failure triggers cluster wide rebuild/rebalancing
- Takes several hours rehydrate data from peer storage cluster nodes and rebuild meta-data

- Host failure doesn’t trigger cluster wide rebuild
- Meta-data in SCM helps in reducing rebuild time for data
Storage Architecture – Persistence

- Full System persistence required to keep Meta data in memory
- Persistence is Platform/CPU dependent
- Software changes required for SCM persistence
- Block IO persistence is slow for meta-data

- Easier to implement persistence for CXL Memory (e.g., battery backed for power fail)
- Removes Platform / CPU dependence
- Speeds up meta-data operations with DDR latency while achieving persistence
Storage Architecture – SDS Metadata Acceleration

- Avoids complex data protection implementation in software (e.g., transaction logs, rollbacks)
- Meta-data is write intensive – reduces latency significantly

Client

- Mounts network block device
- Issues block io (read/write etc.)

NVMe SSD

- NVMe write (LBA, offset) SGL

CXL Memory Buffer

- Get virtual vol to physical dev/LBA
- Get replication node info
- Commit

Host Storage Software

- Issue write to replica node
- Send storage IO payload to host s/w

NIC (PCIe or CXL)

- Issue IO op (e.g., write for vol at offset with length)

Storage Server

- Write Ack from replica node
- Ack to client

- Write to replica node

NVM (persistence)

- DDR (battery backed)

Client

- Ack to client
- Issue IO op (e.g., write for vol at offset with length)
CXL for Memory/Storage converged architecture

- Disaggregation and Resource Sharing
- Memory hierarchy (Persistent/Volatile)
- P2P Communication
Storage Architecture – Converged Device

- Monolithic - Protocol & Media
- Device training/RAS – Unique to device type
- Software – block v/s memory semantics

- Protocol is late binding decision based on workload requirements
- Converged device training/Platform RAS flows
- Open new usages for SSDs – Memory semantics
Storage Architecture – Computational Offloads

- Compute offload semantics – protocol dependent
- Computational storage – early stages of maturity
- Software changes – intrusive

- CXL for computational storage offloads
- Enable memory and SCM semantics for persistence
- Dual protocol support for backward compatibility
Summary and Next Steps

- CXL opens opportunities for storage architecture innovations
- Storage/Memory converged device unlocks potential for memory centric usages
- CXL accelerators provide computational offload architecture for storage
- CXL device DDR persistence to speed up SDS meta-data operations
- High Available architecture for scale out storage using CXL constructs to reduce cluster wide rebuild/recovery time
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