# Advances in Non-Volatile Storage Technologies

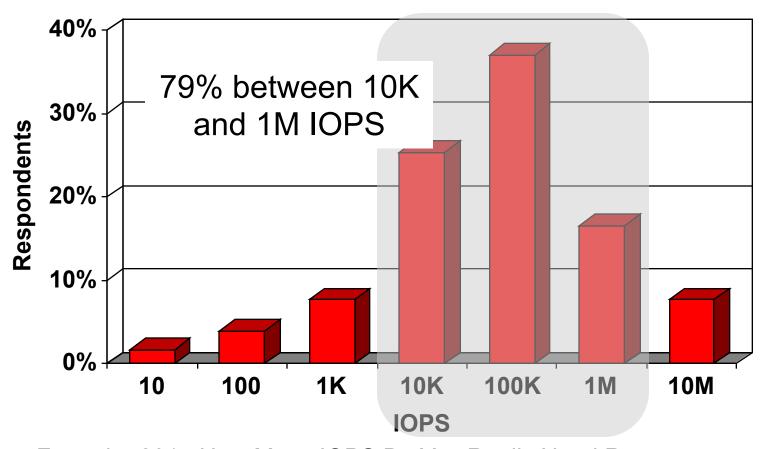
Tom Coughlin
Coughlin Associates
Ed Grochowski, Computer Memory/
Storage Consultant

### Outline

- The Shape of Things to Come
- In Search of New Memories
- Intel/Micron's 3D XPoint Technology
- The Memory is the Computer
- Conclusions

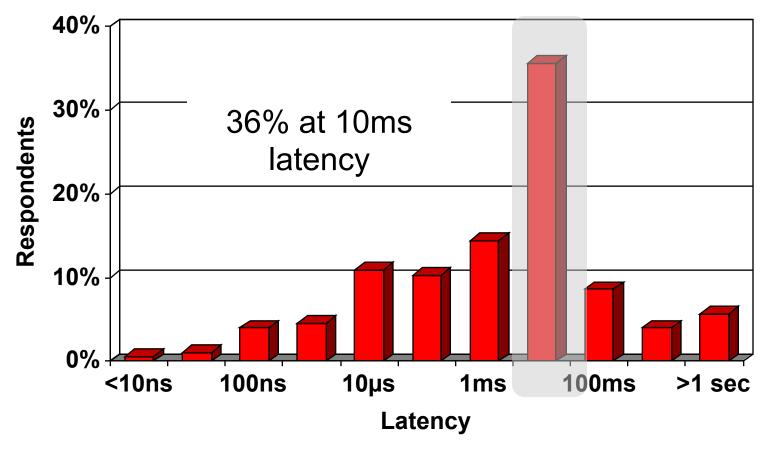


# **IOPS** Required



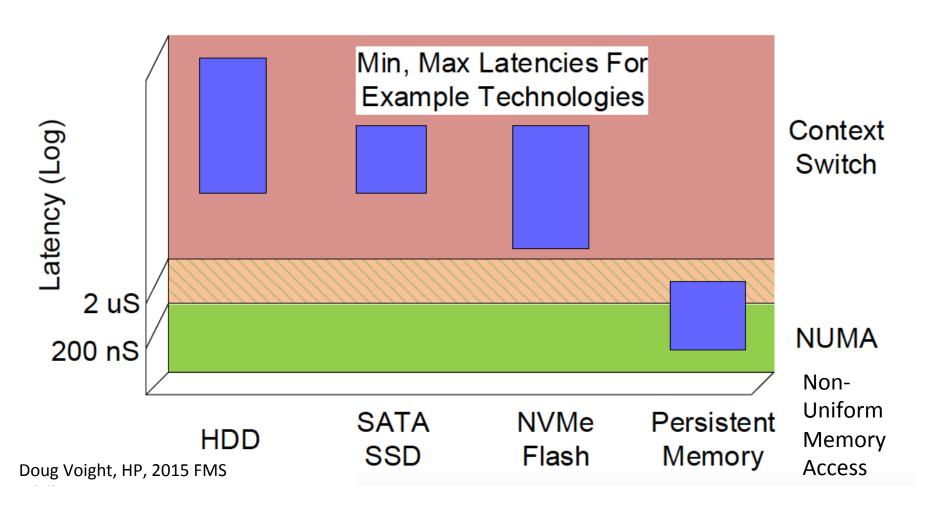
From the 2014 How Many IOPS Do You Really Need Report, Coughlin and Handy, http://www.tomcoughlin.com/techpapers.htm

# Maximum Latency Requirement

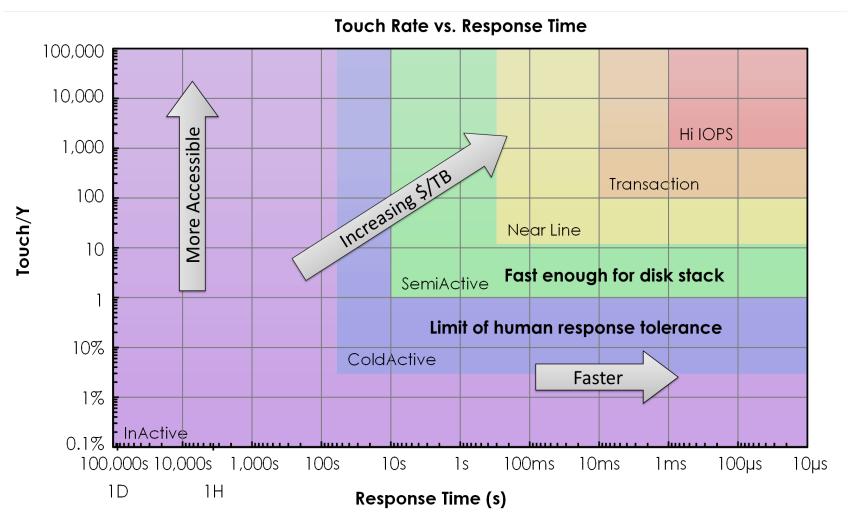


From the 2014 How Many IOPS Do You Really Need Report, Coughlin and Handy, http://www.tomcoughlin.com/techpapers.htm

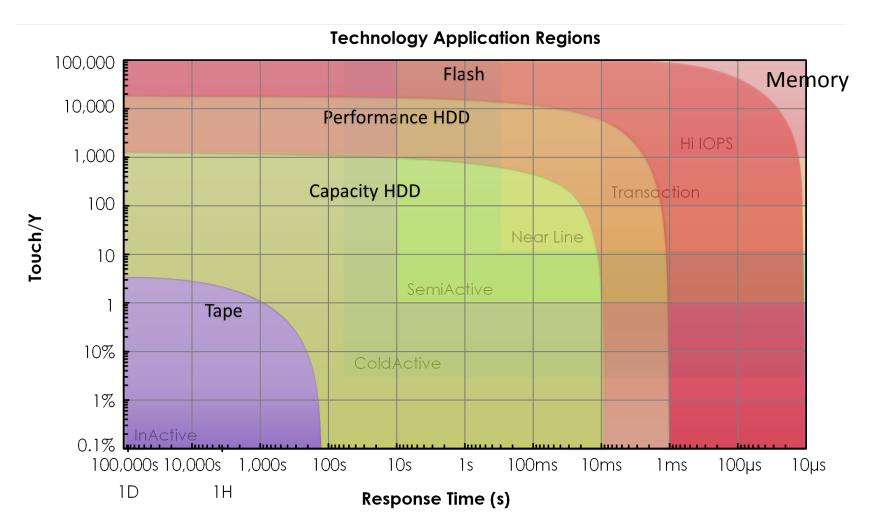
# Latencies Separate Computer Memory from Storage



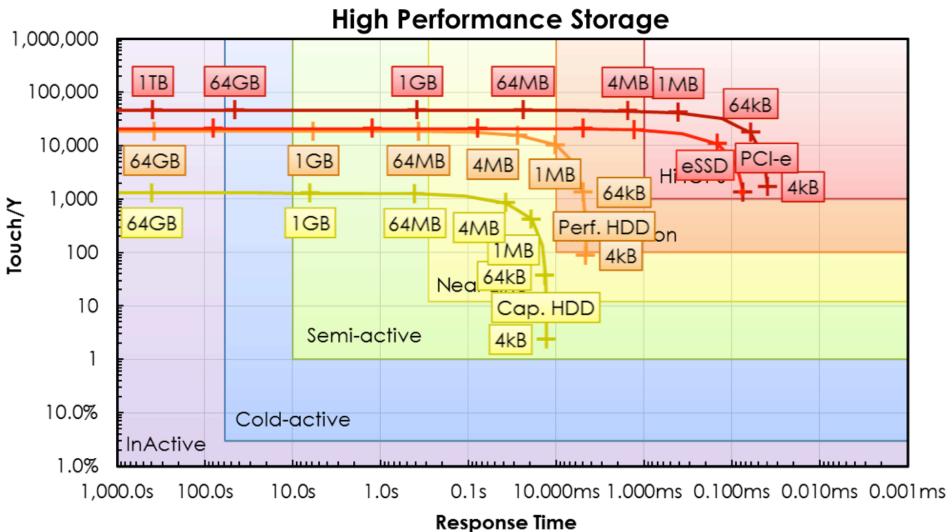
# Touch rate versus response time indicating various types of uses



# Digital storage technologies regions overlaid on the Touch Rate/Response Time chart



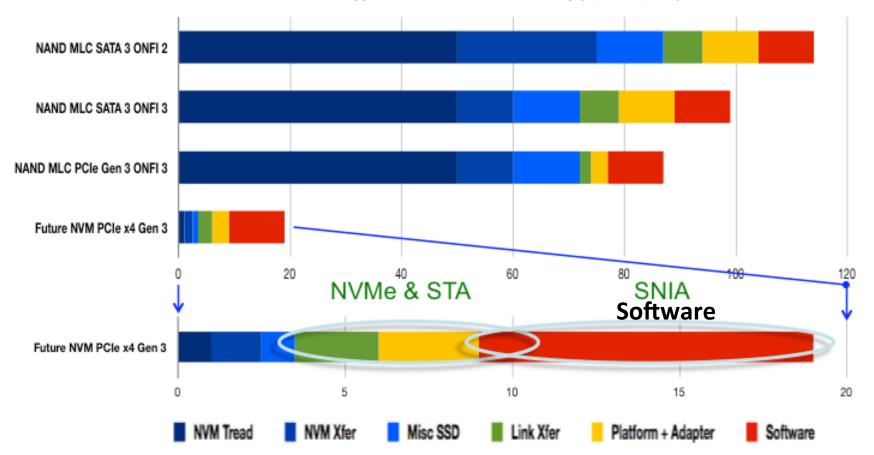
# Ent. SSDs, perf. HDDs and capacity HDDs



# Storage Latency with Current and Future NV Solid State NV Technologies

(from NVMP talk at SNIA Winter Symposium, 2014)

Application to SSD IO Read Latency (us, QD=1, 4KB)



# Implications of Persistent Memory

- NV memory retains its data even when power off—thus instant recovery of state before power down is now possible
- NV memory with the right SW changes can provide much better latencies than current systems and SW
- Non-volatile memory will save power since refreshes not needed
- Persistent memory creates new opportunities to share that memory between different computers or computer chips using Remote Direct Memory Access (RDMA)
- Embedded NVM technology can lead to "logic-in-memory architecture" for future SoC—this can lead to new distributed computer architectures

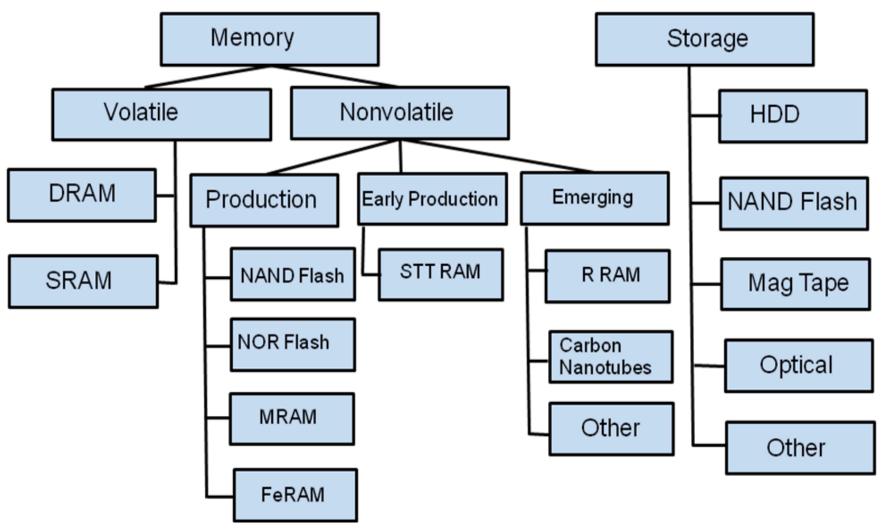
# Challenges of Persistent Memory

- If the memory isn't cleared by rebooting a system, then reboots to recover functionality with corrupted data won't work
- There will need to be a special reboot and clear function that erases and recovers data in memory
- Or, and this may be an even better solution, we need to built devices and software that are selfmonitoring and self correcting so we don't need to reboot in order to retain functionality

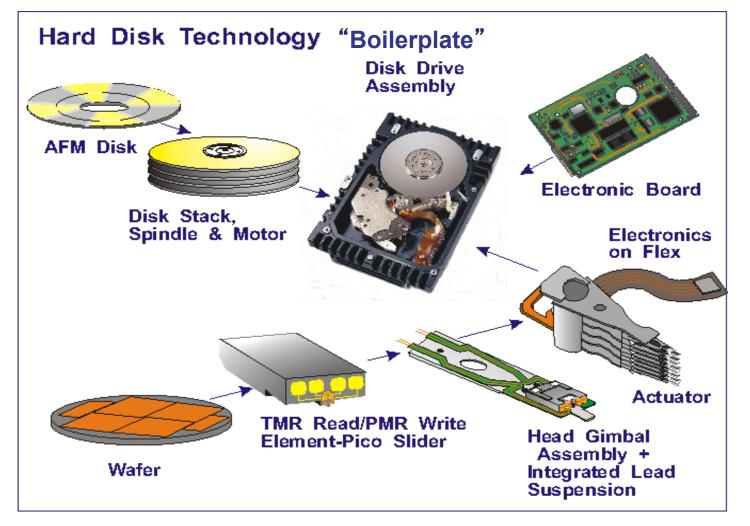


# Memory and Storage Today

2015 Emerging NVM and Their Manufacture Report, Coughlin Associates



## Hard Disk Drives

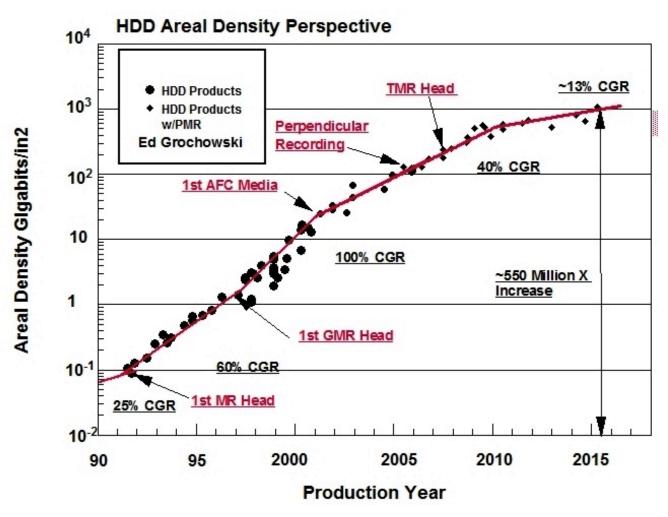


HDD Components

Ed Grochowski

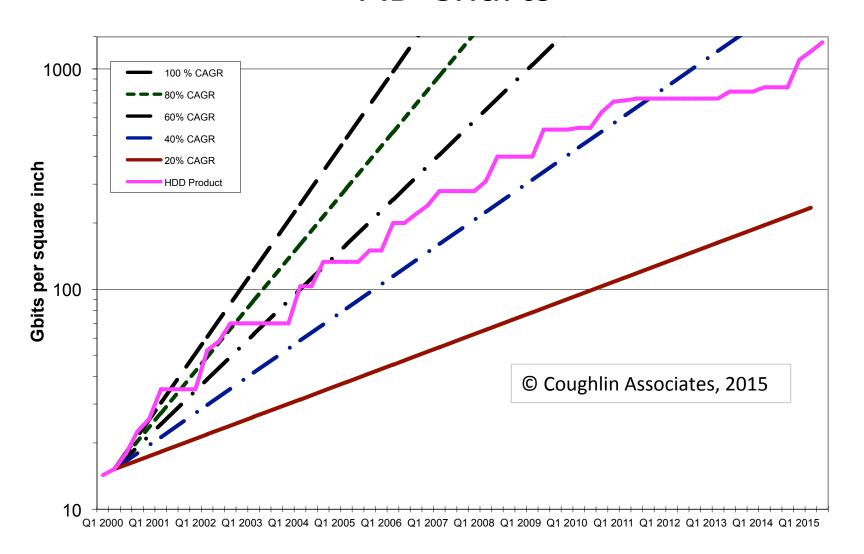
# **HDD Areal Density Growth**





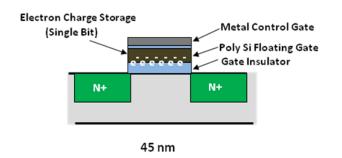
Recent Developments: SMR, HAMR, He-filled HDDs, MAMR with 3D Recording,

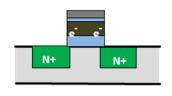
# Actual Quarterly Announced HDD Product AD Charts



# Flash Memory

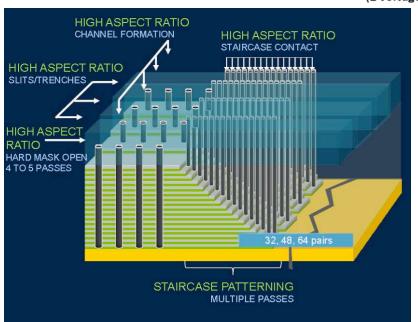
#### **Flash Scaling**

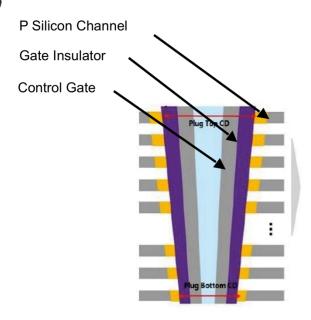




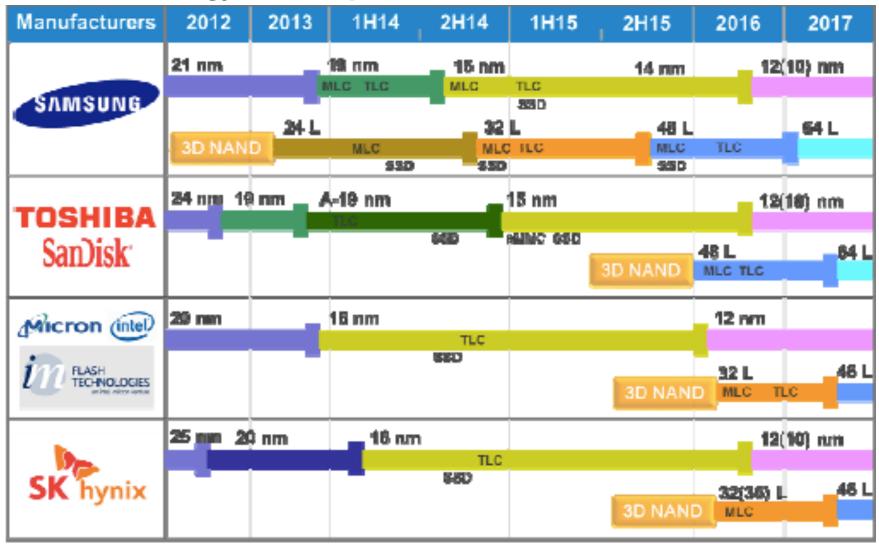
<22 nm

Floating Gate SLC (2 voltage levels)



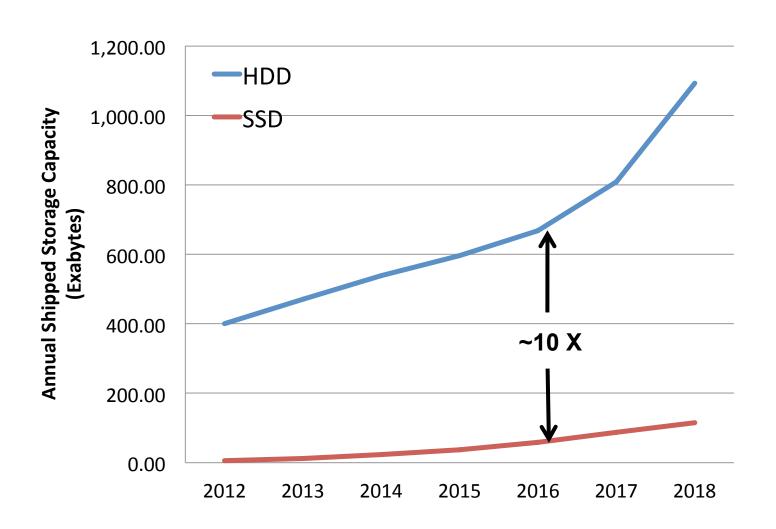


#### **NAND Technology Roadmap**



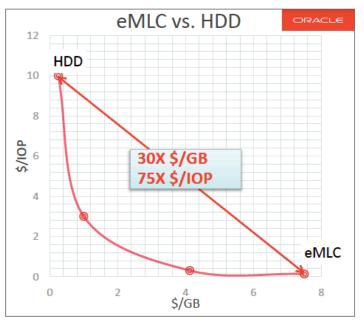
J. Choe FMS 2015

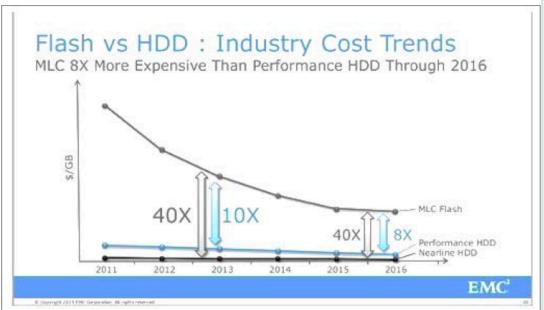
# Annual HDD/SSD Storage Shipments



# Comparisons of Flash and HDDs

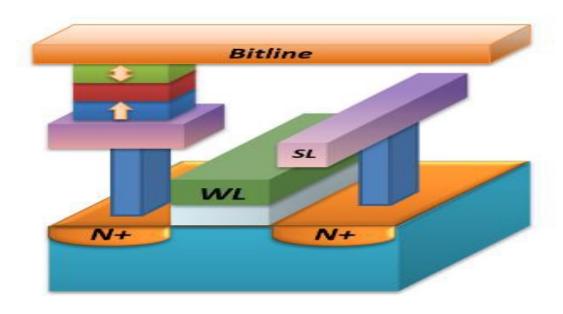
#### Mike Workman Keynote, 2015 FMS





# **Emerging Memory Technology**

- NVM will save power
- Persistent memory enables memory sharing (RDMA)
- Embedded NVM technology can lead to "logic-inmemory architecture"



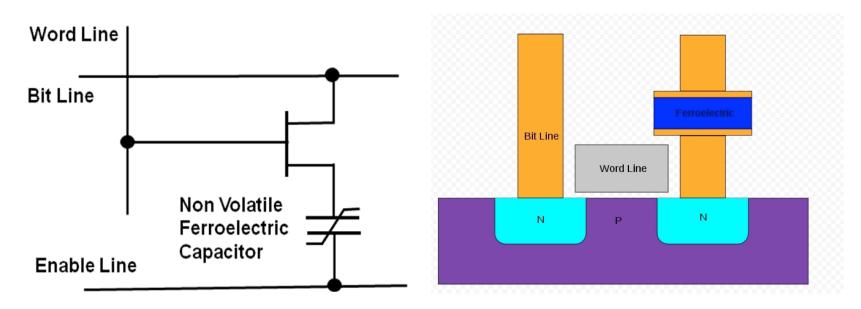
The emerging NVM market could exceed \$2 B by 2019

2014 Emerging NVM Report and Their Manufacture, Coughlin Associates

© 2015 Coughlin Associates

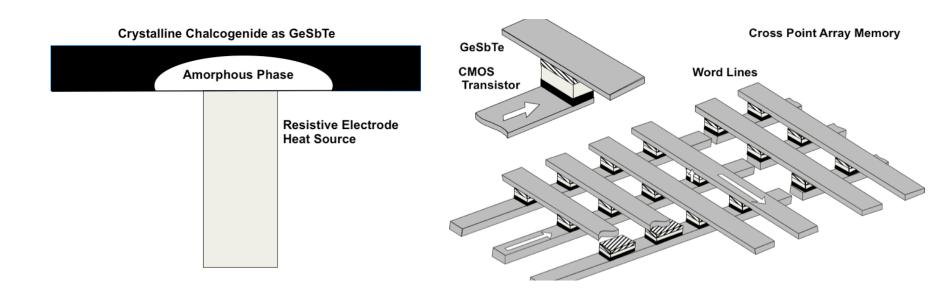
### **FeRAM**





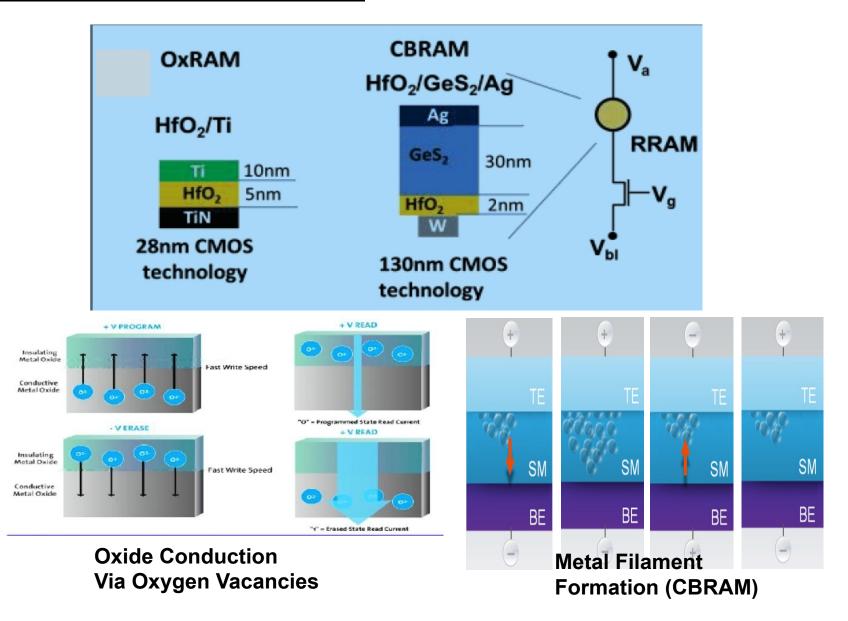
FeRAM products shipping for many years for niche applications, hard to scale density...

# Phase Change Memory (PCM)



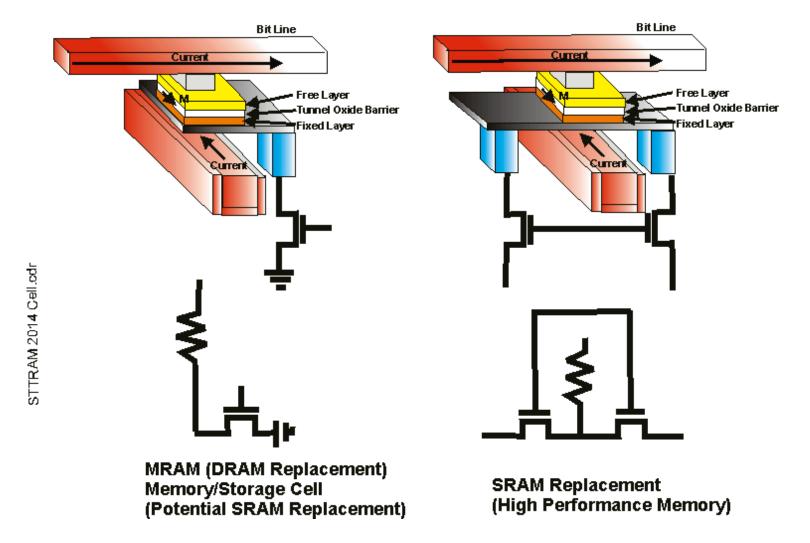
Several industry experts think that Micron/Intel's 3D XPoint Technology is a crossbar phase change memory

#### TYPES OF RRAM TECHNOLOGY

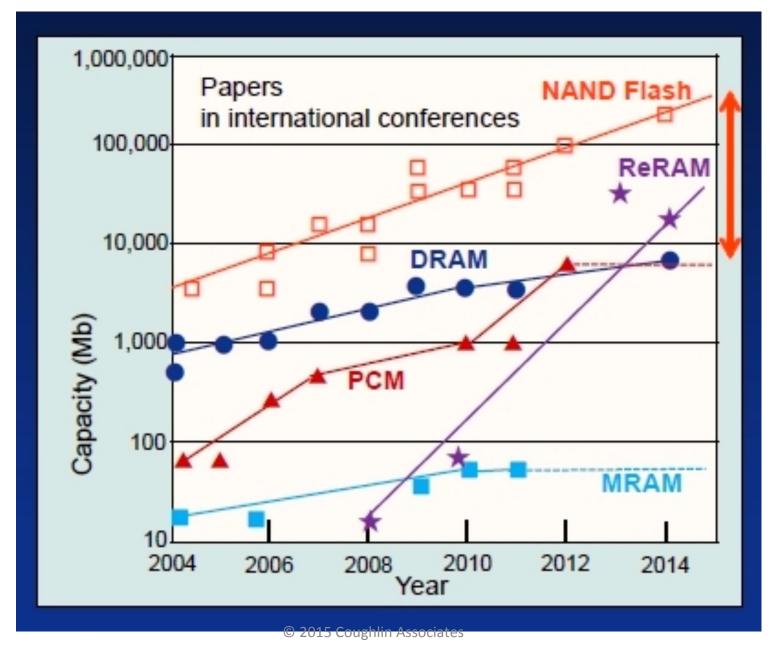


## STT MRAM Replacing DRAM and SRAM

Over 50 M MRAM chips shipped by Everspin

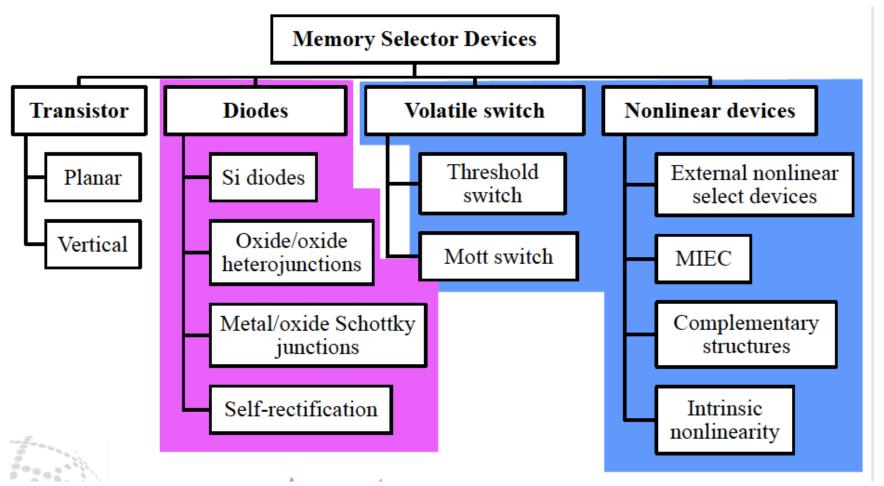


#### **NVM Progress (Amigo Tsutsui, Sony at the 2015 FMS)**



# Memory Selector Device Options

An Chen, 2014 AVS TFUG Seminar

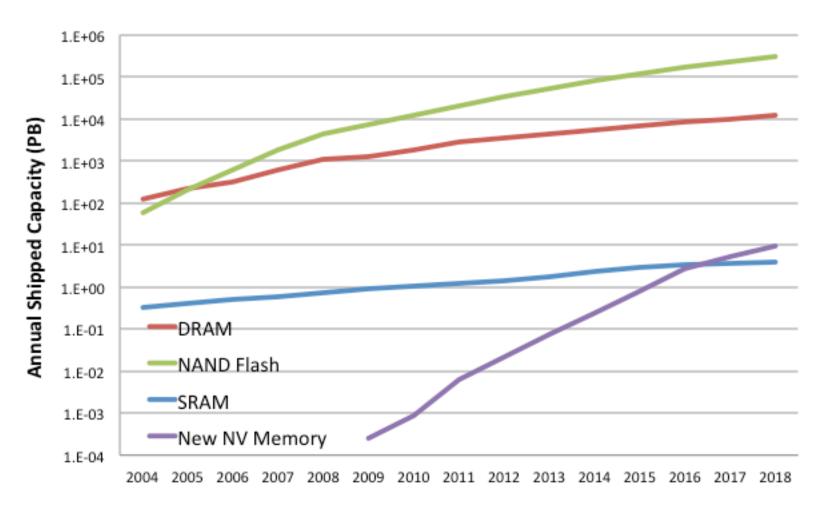


#### **SUMMARY OF STORAGE AND MEMORY TECHNOLOGIES**

	HDD	Flash (SLC)	Flash MLC)	Fe- RAM	M- RAM	PC- RAM	Re- RAM	STT- RAM	Race Track	CNT
Cell Structure	none	1T/0C	1T/0C	1T/1R	1T/1R	1T/1R	1T/1R- 0T/1R (e)	1T/1R	none	1T/1R
Cell Size (F <sup>2</sup> )	0.5	4-5	4-5	16- 32	16- 32	5-8	4-6	4	1 (e)	5(e)
Read Time (ns)	2000	50	50	20- 50	3-20	5-20	10-20	3-15	500	50(e)
Write Erase Time (ns)	500- 1000	1 ms- 0.1 ms	1 ms- 0.1 ms	50	10-20	>30	20	3-15	250	50(e)
Endurance	10 <sup>16</sup>	10 <sup>5</sup>	10 <sup>3</sup>	10 <sup>12</sup>	10 <sup>15</sup>	10 <sup>12</sup>	10 <sup>5</sup>	10 <sup>15</sup>	10 <sup>15</sup> (e)	10 <sup>15</sup>
Write Power	Med	High	Med	Low	High	High	Low	Low	Low (e)	Low (e)
Max.Areal Density Gbits/in2	750- 1000	150	550	0.1	10	200(e)	>200	>400 (e)	1000 (e)	>200 (e)
Voltage Required	3-5V	3.3 V	1.8 V	2-3V	3V	1.5-3V	1.2V	1.5V	3-5V (e)	3-5V (e)
	Existing Products					In Development			Laboratory	

# **Annual Memory Capacity Shipments**

(2014 Emerging NVM Report and Their Manufacture, Coughlin Associates)

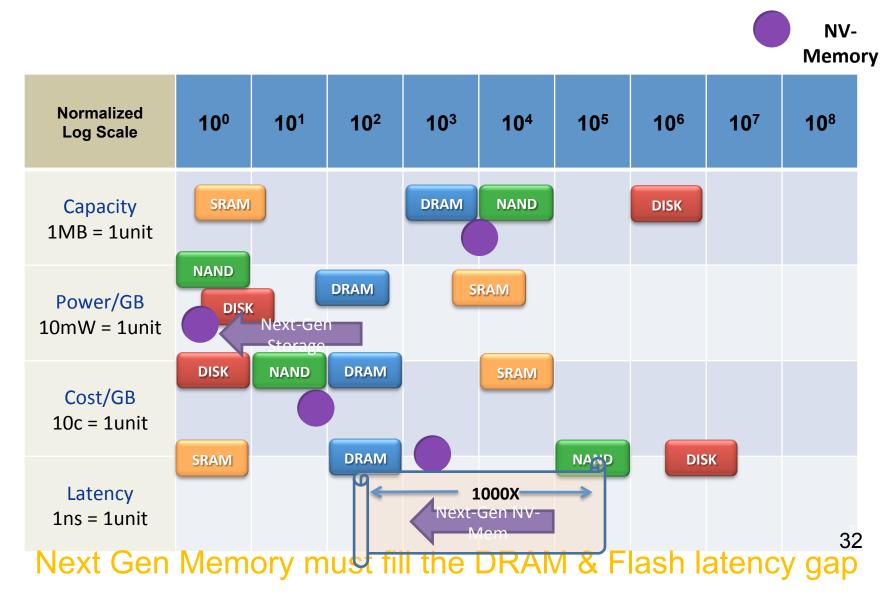


# 3D XPoint Technology

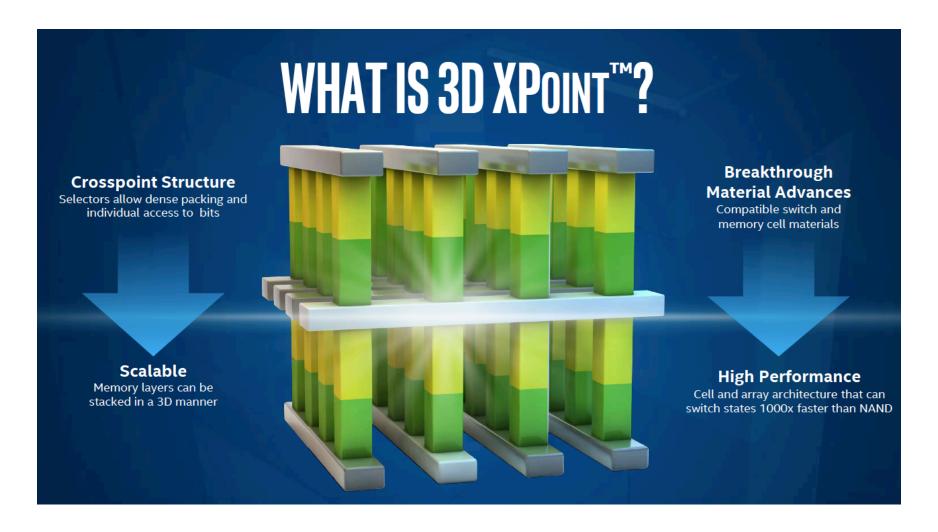
© 2015 Coughlin Assoc

#### Comparison of Memory Technologies

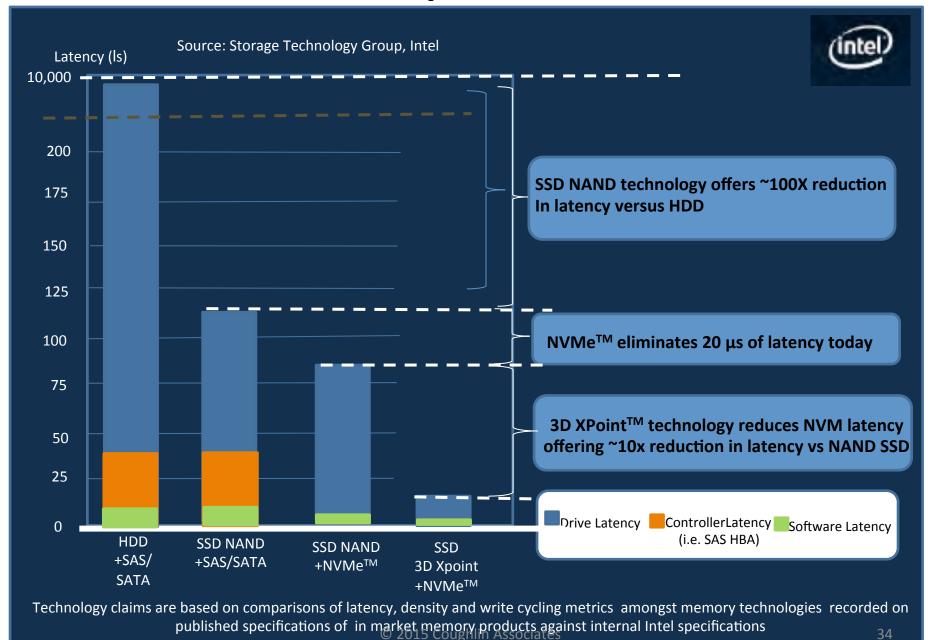
Slide from 2015 Storage Visions Conference



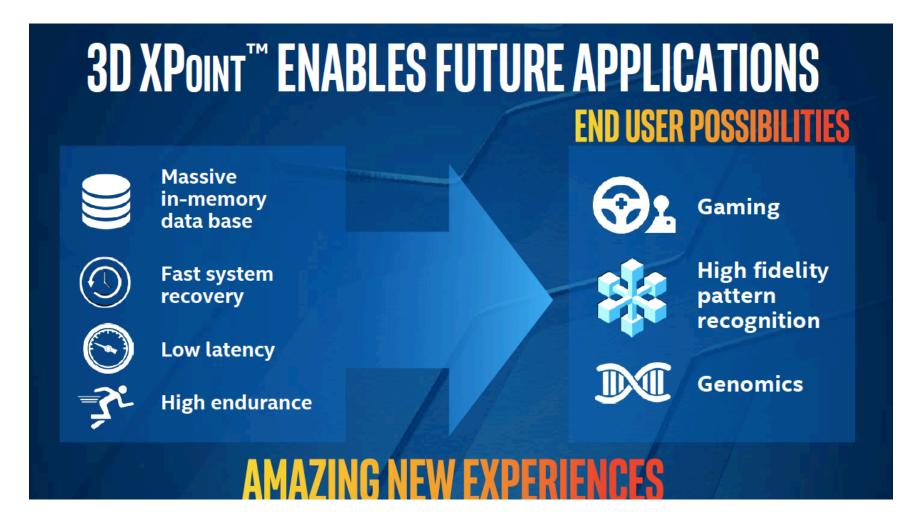
# **3D XPoint Memory**



#### **3D XPoint Comparisons to NAND**



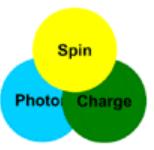
# 3D Xpoint Memory





## **Spintronics**

## **Spintronics (Spin + Charge)**



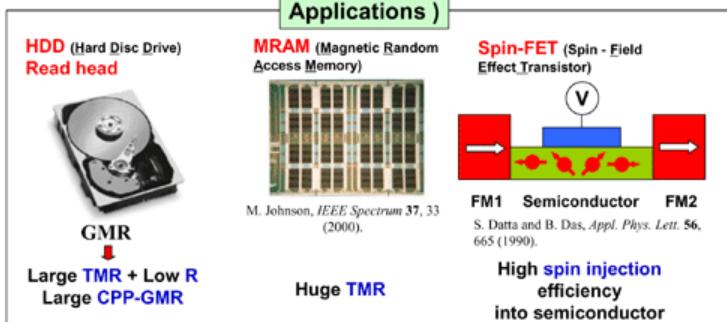
Semiconductor (Charge)



SPINTRONICS

Magnetic materials (Spin)

From Tohoku University in Japan

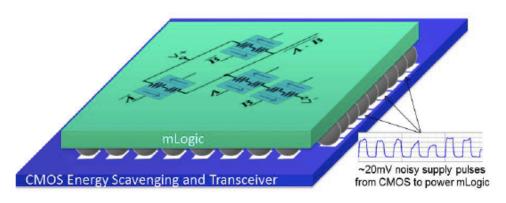


TMR : <u>Tunnel Magnetoresistance</u>

•CPP-GMR : Current Perpendicular to Plane- Giant Magnetoresistance

## Spin-Based Computing

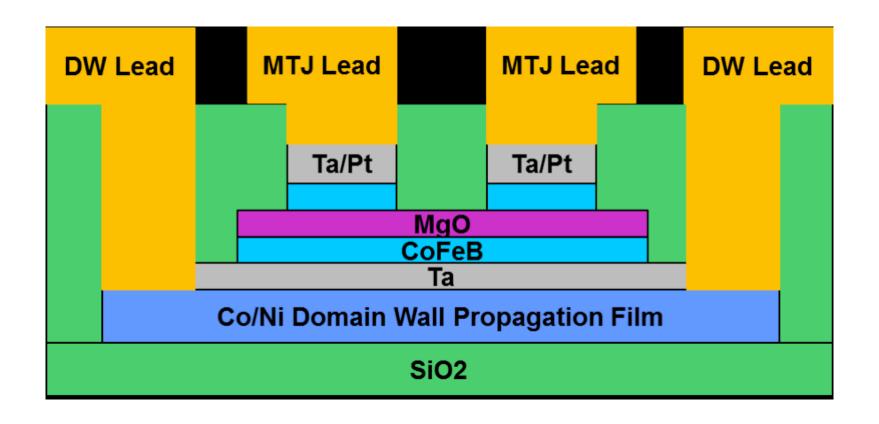
mLogic: All Spin Logic Device and Circuits for Future Electronics, Jimmy Zhu, et. Al, March 2015



- All STT based metallic logic
- Nonvolatile logic states
- Ultra-low pulsed voltage
- Portable & energy-harvesting
- Rad-hard for space applications
- Very low cost manufacturing
- Scalable to 5nm CD



# mCell Spin Logic Unit (J. Zhu, Carnegie Mellon Univ.)



# STT Logic Application (Reducing Dark Silicon)

# CPU/Multiple Memories CPU/STT RAM/Logic CPU STT RAM/Logic CPU STT RAM/Logic Inactive CPU Analog

# What if Spin Transfer Replaced Charge Transfer (Current)?

- Spin transfer would not generate the heat that electrical currents generate
- This allow building powerful devices in small spaces
- Spin could be used for both processing and memory/storage

## Conclusions

- Faster memory/storage is needed for modern applications
- The storage/memory landscape has more options than ever—e.g. 3D XPoint
- Non-volatile memories will replace volatile memories
- NVM and processors want to come together
- Spin-based electronics are one example of a technology that could put memory and processing in one device

## References

- 2014 How Many IOPS Do You Really Need Report, Coughlin and Handy, Coughlin Associates
- 2014 and 2015 Emerging NVM Report and Their Manufacture, Coughlin Associates
- 2015 Storage Visions Conference Presentations
- Touch Rate: A metric for analyzing storage system performance, Steven Heltzer and Tom Coughlin, 2015
- Information on all these documents are available at: <a href="http://www.tomcoughlin.com/techpapers.htm">http://www.tomcoughlin.com/techpapers.htm</a>

