

## Persistent Memory what developers need to know

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### Persistent Memory Overview

## Non-Volatile Memory (NVM) Programming Model

# Non-Volatile DIMM (NVDIMM) SD® 2018 Storage Developer Conference EMEA. All Rights Reserved.

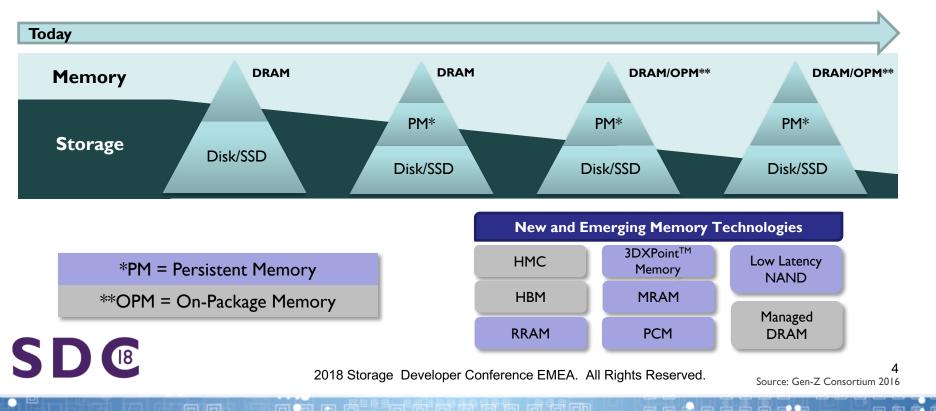
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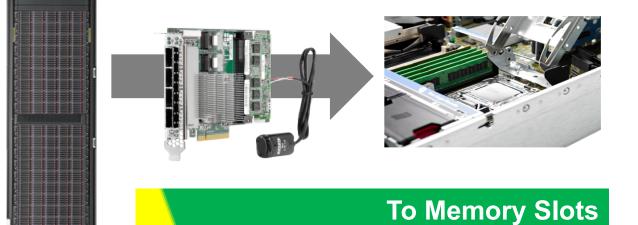
# The Trend: Memory & Storage Convergence

□ Volatile and non-volatile technologies are continuing to converge



## **Persistent Memory (PM) Vision**

### **Persistent Memory Brings Storage**







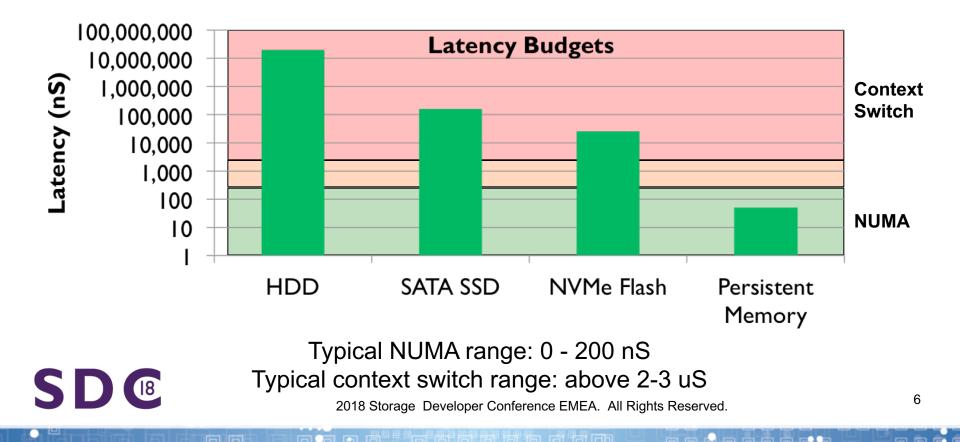
For system acceleration

For real-time data capture, analysis and intelligent response

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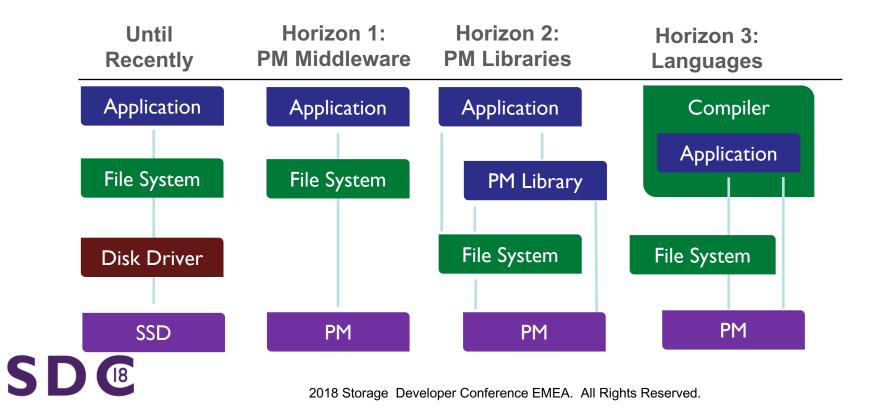
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## **Storage vs. Memory**



## **Application Horizons**

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## Persistent Memory (PM) Characteristics

- Byte addressable from programmer's point of view
- Provides Load/Store access
- Has Memory-like performance
- Supports DMA including RDMA
- Not Prone to unexpected latencies associated with demand paging or page caching
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## NVM Programming Model – Writing Applications for Persistent Memory

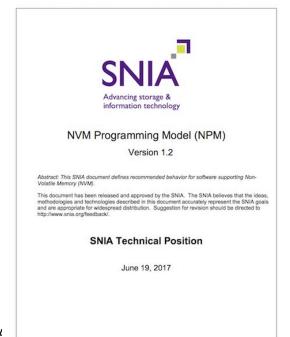
Role of the NVM Programming Model Rally the industry around a view of Persistent Memory that is:

- Application centric
- Vendor neutral
- Achievable today
- Beyond storage
  - Applications
  - Memory

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Networking/Fabrics

Processors



## NVM Programming Model TWG -Mission

- Accelerate the availability of software that enables Persistent Memory hardware.
  - Hardware includes SSD's and PM
  - Software spans applications (user-space) and OS's (kernel-space)

### Create the NVM Programming Model

- Describes application visible behaviors
- Allows API's to align with OS's

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Exposes opportunities in networks and processors

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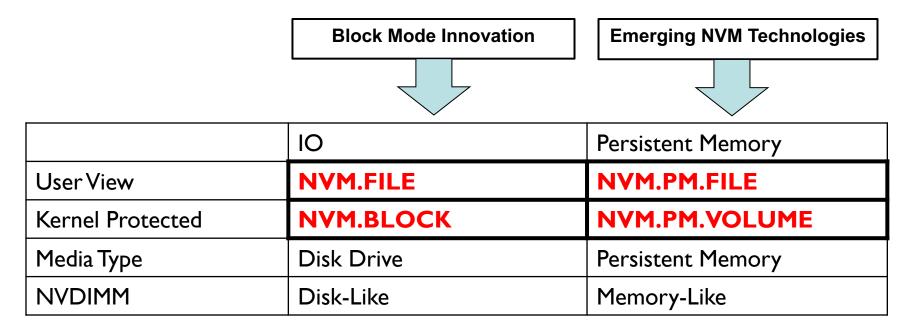
## **SNIA NVM Programming Model**

- Version 1.2 approved by SNIA in June 2017
  - http://www.snia.org/tech\_activities/standards/curr\_standards/npm
- Expose new block and file features to applications
  - Atomicity capability and granularity
  - Thin provisioning management
- Use of memory mapped files for persistent memory
  - Existing abstraction that can act as a bridge
  - Limits the scope of application re-invention
  - Open source implementations available
- Programming Model, not API
  - Described in terms of attributes, actions and use cases

Implementations map actions and attributes to API's

## The NVM Programming Model Has 4 Modes

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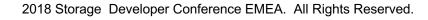


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## **Programming Model Modes**

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- NVM.FILE and NVM.BLOCK modes use IO
  - Data is read or written using RAM buffers
  - Software controls how to wait (context switch or poll)
  - Status is explicitly checked by software
- NVM.PM.\* (FILE and VOLUME) modes enable Load/Store
  - Data is loaded into or stored from processor registers
  - Processor makes software wait for data during instruction
  - No status checking errors generate exceptions



## User mode

## File and Block Mode Extensions

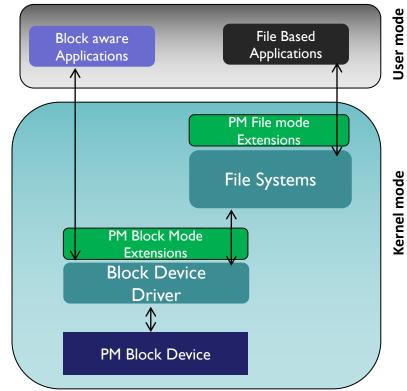
### NVM.BLOCK Mode

- Targeted for file systems and block-aware applications
- Atomic writes
- Length and alignment granularities
- Thin provisioning management

### NVM.FILE Mode

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- Targeted for file based apps.
- Discovery and use of atomic write features
- Discovery of granularities



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## **Persistent Memory (PM) Modes**

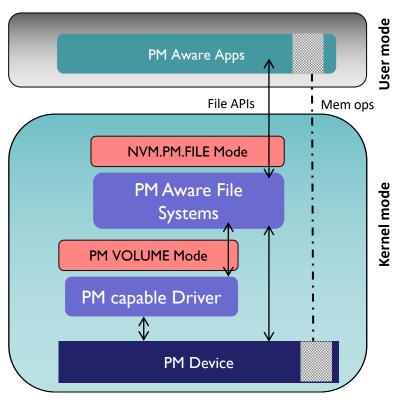
- NVM.PM.VOLUME Mode
  - Software abstraction for persistent memory hardware
  - Address ranges
  - Thin provisioning management

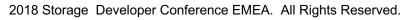
### NVM.PM.FILE Mode

Application behavior for accessing PM

- Mapping PM files to application address space
- Syncing PM files

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## Map and Sync

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- Associates memory addresses with open file
- Caller may request specific address

### Sync

- Flush CPU cache for indicated range
- Additional Sync types
- Optimized Flush multiple ranges from user space
- Optimized Flush and Verify Optimized flush with read back from media

### Warning! Sync does not guarantee order

- Parts of CPU cache may be flushed out of order
- This may occur before the sync action is taken by the application

Sync only guarantees that all data in the indicated range has been flushed some time before the sync completes

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## **Failure Atomicity**

### Current processor + memory systems

- □ Guarantee inter-process consistency (SMP)
- But only provide limited atomicity with respect to failure
  - □ System reset/restart/crash
  - Power Failure

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Memory Failure

### ■ Failure atomicity is processor architecture specific

- Processors provide failure atomicity of aligned fundamental data types
- □ Fundamental data types include pointers and integers

- PM programs use these to create larger atomic updates or transactions
- Fallback is an additional checksum or CRC

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## **Ongoing SNIA NVMP TWG Work**

- NVM Programming Model Specification
  - NVM Interfaces between OS components
  - □ Application Interfaces to NVM related OS, hypervisor and hardware components
- Remote Access for High Availability white paper
  - Create models and requirements for communication with remote persistent memory for the purpose of High Availability
- □ Asynchronous Flush, Persistence Failure
  - Describe considerations for supporting atomics and transactions using extensions to the NVM Programming Model Specification
- PM Security for Multi-Tenancy

- Describe models for PM security when multiple tenants are present
- See companion SNIA Storage Developer Conference talk
  - https://www.snia.org/events/storage-developer/presentations17

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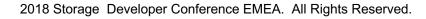
□ The NVM Programming Model is aligning the industry (<u>http://pmem.io/</u>)

- Gaining common terminology
- Not forcing specific APIs
- http://snia.org/forums/sssi/nvmp
- What are we doing with it?

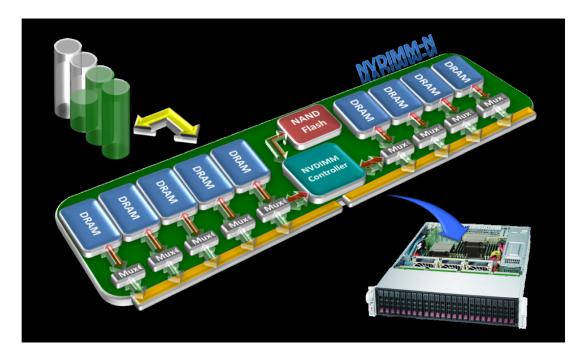
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- PM models expose it
  - DAX-aware file-systems in Linux (see FS\_DAX for more info)
- New PM models build on existing ones

- Linux Pmem Examples (see examples folder) <u>https://github.com/pmem/nvml</u>
- □ New TWG work items
- Emerging technologies will drive increasing work in this area as cost comes down (e.g. materials and memory-centric fabrics)



## **NVDIMM Example**



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## NVDIMM-N

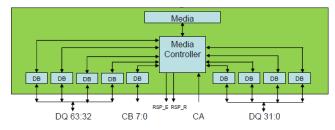


Host has direct access to DRAM

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- CNTLR moves DRAM data to Flash on power fail
- Requires backup power (typically 10's of seconds)
- CNTLR restores DRAM data from Flash on next boot
- **Communication through SMBus (JEDEC standard)**
- Byte-addressable DRAM for lowest latency with NAND for persistence backup

### NVDIMM-P



Block diagram example, JEDEC Server Forum Jul'17

- NVDIMM-P interface specification targeting persistent memories and high capacity DRAM memory on DDR4 and DDR5 channels
- It extends the DDR protocol to enable transactional access

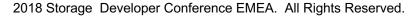
- Host is decoupled from the media
- Multiple media types supported
- Supports any latency (ns ~ us)
- JEDEC specification publication in 2018

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## **NVDIMM-N Applications**

- In Memory Database: Journaling, reduced recovery time, Ex-large tables
- Traditional Database: Log acceleration by write combining and caching
- Enterprise Storage: Tiering, caching, write buffering and meta data storage
- Virtualization: Higher VM consolidation with greater memory density
- High-Performance Computing: Check point acceleration and/or elimination

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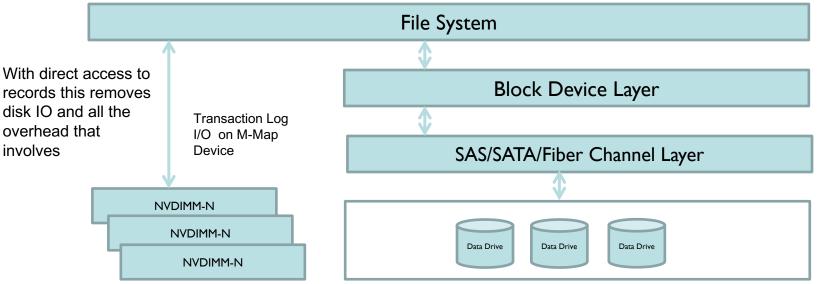




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## **NVDIMM-N Use Case** File System Transaction Log

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A transaction log is a history of actions executed by a DBMS used to guarantee Atomicity, Consistency, Isolation, and Durability (ACID) over a hardware failure. When these logs can be stored in NVDIMMs vs storage then system performance can be dramatically improved.

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## Linux Kernel 4.4+ NVDIMM-N OS Support



- Linux 4.4 + subsystems added support of NVDIMMs
- NVDIMM modules presented as device links: /dev/pmem0, /dev/pmem1

QEMO support (experimental)

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XFS-DAX and EXT4-DAX available

DAXFile syst<br/>persisterBTT (Block, Atomic)Block Tr<br/>have an<br/>bytes. Ti<br/>block dePMEMA system<br/>of PMEN<br/>DIMMs.BLKA set of<br/>access i

File system extensions to bypass the page cache and block layer to memory map persistent memory, from a PMEM block device, directly into a process address space.

Block Translation Table: Persistent memory is byte addressable. Existing software may have an expectation that the power-fail-atomicity of writes is at least one sector, 512 bytes. The BTT is an indirection table with atomic update semantics to front a PMEM/BLK block device driver and present arbitrary atomic sector sizes.

A system-physical-address range where writes are persistent. A block device composed of PMEM is capable of DAX. A PMEM address range may span an interleave of several DIMMs.

A set of one or more programmable memory mapped apertures provided by a DIMM to access its media. This indirection precludes the performance benefit of interleaving, but enables DIMM-bounded failure modes.

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## Windows NVDIMM-N OS Support



### Windows Server 2016 supports DDR4 NVDIMM-N

### Block Mode

- No code change, fast I/O device (4K sectors)
- Still have software overhead of I/O path

### Direct Access

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- Achieve full performance potential of NVDIMM using memory-mapped files on Direct Access volumes (NTFS-DAX)
- No I/O, no queueing, no async reads/writes

### More info on Windows NVDIMM-N support:

- https://channel9.msdn.com/events/build/2016/p466
- https://channel9.msdn.com/events/build/2016/p470

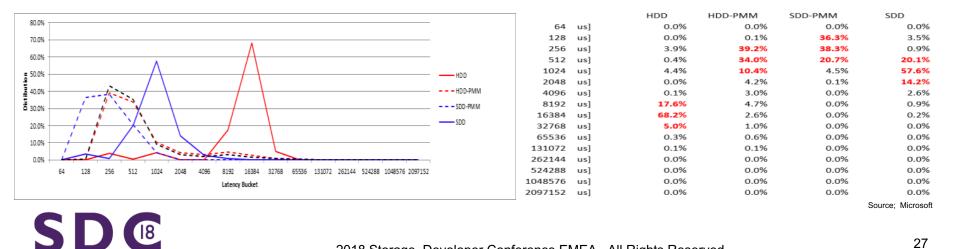
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## **Application Benefits – Windows Example**

### Tail of Log in SQL 2016

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- Writes updates to SQL log through persistent memory first
- Uses memory instructions to issue log updates to persistent memory directly •
- Utilizes memory-mapped files on NTFS Direct Access (DAX) volume ٠



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## Summary

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- The NVM Programming Model is perfect for NVDIMMs
  - Block and File mode atomicity features
  - PM Mode memory mapped storage
- Use the NVM programming model with NVDIMMs
  - Enable a path forward for applications
  - Lead the way to innovation in NVM optimized software

### **SNIA-at-a-Glance**



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## **Thank You!**

# Visit <u>snia.org/PM</u> for the latest on SNIA Persistent Memory activities