

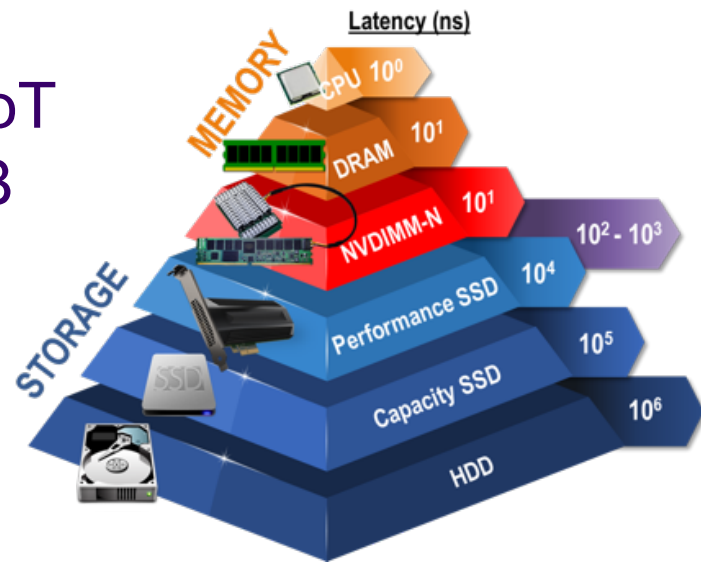
A Brief Introduction to Persistent Memory



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The Problem with Storage

- Storage IO is slow, big and cheap
- DRAM is fast, small & expensive
- Machine Learning, Big Data and IoT demand nanosecond latency & PB scale
- There's a layer missing



SDC 20
SNIA EMEA



Everyone should know...

➤ Persistent memory...

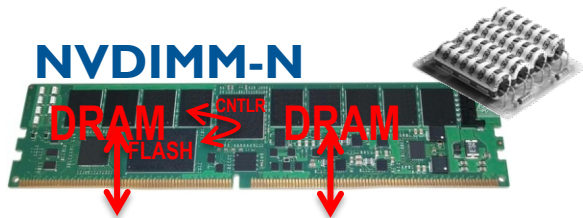
- ◆ Allows load/store access like memory
- ◆ Is persistent like storage
- ◆ Exposed to applications using SNIA NVM programming model

➤ What persistent memory isn't:

- ◆ Something that can only speak blocks (like a disk/SSD)
- ◆ Something that is too slow for load/store access
 - That is: would reasonably stall the CPU waiting for a load to complete

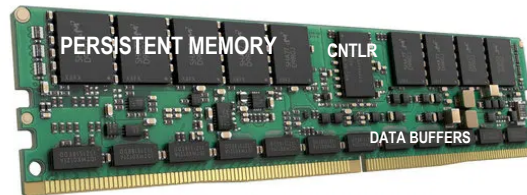
JEDEC-Defined NVDIMM Types

NVDIMM-N

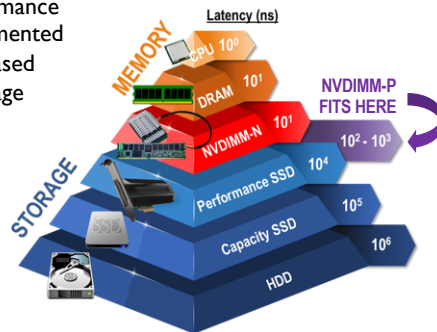


- Host has direct access to DRAM
- NAND flash is only used for backup
- Capacity = DRAM (10's - 100's GB)
- Latency = DRAM (10's of nanoseconds)
- Endurance = DRAM (effectively infinite)
- No impact to memory bus performance
- Low cost controller can be implemented
- Specifications completed and released
- Ecosystem moving into mature stage

NVDIMM-P

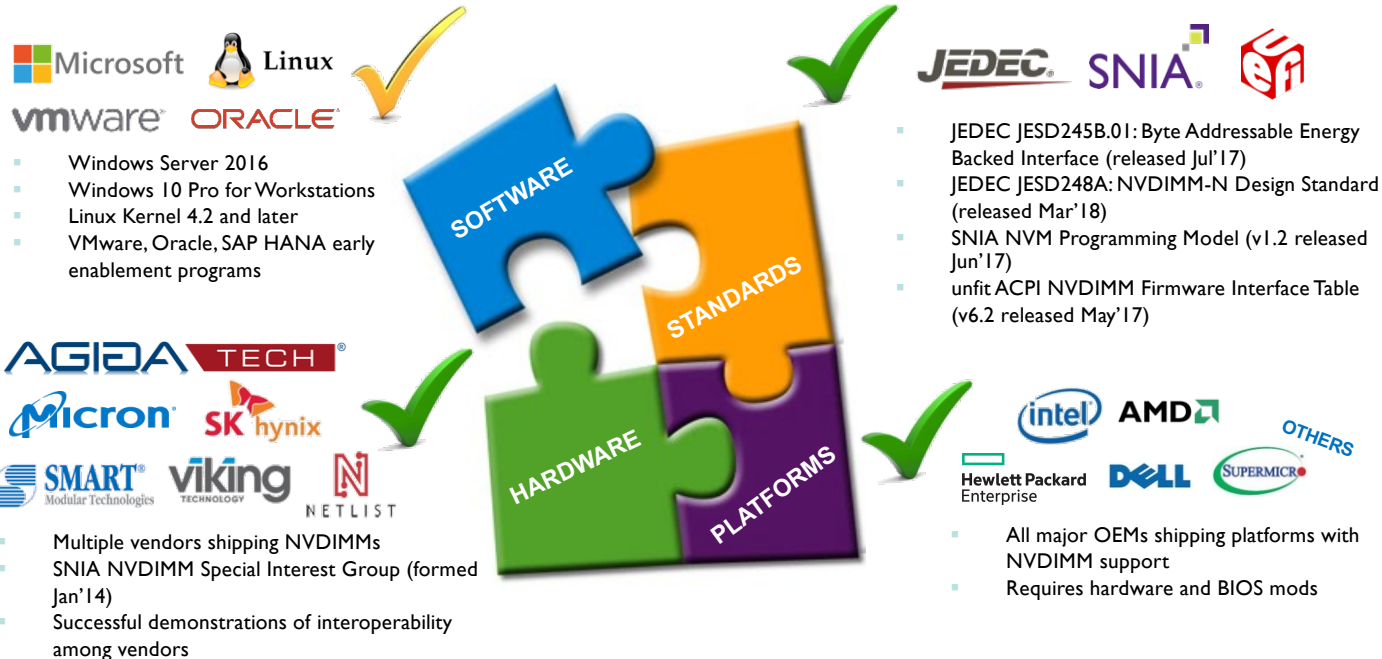


- Host is decoupled from the media (agnostic to PM type)
- New protocol to "hide" non-deterministic access
- Capacity = PM (100's GB+ to 10's TB)
- Latency = PM (>> 10's of nanoseconds)
- Endurance = PM (finite)



NVDIMM Types Are Complementary, Not Competing

A Fundamental Change Requires An Ecosystem



- **Hardware (JEDEC, Others)**
 - ◆ Supporting early development
 - ◆ Ongoing requirements
 - ◆ Form factors, interfaces
- **Software support (SNIA, Others)**
 - ◆ O/S support
 - ◆ Application program support

➤ Using PM as a fast SSD

- ◆ Storage APIs work as expected
- ◆ Memory-mapping files will page them into DRAM

➤ Using PM as DAX

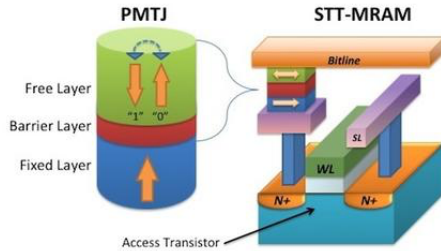
- ◆ Storage APIs work as expected
- ◆ No paging (DAX stands for “Direct Access”)

➤ Using PM as volatile capacity

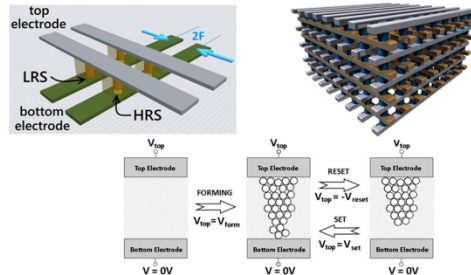
- ◆ Just big main memory
- ◆ Vendor-specific feature

Many Emerging Memory Types

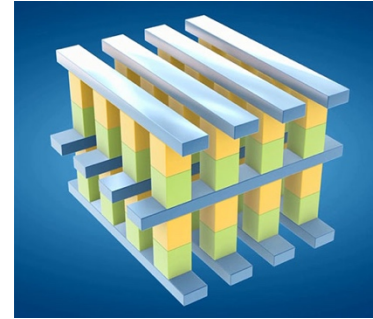
MRAM



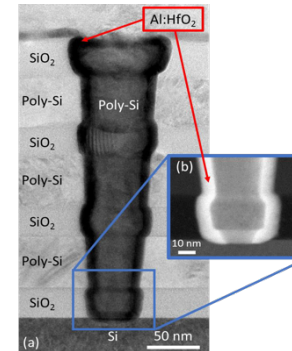
ReRAM



PCM



FRAM



Ongoing Hardware Requirements

- Nonuniform Memory Architecture: “NUMA”
- MMU redesign
- Faster CPU context switches needed
 - ◆ Use polling for now
- Updated DDR4 bus, DDR5 “RSN”
 - ◆ Intel has developed proprietary DDR-T
 - “Transactional”
 - ◆ Support for non-deterministic access times

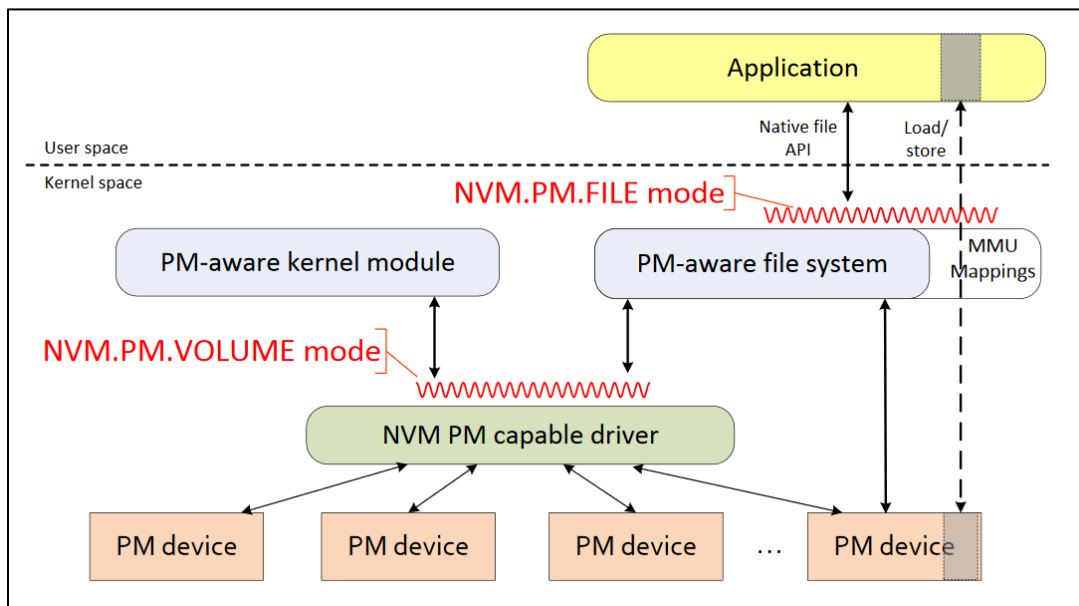
- Discussion on tech mailing list re async callbacks reminded me of this

There are only 3 hard problems in computer science.

0. Cache management
1. Naming things
1. Off by one errors
7. Async callbacks

➤ SNIA's Persistent Memory Programming Model

- ◆ <https://www.SNIA.org/PM>



SNIA's Persistent Memory Progress

➤ 2019

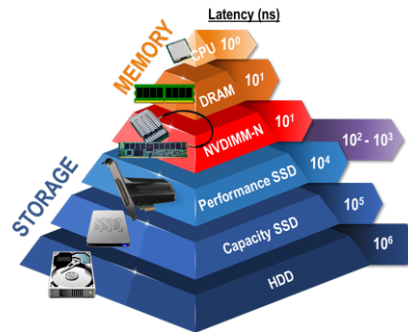
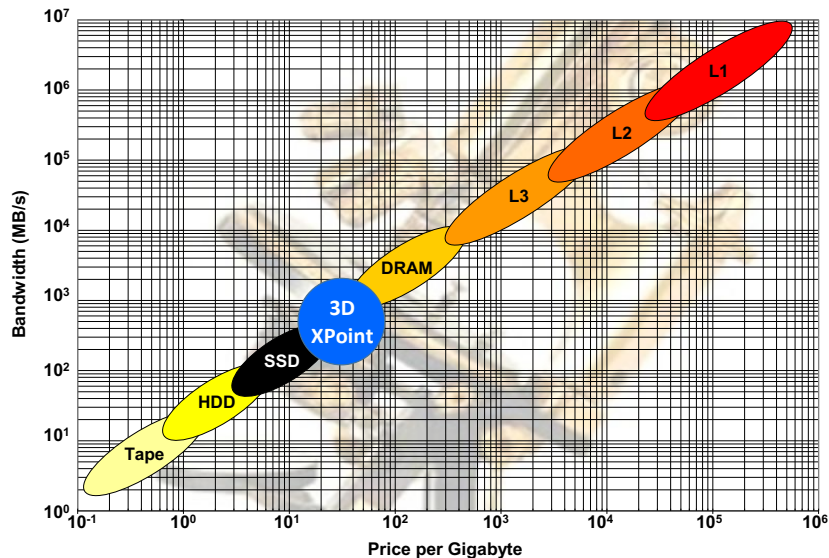
- ◆ PM Programing Hackathon and Workshops launched
- ◆ Work on PM software interface specifications
 - › Developed PMDK
- ◆ Persistent Memory Summit
 - › One running this week at SDC EMEA 2020
- ◆ White papers

➤ Future

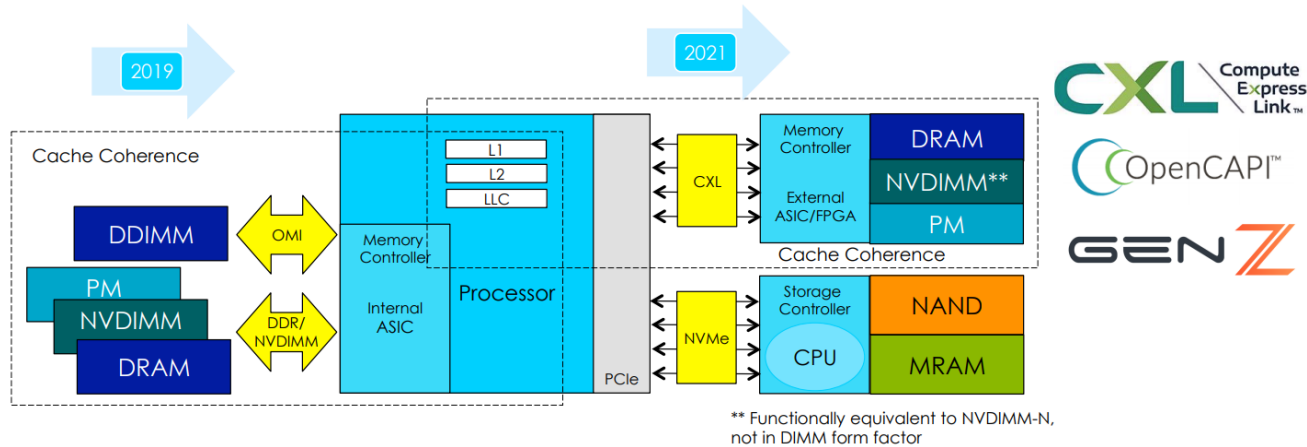
- ◆ Define Remote PM Programming Model (i.e. RDMA)
- ◆ Updates to current PM Programming Model

3D XPoint Must Be Priced Below DRAM

Otherwise People will Just Buy DRAM



PM Future



- Today memory is direct-attached to the CPU
- New emerging interfaces will add high-speed differential CPU-attach options
- Systems will be aware of what type of memory or storage is available and how it is connected
- Lots of new types of memory, persistent memory and storage products are possible!

Want to learn more about PM?

- SNIA – Persistent Memory Resource Page

<https://www.snia.org/PM>

- 2020 Persistent Memory Summit

<https://www.snia.org/pm-summit>

➤ SNIA EMEA organizes & hosts SDC EMEA

- ◆ Storage Developer Conference
February 4-5 2020
Tel Aviv, Israel
- ◆ <https://www.snia.org/events/sdcemea>
- ◆ Platform for the storage development community to come together and share knowledge
- ◆ Educations sessions delivered by storage developers

➤ Features

- ◆ SMB3 IO Lab
- ◆ Persistent Memory Hackathon
- ◆ SNIA Education tracks
- ◆ Local Storagebeers meetup

Questions?