BladeServer

Base Specification
For
Switch Module Subsystems

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1 Preface

1.1 Introduction

This document specifies the mechanical, electrical, logical, management and functional aspects of Switch Modules for compatibility with BladeServer Chassis platforms and related subsystems. The term "Switch Module" is generic and may also be applicable to special function Modules that provide a specific function in common with the Processor Blade subsystems.

Specific functional requirements for unique applications, such as an Ethernet Switch, are not addressed in this document but will be addressed in applicable product requirements and/or specification documents.

Multiple BladeServer Chassis have been developed, addressing a variety of market segments. All use the same form-factor and electrical interface for the switch modules. However, requirements may be different based on the segment. This document specifies both enterprise (datacenter or NEBS level 1) and telecom (NEBS Level 3 and ETSI) environmental requirements. Developers of switch modules are responsible for establishing environment and ensuring the designs meet requirements as specified.

1.2 Document Control

All approved levels are 1.01 and higher. The document is only available in PDF format.

1.3 Version Levels

Version	Date M/D/Y	Reason
1.0	07/30/2003	Not approved; see version 1.01 reasons
2.21	10/25/2007	APPROVED
2.30	04/25/2008	DRAFT

1.4 Document Change History

Document change history will be maintained for versions 1.x and greater.

Version	Date M/D/Y	Modified	Reason
1.01	08/13/2003	*	Changed "required" to "objective", section 3.4, Telco, High Altitude Added statement in Section 4 for "switches with fewer than 14 blade ports"
1.02	08/25/2003	*	Page 5, fig 2.2; Page 5, section 2.2; Page 6, section 2.3; Page 8, table 2.3; Page 9, section 3.2.1; Page 9, section 3.2.3; Page 18, table 5.4; Page 23, SR bit 3
1.16	08/16/2004	*	Major revision of version 1.02
2.01	09/16/2005	*	First draft high speed (4X) switch
2.03	10/18/2005	*	Update first draft of high speed switch
2.04	11/18/2005	*	Added PRBS statement, presence detect bits reserved. Corrected shock and vibration.
2.06	12/12/2005	*	Completed additions and updates
2.06a	01/17/2006	*	Advance Interim Version
2.06b	01/20/2006	*	Section 4.2.1, section 9.7, section 9.9 updated
2.07	06/08/2006	*	Added new airflow requirements for high speed switch modules Added NOM (Mexico - Safety) HSSM1-4 numbering changed to HSSM7-10, SEM/Bridge 1,2 changed to 5,6 Added 1X switch thermal model. Added pin names to 12-blade 4X

			chassis
2.07F	06/29/2006	*	Added surface finish requirements for 1X switch modules
2.07G	08/10/2006	*	Section 6.4, updated air flow diagram Section 9, updated 1x switch section and changed figure numbering and updated card drawings to 4x switch section. Section 9.2 & 9.6, updated statements to mechanical design kit.
2.20	09/13/2007	JEB	Section 4.3.4; Added SSH Section 4.3.6; Added VPD information Section 4.3.7; Added VLAN information, capability bits and several mgmt items Section 8.5.1, 8.5.3, 8.5.4; Added clarifications on register bits Section 8.6; fixed current MM support for port compatibility checking
2.20	9/13/2007	DH	Section 1.6; new Section 6.4.1; Update air impedance equation Section 7.1; Modified 1xSM connector table Section 7.2; Modified 4xSM connector table Section 9.5; Include the Double-High 4x Switch Modules for both the FFA and FFB Section 9; added Figure 9.7 & 9.9, renumbered previous figures 9-7 thru 9-20, Updated Figures 9-10 & 9-11 of card outlines
2.21	10/25/2007	JEB	Updated to version 2.21 Section 1.6; incorrect text Section 8.1.1, 8.3.2; changed EEPROM size to 8KB
2.30	04/25/2008	JEB	Added Section 13, Protect Node and Stacking Mode Architecture
2.30	05/02/2008	JEB	Corrected Figure 2-2, 2-4 and 7-9 for SM, HSSM and BM numbering
2.30	05/07/08	JEB	Changed section 13 (PRM/STM) to use term ‘member’ versus ‘member’ Updated table 3.3 reference info for 2.06 spec bay numbering. Added section 9.13 and Figure 9-21.
2.30a	08/20/2008	MDH	Update to Section 6.1 to change single 4XSM maximum power from 60 to 75 watts. Updated Section 6.4.1 to include an Upper Bound formula for air impedance of a 1XSM. Updates to Avg. Air Temp values for Table 6-2. Added mechanical information for Bridge Module (Section 9.13 thru 9.16). Reordered Section 9.13 to 9.17.
2.40	09/19/2008	PKP	Updated Table 1-1; Updated; confirmed changes to table 6.2; Added in currently numbered section 7.2 with bridge connector information
2.41	02/04/2009	HA	Updated switch temperature inlet to 56 deg C on Table 6-1-1X. Updated Section 2, Section 8.1, Figure 8-1, Table 8-2, Table 8-3, Table 8-5, Section 8.3.2 and Section 9.13. Changed all references of "Bay ID" to "Switch Bay ID". Updated Table of Contents.
2.42	06/01/2009	DAG	Updated connector part numbers in Tables 7-1, 7-6. Updated text in Sections 9.2, 9.3, 9.6, 9.7 and 10.2. Removed Section 9.9. Expanded Section 10.4.
2.43	12/01/2009	PLC	Updated table 7-11
2.44	04/21/2010	HA	Updated section 6-1.
2.45	05/1202010	HA	Updated BOSSC Web site link.

1.5 Change Frequency

This document will be updated to reflect changes and updates that are approved by the joint Intel/IBM Collaboration Architecture Review Board.

1.6 VPD Base Field for ‘Base Specification Major and Minor Version’

Below is the information that must be initialized into the components Vital Product Data (VPD) field described as ‘*Base Specification Major and Minor Version*’. For a Switch Module component this is

the equivalent of the information as specified in the ‘Document Version’ on the title page of this specification. See ‘Base Specification for VPD’ for additional information.

Table 1-1 Component VPD Field for 'Base Specification Major and Minor Version'

VPD Field Location	Hex Value in VPD	Displayed ASCII value on MM Management Interfaces
Block1 (Dynamic Block Controller Area) byte offset: 01B2h	02 0d	‘2.45’

2 Switch Module Overview

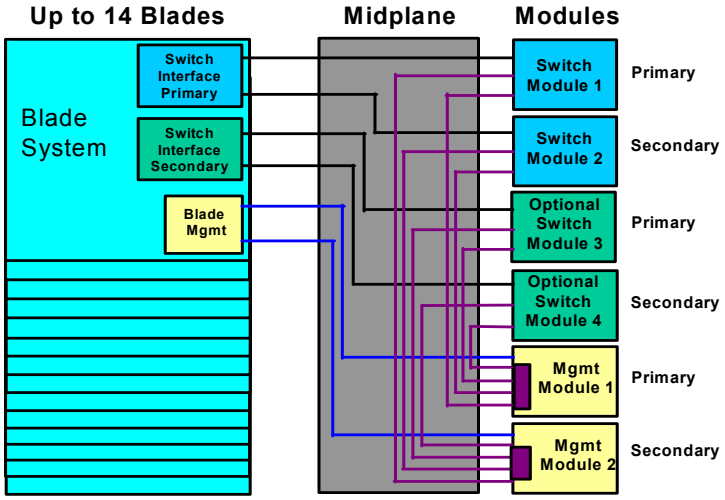
Figure 2-1 shows the 1X chassis architecture, which is capable of supporting either eight or fourteen processor blades, four 1X Switch Modules (1XSM), and two Management Modules (MM). The 4X chassis architecture is shown in Figure 2-2, Figure 2-3 and Figure 2-4, and is capable of supporting either twelve or fourteen processor blades, four 1X Switch Modules (1XSM), four 4X Switch Modules (4XSM), four 4X Bridge Module (4XBM), and two Management Modules (MM). Both 1X and 4X Switch Modules provide networking and/or Switch functions to the processor blades. Each processor blade is capable of accessing all Switch Modules via point-to-point links across the mid-plane. The 1X switches provide a four wire interface, allowing one transmit and one receive differential pair per link. The 4X switches provide a sixteen wire interface, allowing up to four transmit and four receive differential pairs per link.

The switches are generally used in pairs to allow the customer to configure for connection redundancy and/or additional bandwidth. Each pair of 4XSM's provides connectivity to an optional pair of 4XSEM's with a sixteen-wire interface for each link. The 4XSM is also referred to as the High Speed Switch Module (HSSM) in this document.

In the 14-blade 4X chassis, the 1X Switch Modules 3 and 4 and Bridge Modules 3 and 4 are defined for use in common bay positions and are mutually exclusive. Two Bridge Modules have dedicated bays. Thus, a maximum of four 1X Switch Modules and two Bridge Modules or two 1X Switch Modules and four Bridge Modules can be populated in the 14-blade 4X chassis. In the 12-blade 4X chassis, all of the Switch Modules and Bridge Modules share bays. There are no dedicated Bridge Module bays in the 12-blade 4X chassis.

This document provides the interface requirements for integrating a Switch Module or a Bridge Module into a BladeServer Chassis. Details regarding SM power, connectors, mechanical and management interfaces are provided. This document will cover both 1X and 4X Switch Modules. Most of the specification will pertain to both SM's. Sections that pertain to only one type of SM will be denoted with a 1X-only or 4X-only notation. This document also provides the technical details for the Bridge Module. The Bridge Module requirements that differ from a 1X Switch Module include; a shorter midplane connector as BladeServer connections are not required, an additional 54 pin connector for connectivity to the 4x Switch Modules, and a notch on the enclosure for proper chassis installation. Other sections of this document describing 1X Switch Module features pertain to the Bridge Module and are required functions. Additional requirements unique to specific SM or BM implementations are

provided in a Product Requirements Document



(PRD).

Figure 2-1 - Switch Connection Architecture for 1X Chassis (up to 14 blades)

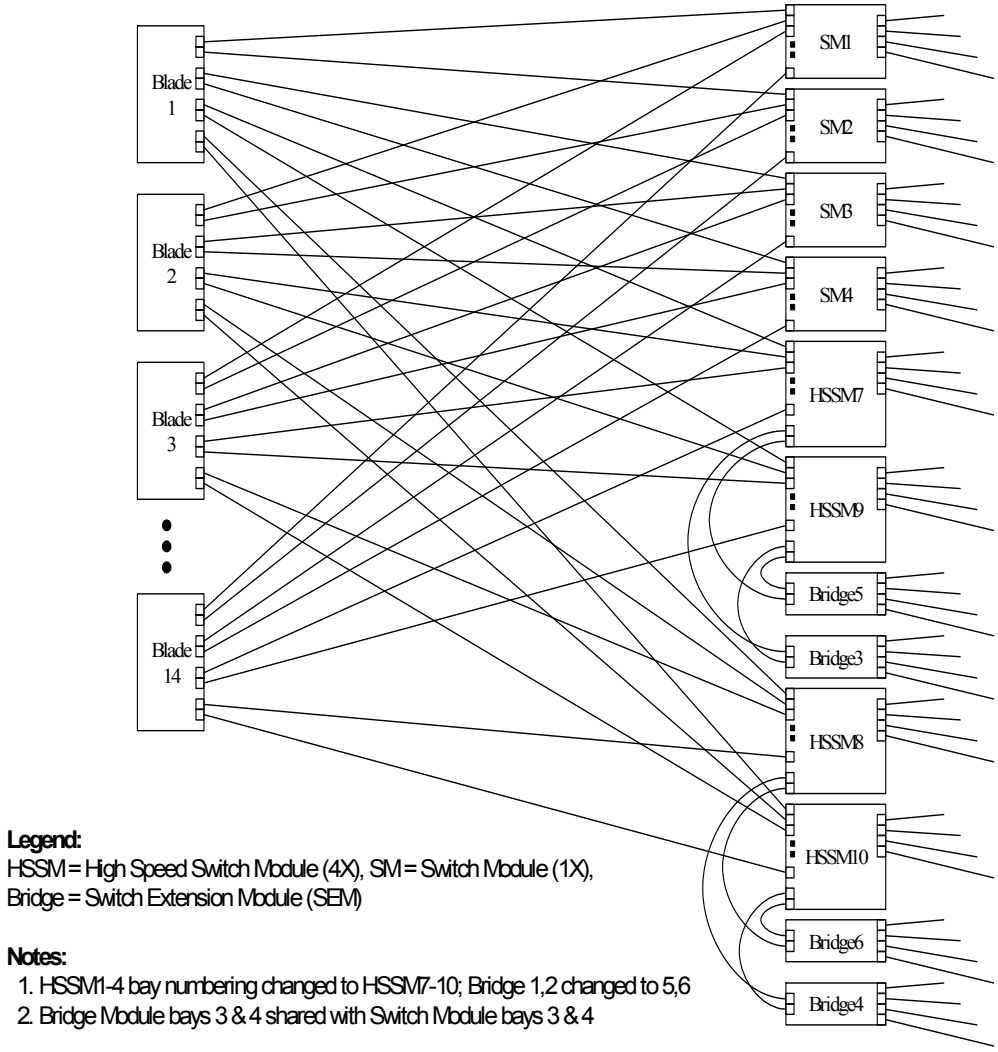


Figure 2-2 - HSSM to Blade Connection Architecture for 4X Chassis (14-blade)

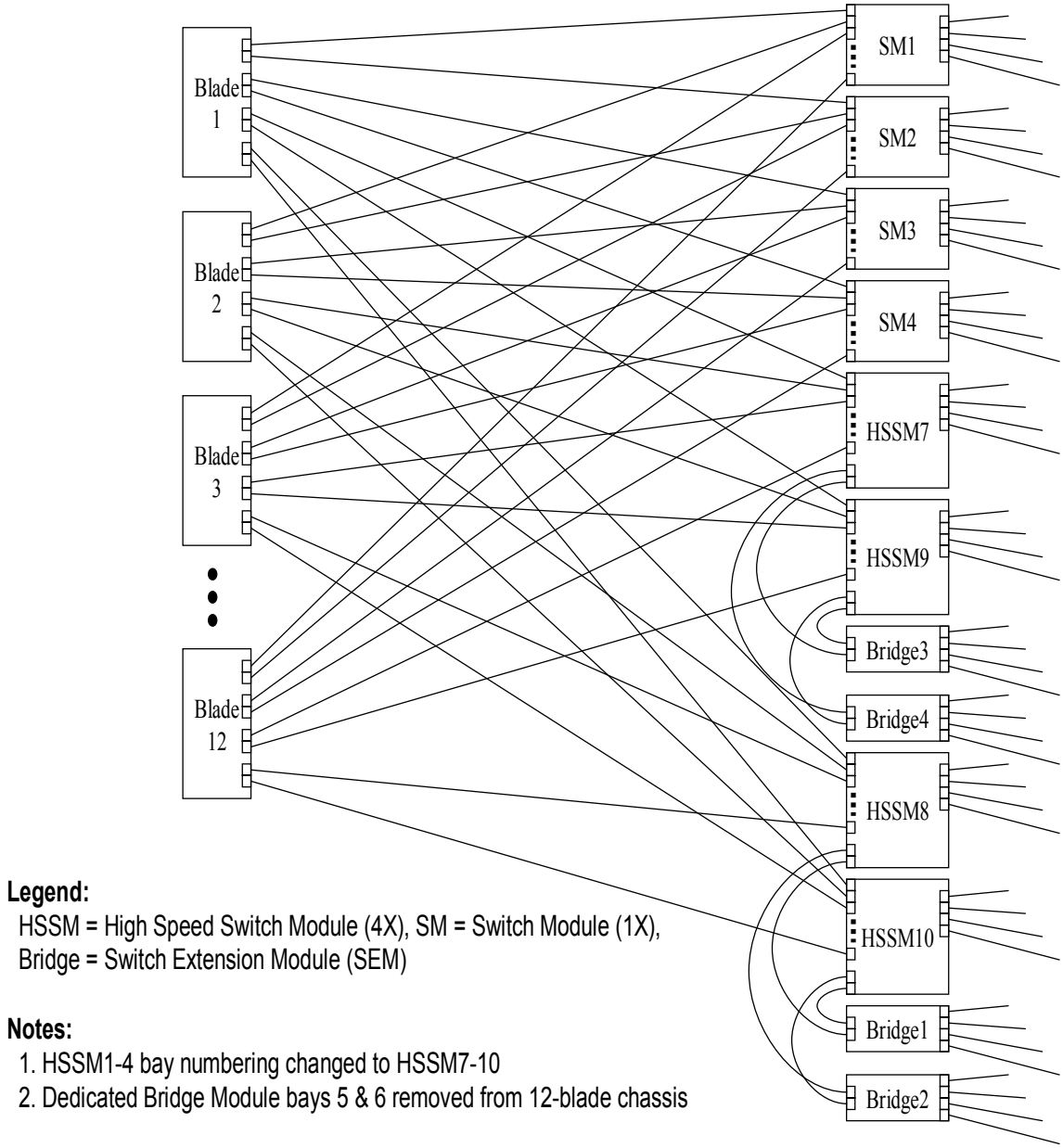
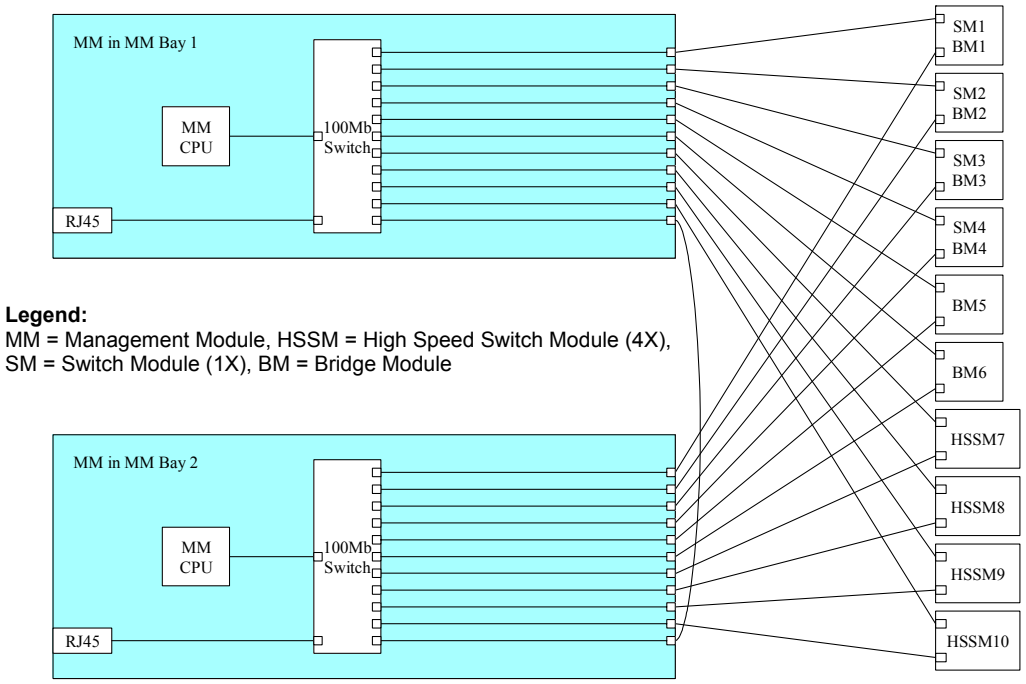


Figure 2-3 - HSSM to Blade Connection Architecture for 4X Chassis (12-blade)



Note 1: BM5 and BM6 are dedicated bridge bays in 14-blade 4X chassis only
Note 2: Shared SM/BM1 and SM/BM2 bays are in 12-blade 4X chassis only

Figure 2-4 - HSSM to MM Connection Architecture for 4X Chassis

The Management Module(s) provides a single point of control for the BladeServer Chassis. An I^2C interface is required between the Management Module and Switch Modules. The I^2C interface is utilized to collect information, perform initial configuration as well as provide monitoring and control of the Switch Modules. Each Management Module also has a100 Mbps Ethernet interface to each of the SMs / HSSMs. This Ethernet interface can be used, once IP traffic has been established between the management module and Switch Module, for internal IP traffic to configure and monitor the Switches. The Ethernet link between the MM and the SM / HSSM is a 100 Mb Ethernet link (without magnetics).

As an example, a 1X Ethernet Switch Module for the BladeServer (Figure 2-5) has four external Ethernet links, fourteen internal point-to-point 1Gbps links to the processor blades, two point-to-point internal 100 Mbps links to the Management Modules and an I^2C interface to each of the two Management Modules (for I^2C VPD and register access). Other signals include power, Switch Bay ID, and presence indicator. An example for a High Speed Ethernet Switch Module is shown in Figure 2-6, where the fourteen internal processor blade connections through the midplane are made up of four 4-wire SerDes interfaces, which can provide an aggregated speed of 10Gbps to each processor blade.

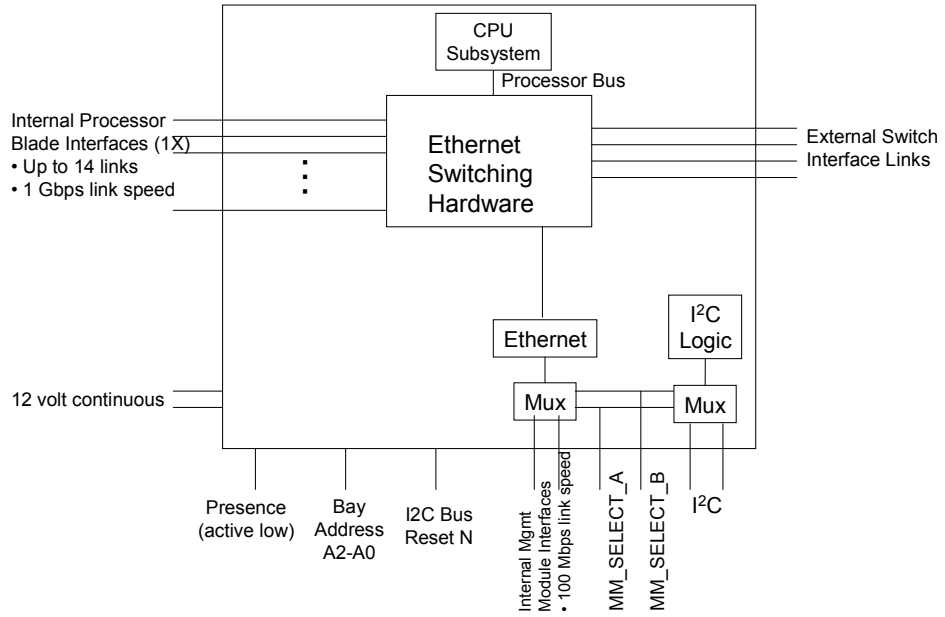


Figure 2-5 - 1X Ethernet Switch Design Example

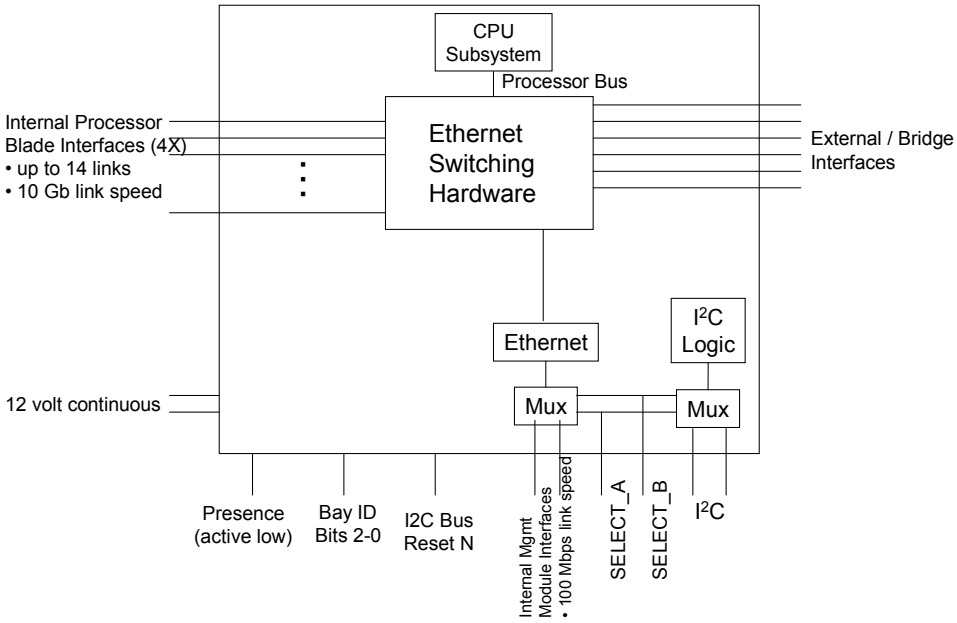


Figure 2-6 - 4X Ethernet Switch Design Example

3 Chassis Configurations

As described above, the BladeServer 4X Chassis architecture can support up to four 1X Switch Modules, four 4X Switch Modules, and four 4X Bridge Modules. The bays are numbered from a front view perspective, but are shown from a rear view perspective.

Figure 3-1 shows the switch locations in the 1X chassis. Figure 3-2 and Figure 3-3 show the 14-blade and 12-blade 4X chassis, respectively. In order to determine its bay, the SM or SEM must read the Switch Bay ID from the mid-plane connector. The Switch Bay ID value is mapped to the appropriate Switch bay number as shown in Tables Table 3-1, Table 3-2, and Table 3-3. In addition, the Switch Bay ID is mapped to the least significant three bits of the default IP address recorded in the VPD to ensure a unique IP address is assigned to each SM.

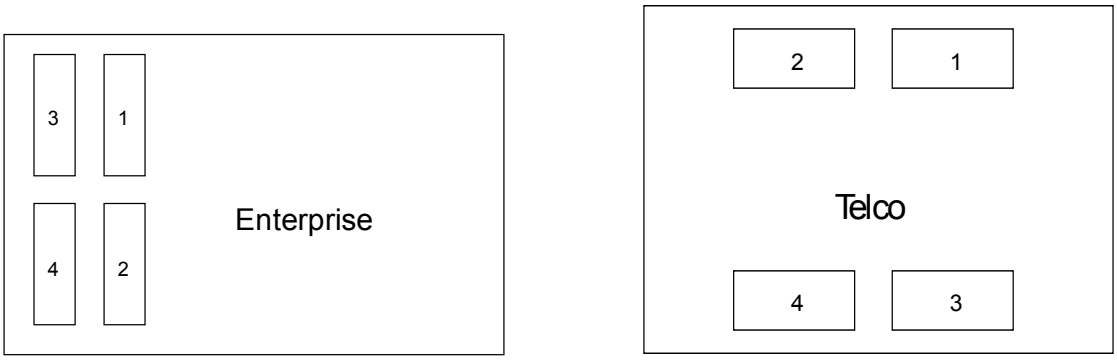


Figure 3-1 - 1X Chassis Bay Numbering, Enterprise shown on left, Telco right (Rear View Perspective)

	Switch Bay ID Pin		
Switch Bay	**F18**	**E18**	**D18**
Bay 1	0	0	1
Bay 2	0	1	0
Bay 3	1	0	0
Bay 4	1	1	1

Table 3-1 1X SM Switch Bay Identification

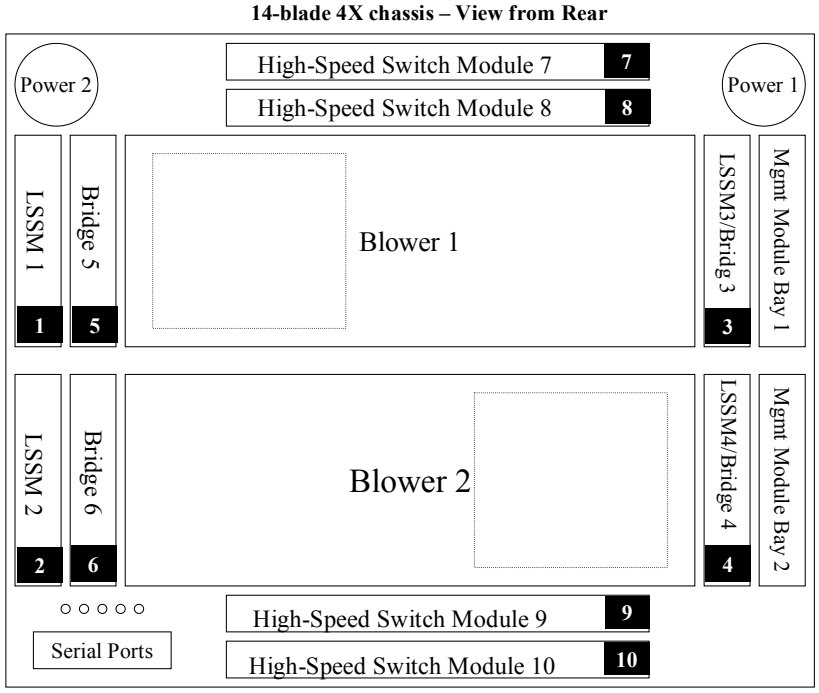


Figure 3-2- 4X Chassis Bay Numbering (14 blade), rear view

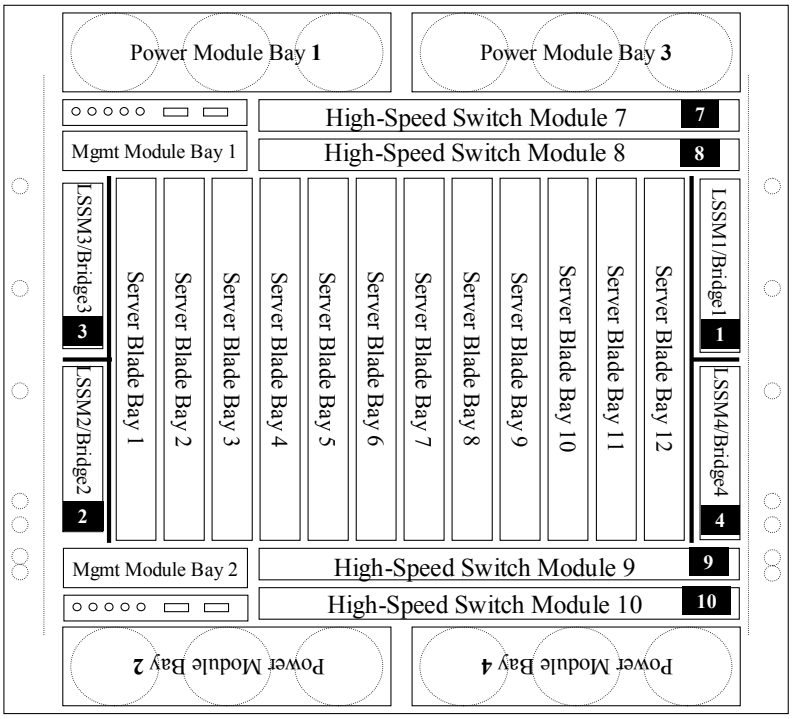


Figure 3-3 - 4X Chassis Bay Numbering (12 blade), front view

Switch or Bridge Bay	Switch Bay ID Pin		
	F18	E18	D18
Bay 1	0	0	1
Bay 2	0	1	0
Bay 3	1	0	0
Bay 4	1	1	1
Bay 5	1	0	1
Bay 6	1	1	0

Table 3-2 4X SM Switch Bay IDentification

Switch Module Bay	HSSM Number (Rev 2.06 or earlier)	HSSM Number (Rev 2.07 and later)	Switch Bay ID D24 B24 A24
7	1	7	000
8	3	8	010
9	2	9	001
10	4	10	011

Table 3-3 4X Chassis HSSM Switch Bay IDentification

4 Interface Definitions

The SM has four types of interfaces to connect to internal (within Chassis) or external devices. These include external interfaces (Ethernet, Fibre Channel, InfiniBand, etc.), internal interfaces (Ethernet, Fibre Channel, InfiniBand, etc.), internal I^2C interfaces and internal Ethernet interfaces to the Management Module.

4.1 External Switch Interface(s)

To provide cost, connectivity, and performance trade-offs, multiple versions of external links may be provided. External interface options may include:

- Ethernet (copper or fiber)
- Fibre Channel
- InfiniBand
- Wide Area Network (WAN) access

4.2 Internal Switch Interfaces

One of the motivations for physically integrating Switch Modules into the BladeServer Chassis is to minimize the cables typically required to connect server systems. This is accomplished with internal network connections across the BladeServer Chassis mid-plane. These high-speed interfaces are point-to-point links from the Switches to the Management Modules and processor blades as described below.

4.2.1 Processor Blade Interfaces

Each processor blade bay has four 1X and four 4X interfaces with one interface to each of the Switch Module bays. Interface circuitry on the blade must be designed for the specific Switch interface in the respective SM bay. Switches must be designed with the capability to support logical to physical blade port mappings as a function of the chassis type (enumeration of the internal blade ports in not fixed across chassis types). The following SERDES switch fabric interfaces are supported:

- Gigabit Ethernet – 1.25Gb/s
- 10 Gigabit Ethernet – 4x 3.125Gb/s
- Fibre Channel – 2.125 Gb/s
- Fibre Channel – 4.25 Gb/s
- Infiniband – 2.5Gb/s
- Infiniband – 4x 2.5Gb/sec

Reference the *Blade Server Base Specification and Design Guide for SERDES High Speed Electrical Signaling* for detailed design requirements.

For Ethernet switches, when an internal processor blade port is disabled (via SW control or HW failure), the SM will transmit a pseudo random bit stream (PRBS) for 3ms prior to disabling the transmitter. The purpose of this action is to actively cause the processor blade NIC to recognize the link down condition to guard against the potential that the blade NIC receiver may have increased susceptibility to cross-talk once the switch transmitter is turned off.

4.2.2 Management Module Interfaces

There are two Ethernet interfaces on each SM connected through the midplane to the two Management Modules (see Figure 2-1 and Figure 2-4). These interfaces can be used to initialize, configure and monitor the Switches.

The switch to MM links are 100 Mbps full-duplex, fixed speed (not auto-negotiated) Ethernet on a four-wire link that does not require magnetics (i.e., "transformerless"). This implementation saves space by reducing the number of physical layer components.

4.2.2.1 Switch Support for Dual Management Modules

In order to eliminate single points of failure within the Chassis, the option for having dual Management Modules exists. Select circuitry is required on the SM / HSSM to connect the appropriate master Management Module to the I^2C bus and to the Ethernet Management port. The MM_SELECT_A[1] and MM_SELECT_B[1] signals shall be used as shown in Table 8-1 to make that selection.

4.2.3 Internal I^2C Interfaces

An I^2C interface is used by the management Module(s) to internally provide control of the Switch Module and to collect system status and VPD information. The I^2C interface and operation are described in more detail later in this document.

Other interfaces that exist on the mid-plane include the presence indicator and Switch Bay ID. The presence indicator signal is active at a low logical state and is asserted when the Switch Module is connected to the BladeServer mid-plane. The Switch Bay ID is read-only by the Switch and designates the physical bay in which the Switch is inserted (see Table 3-1 and Table 3-3).

4.3 User Interface

4.3.1 Switch Management

The Switch Module must provide management functionality:

- Switch Initialization
- Switch Configuration
- Diagnostics (both power-on and concurrent)
- Status Reporting

The Switch Module software and firmware[2] (SW) will (unless otherwise noted) provide these management interfaces that can be used by external entities to enable/control the above functions:

- Simple Network Management Protocol (SNMP)/Management Information Base (MIB)
- Command Line Interface (CLI)
- Web Browser Management Interface

4.3.2 SNMP/MIB

The Switch Module must provide SNMP/MIB monitoring functionality contained within the Ethernet Control MIB-II (RFC1213-MIB)

It must also support SNMP versions 1 and 3.

Switch UUID (Universal Unique ID) information from the VPD (Vital Product Data) manufacturing fixed data block at address '009F'h shall be put into the MIB structure of the switch SNMP agent. Note, VPD data is defined in the *BladeServer Base Specification for VPD*.

[1] In the 4X chassis, control signals are named SELECT_A and SELECT _B

[2] Will use SW to refer to both Switch Module software and firmware in this section.

Specifically, the SNMP Engine ID object of the SNMP Management Frameworks defined in RFC 3411 is to be implemented as follows:

- First Bit = 1
- Octets 1-4 : set to the binary equivalent of the agent's SNMP management private enterprise number as assigned by the Internet Assigned Numbers Authority (IANA)
- Octet 5 = 177
- Octets 6-21 : set to the UUID value stored in the VPD fixed block manufacturing data area at address '009F'h

As an example, for an enterprise with an assigned IANA value of 696 and a VPD UUID of DCADBC89AFFA118DBD53824C6B588D67, the SNMP Engine ID would be set equal to '800002B8B1DCADBC89AFFA118DBD53824C6B588D67'.

Note, that the snmpEngineBoots, snmpEngineTime, and snmpEngineMaxMessageSize objects in the snmpEngineGroup can be set to zero.

4.3.3 SNMP Traps

The following minimum subset of Traps (see RFC 1215) must be supported:

- Cold Start
  This trap signifies that the Switch has been powered up and initialized such that software settings are reconfigured and hardware systems are rebooted. A cold start is different from a factory reset in that configuration settings saved to non-volatile RAM are used to reconfigure the switch.

- Warm Start (if applicable)
  This trap signifies that the switch is reinitializing itself such that the switch configuration is not altered.

- Link Up/ Link Down Traps
  These traps signify that a link has either been connected or disconnected. Both the internal MM Ethernet interface and the switch specific port interfaces should provide the Link Up/Link Down traps.

- Authentication Failure Trap
  This trap signifies that someone has tried to access the switch using an invalid SNMP community string. The Switch Module automatically stores the source IP address of the unauthorized user.

4.3.4 Text Sessions for Management

Switch Module requirements for CLI are:

- Support for multiple concurrent Telnet/SSH Sessions – required 4 sessions, preferred 8 sessions
- Support for SSH Version 2
- Default session time-out after inactivity for a period of 10 minutes (configurable by user)
- Must provide a scriptable interface

4.3.5 Serial Port

The Switch must provide some form of a standard serial interface connection either via cable or board connector. This interface is to provide development control/configuration of the switch module via the switch firmware's CLI interface.

4.3.6 Web Browser Management Interface

Base requirements are, but not limited to:

- Hardware status information
- Vital Product Data information that must at a minimum include, but not limited to: Switch type (for example - Ethernet, Fibre Channel, Infiniband), FRU Part Number, FRU Serial Number, Manufacturing Date, Hardware Revision, UUID, Firmware VPD(s) (including any CPLD's), MAC Address of Management Port(s), WWN or GUID when appropriate.
- POST status
- Port Diagnostics
- Switch Properties
- Network Configuration (IP address, SN, GW, Boot method)
- SNMP configuration (contact, location, communities)
- Provide switch firmware update function
- Provide default configuration reset feature
- Port information/status
- Support for SSL
- Support for standard web browser interfaces (see Browser Compatibility below)

Note: Specific implementation of these requirements is not specified.

4.3.6.1 Browser Compatibility

The Switch Module web browser interface must be compatible with following browsers/version:

- Microsoft Internet Explorer version 5.5 or later with latest Service Pack installed
- Netscape Navigator version 7.0 or later
- Mozilla version 1.3 or later
- If a Switch Module provides a Web Server Java Applet, it must be W3C Compliant and run with JRE 1.4 or later (e.g., Should be able to run with Mozilla and Konquerer, with an additional option for Opera)

4.3.7 Other Basic Functions

The following are some basic requirements that all Switch Modules must implement to allow for IP connectivity and provide a known default behavior:

1. Must support a default Administrator user profile with a userid/password combination of userid=USERID and password=PASSW0RD (note the zero in PASSW0RD)
   a. Various user account privileges should be provided (for example administrator, read-write, read-only)
2. Firmware revision information must be provided in the appropriate 'Code Level Version' field(s) of the Dynamic Block Controller Area of VPD.
3. A scriptable telnet and SSH CLI, a Web server with SSL support, SNMPv1 Agent, and SNMPv3 Agent
4. Authentication protocols, LDAP mandatory, RADIUS and TACACS optional

5. Management access via the following default ports:
    - Telnet - TCP/23
    - SSH – TCP/22
    - Web server HTTP – TCP/80
    - Web server HTTPS – TCP/443
    - SNMPv1/v3 agents – UDP/161
    - SNMPv1/v3 traps – UDP/162
    - FTP, FTP-Data – TCP/20,21
    - TFTP – UDP/69
6. FTP and/or TFTP support for firmware upgrades, the ability to perform a get/put of a switch configuration file, the ability to perform a get/put of 'First Failure Data Capture' (FFDC) data file.
7. Ability to detect firmware/hardware hangs and provides the support to perform a get/put of a 'crash-failure dump' file (this may be part of FFDC) to a FTP and/or TFTP server.
8. Support of a primary and backup firmware image and a method to select either primary or backup image as the current operational firmware.
9. Support an event log with a date and timestamp that can be saved to a file with the ability to perform a get/put of the event log file to a FTP and/or TFTP server
10. NTP Client support (NTP V3)
11. Ability to configure and enable/disable various supported TCP and UDP ports supported by the switch module
12. Ability to send various levels of SM events and logs to an external 'SYSLOG' server.
13. IPv6 must be supported on the internal and external ports of an Ethernet Switch Module.
14. SNMPv1 Agent should be enabled by default with at least one community name of 'public' and should allow for a GET of the 'system group' information
15. Port mirroring requirements are:
    - Ability to perform port mirroring of MM ports to both internal and external ports.
    - ability to perform port mirroring of internal ports to external ports (this would also include traffic on the Management Module VLAN)
    - For security reasons, the ability to mirror the MM traffic is hidden and is available only to Development and service personnel
16. Management VLAN(s) requirements for Ethernet switches:
    a. A manufacturing default management 802.1q tagged VLAN of 4095 that includes the MM's internal management ports and the switch's internal ports that are connected to the BladeServers.
    b. An additional configurable management 802.1q tagged VLAN (in the standard VLAN range of 1 - 4094) that includes the MM's internal management ports and the switch's internal ports that are connected to the BladeServers.
    c. The above VLANs must not include the external ports of the Switch Module.
17. Detection of the chassis type via the 'Dynamic Block Systems Management Area' current 'History Log' entry (for additional information see the 'Base Specification for VPD'). This information will be utilized by the switch module to adjust any required behavior, and alter any user interface strings or number of BladeServer ports that is unique to a given chassis type (for example telco versus enterprise chassis).
18. The switch module must insure that the VPD 'Capability' bits in the 'Dynamic Block Controller Area' must be initialized to reflect the current operating firmware capabilities. The capability bits must be valid when the switch module has signaled a POST completion status indication to the MM for any reset or whenever a firmware

version level changes (for additional information see the ‘Base Specification for VPD’).

5 External User Indicators and Controls

5.1 System LED Indicators:

Indicator Name	Color	Usage
OK	Green	On solid when Switch Module is powered up and operating normally. See Table 5-2 for detailed definition.
Fault	Yellow	On solid indicates a fault has been detected somewhere on this Switch Module. If this indicator is on then the General Fault indicator of the Enclosure Front Panel should also be on. See Table 5-2 for detailed definition.

Table 5-1 - LED Indicator

5.2 Behavior of OK and Fault LEDs

	OK LED	Fault LED[3]	
Condition	**Green**	**Amber**	**Comments**
pre-POST	Off	Off	Power domain 2 not powered on[1]
POST start	first 1 - 3 sec on	first 1 - 3 sec on	Lamp Test
	Blink during diags / initialization[2] (500 msec on and 500 msec off)	Off	Progress indication
Post critical Fail	Off	On	switch not functional- replacement req'd
Post non-critical Fail	On	On	switch operational in degraded mode
POST complete OK	On	Off	fully operational
Extended POST start	Blink during diags / initialization (500 msec on and 500 msec off)	Off	Progress indication
Extended POST critical fail	Off	On	switch not functional- replacement req'd
Extended POST non-critical fail	On	On	switch operational in degraded mode
Operational non-critical fault	On	On	switch operational in degraded mode
Operational critical fault	Off	On	switch not functional- replacement req'd

Notes:

1. Power domain 2 is discussed in section 6.2.2.
   Power domain 2 will remain powered off if the Management Module detects a configuration mis-match or if the chassis power budget is exceeded.
2. The condition where the blink time exceeds 60 seconds due to a POST fault, shall be documented as a fault condition.
3. The Fault LED is set by a POST failure, a Status Register bit 3 transistion to a fault condition, or a thermal fault condition (bit 0 and/or bit 1) .
   For a critical fault, the Fault LED is cleared by POR/Reset. For thermal faults the Fault LED will reflect the state of the thermal fault (bit 0 and/or bit 1)
   For a non-critical fault, the Fault LED is cleared by the switch application read of the error log, user overt action which clears the Fault LED, or by the switch detecting the absence of the fault condition.

Additional note: Turn on the Fault LED when Power Domain 2 cannot be powered on due to a fault, or a fault is detected in Power Domain 1.

Table 5-2 - Behavior of OK and Fault LEDs

5.3 LED visibility requirement

Any Power, Activity, or Information indicator LEDs on I/O panel of SM must be visible at 8 feet. Indicators should be visible in a 120-degree cone (60 degrees off of perpendicular line from flat surface of I/O panel).

5.4 Other LED Indicators

For any switch unique LEDs such as link activity, link speed, etc, it is strongly preferred that Bi-Color LEDs not be used.

6 Power and Thermal

6.1 Power

The Switch Module's power interface circuitry (see Figure 6-1) must accept input from two separate (redundant) 12V power sources (+12.2V nominal, +/- 3%) on the mating midplane and provide circuitry for the following functions:

- Hot plugging of the Switch Module into an energized midplane
- Soft start to minimize impact on the 12V input when the Switch Module circuitry is powered on (see Figure 6-2). There must be no capacitors between the soft start circuitry and the backplane +12V sources that connect directly from the +12V to Gnd. The maximum inrush current during SM insertion should be 100 mA. While the input voltage is stabilizing after insertion, the current slew rate should be limited to 500 mA/ms. Soft start must be completed within 9 ms. After insertion in the low-power state, the maximum allowed current is 1.8 A (
- Figure 6-3 shows a graphical representation of these requirements).
- Auxiliary (continuous) voltage to onboard service processor or control circuitry (I^2C).
- OR'ing and isolation of the two input voltages allows continued power to the Module if one of the 12V power sources should fail. Fuses on each of the two 12V inputs ahead of the OR'ing diodes are required to protect the redundant power sources, as shown in Figure 6-2.
- Comparator which monitors the dual fuses at the redundant 12V inputs and provides a status bit in the I2C Extended Status Register (Bit 1) indicating state of fuses (a value of '0'b = fuses OK, '1'b = fuse fault), as shown in Figure 6-2. Any design implementing the fuse fault detection circuit must indicate this capability in the Vital Product Data.
- Current sensing and limiting so a circuit fault on the Switch Module will not pull the 12V power sources down. The implementation should isolate the fault from the 12V source and latch the card in an OFF state when detected. For a Power Domain 2 fault (see section below on "Fully Powered State), I^2C status register bits 3 and 4 shall be set.
- 240VA power limiting Fuse/FET protection implemented within the area specified by the mechanical drawings.

Once inserted into the Chassis, the Switch Module will be in either low power or fully powered state as described in following sections.

- 1X-only: In the fully powered state, a single 1XSM can use a maximum of 45 watts.
- 4X-only: In the fully powered state, a single 4XSM can use a maximum of 75 watts.
    - A double-high 4XSM can use the total available power of the two bays (150 watts). Due to design limitations of the connector used, if the double-high 4XSM exceeds 120 watts, power must be drawn from the power connectors in both bays.

6.2 Hot Plug Capabilities

The specified Switch Module power connector consists of long ground pins and short power pins to allow for the appropriate hot plug enabling of circuitry. Upon insertion, the Switch Module enters a Low Power state thus enabling the I^2C circuitry in Power Domain 1 (see section below on Low Power State). The Switch will not enter the Full Power state until the Management Module turns on the power bit in the Control Register.

6.2.1 Low Power State

Once fully inserted into a Switch Module bay, the Switch is put into a low power state. The low power state requires at a minimum that all of the I^2C logic be operational. This includes the:

- I^2C Registers
- VPD EEPROM
- Switch Module fault LED
- Slot Address
- Presence bit

The circuitry powered in this state is referred to as "Power Domain 1". The maximum power in this state is 1.8A x 12V = 21.6W.

6.2.2 Fully Powered State

The fully powered state is entered after the Management Module powers on the Switch Module by setting bit 0 of the I^2C Control Register to a "1" value. All additional circuitry in the Switch that is powered on during this state is referred to as "Power Domain 2".

6.2.3 Over Current Protection

Over current protection must be provided for both Power Domains 1 and 2. Power Domain 1 must report the over current condition, Status Register bit 4, via the Power Domain's I^2C interface.

- 1X-only Maximum over current is 6 amps
- 4X-only Maximum over current is 7.5 amps

6.2.4 Over Temperature Protection

A SM should not run when the temperature of the SM exceeds the SM's Shutdown temperature. Over temperature protection must be provided for by the SM and when the critical threshold is reached, then Power Domain 2 is turned off without assistance from the MM.

For further details see Section 8.6.4 Switch Module Overtemp.

6.3 Reset

There are several events that will result in a reset of the Switch Module. These are:

- Power-on cycle
- Hot-plug insertion
- I^2C Control Register Bit 0 (see I^2C Control Register Definition for operation of this Bit 0 reset)
- Actuation of the Switch Module's reset button (optional)

The following Reset Domains/States are defined:

- A Switch Module reset via the Control Register on the I^2C bus should reset the Power Domain 2 circuitry only.
- All circuitry should come up in its default state as part of power on, however, configuration parameters, as specified earlier, should remain unchanged.
- With the exception of power domain 1, a reset should have the same affect as a power on cycle. That is, the I^2C circuitry should not be reset.
- I^2C_RESET_N (see Table 7-5) resets the I^2C circuitry only.

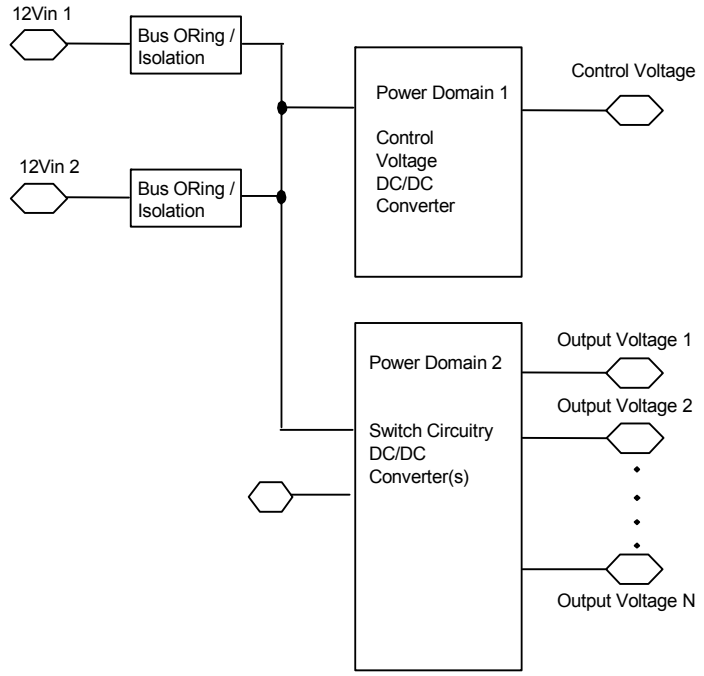


Figure 6-1- Switch Module Power Circuitry

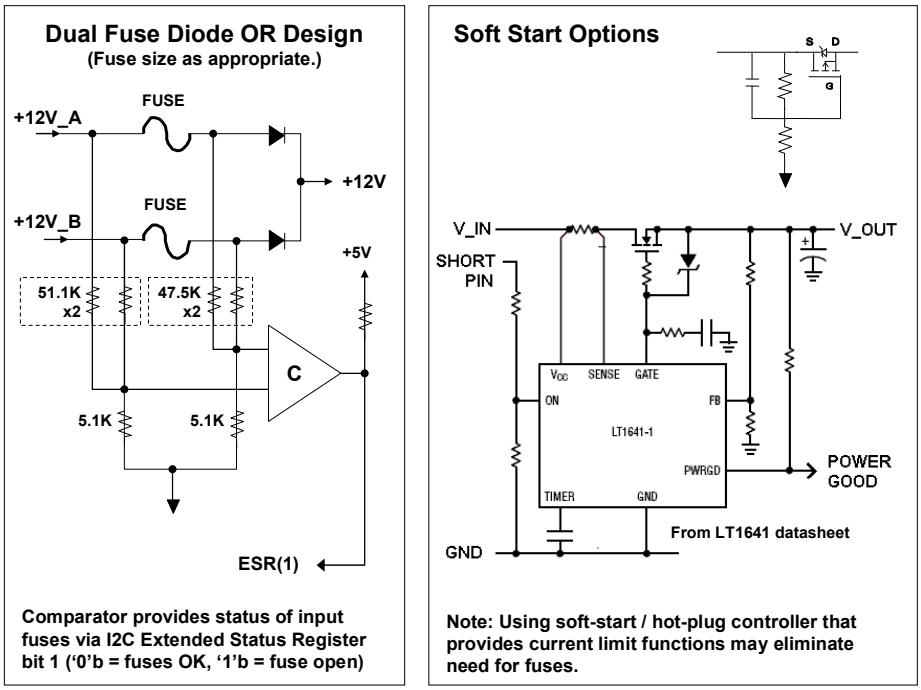
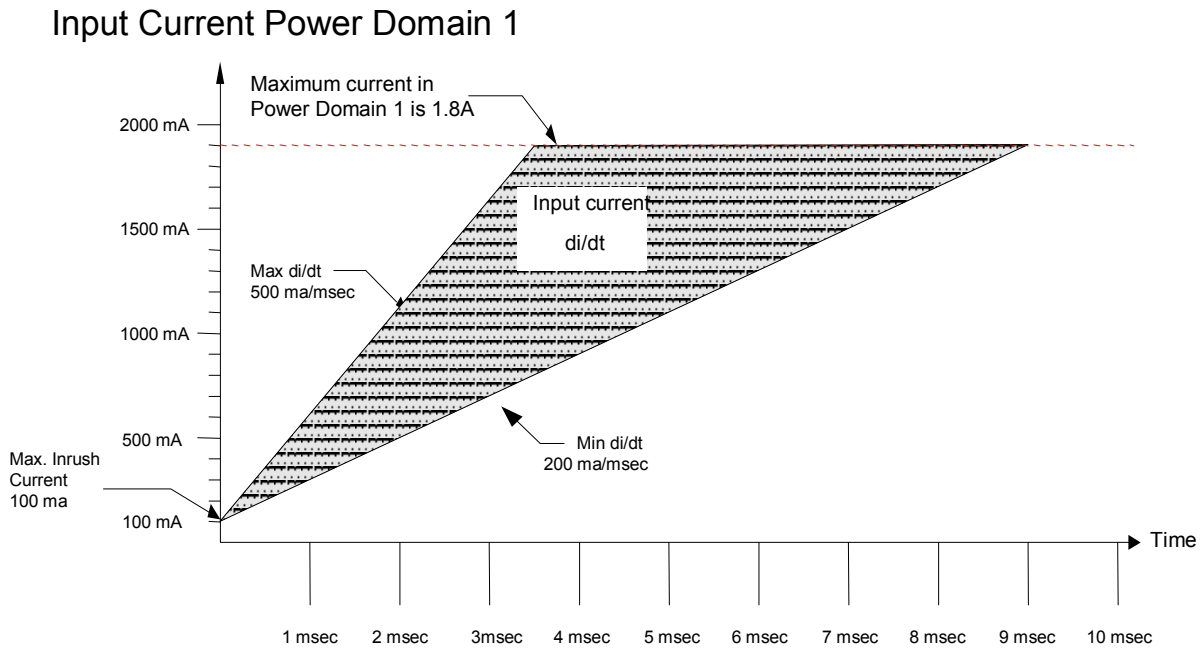


Figure 6-2 - 12V Power Interface Circuitry Reference Design



Note: Not all designs consume the maximum current of 1.88 Amps. For designs consuming less, the maximum power-on time can be determined by drawing a horizontal line at the current consumed in power domain. For example, for a power domain 1 current draw of 600 ma, the minimum power up time is 1 msec and the maximum power up time is approximately 2.5 msec. A similar diagram can be applied to powering on power domain 2. This is design dependent. The designer must extrapolate the input current di/dt for that design up to a maximum current draw of 3.75 Amps for a 1X SM and 5.0 Amps for a 4X SM.

Figure 6-3 - Inrush current

6.4 Thermal/Environmental Requirements

6.4.1 1X Switch

	Enterprise	Telco
Air flow	150-400 LFM	150-400 LFM
Maximum inlet air temperature Low altitude	56 deg C required altitude: 0m to 914m 8-80% RH	55 deg C required altitude: -60m to 1800m 5-85% RH
Maximum inlet air temperature High altitude	56 deg C Altitude 914-2133m	55 deg C objective altitude: 1800-4000m
Maximum allowed temperature rise due to Switch	20 deg C	20 deg C
Minimum inlet air temperature	10 deg C	-5 deg C

Table 6-1 - 1X Switch Operational Environment

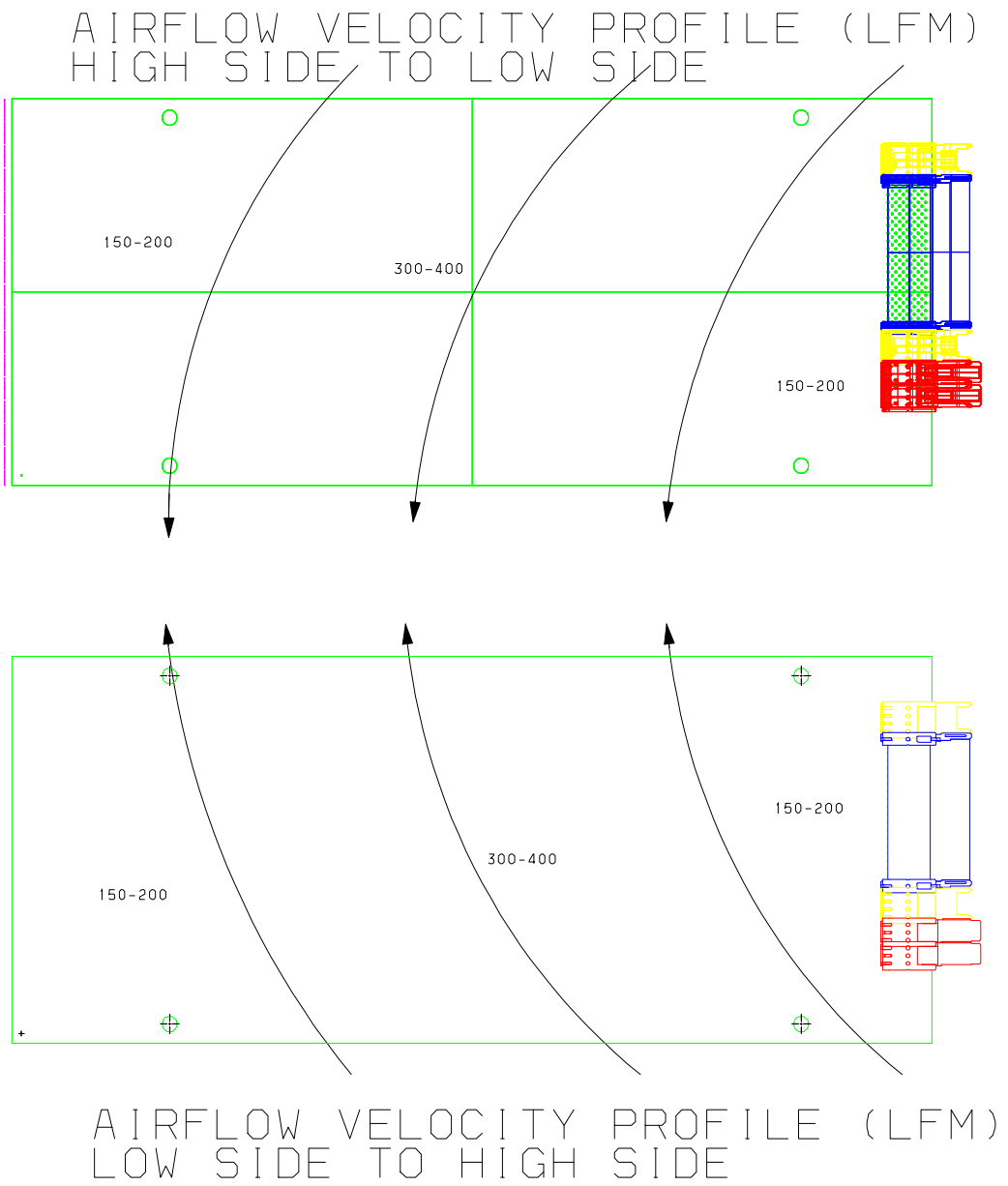


Figure 6-4 - Airflow Velocity Profile

Components should be placed so as to ensure the air impedance across the card is minimal. Components that dissipate the highest power should generally be placed at the center of the card both length and width wise, as this is where the greatest amount of airflow can be expected most reliably.

Air impedance of the Switch Module should be equal to or less than:

$$\text{Lower Bound: } \Delta p = 0.0004 * CFM^{1.976}$$
$$\text{Upper Bound: } \Delta p = 0.000897 * CFM^{1.94}$$

Pressure is expressed in units of Inches of H_2O

For CFD Thermal Modeling (i.e. Flotherm, Icepack, or other), create a model as shown in the figures below. This represents the worst case boundary conditions and will insure thermal compatibility in all BladeServer chassis. Model 5 CFM at 56^{O}C for switches intended exclusively for the Enterprise environment and 5 CFM at 55^{O}C if a switch is intended for both the Enterprise and Telecom environment. Note that flow may be from top to bottom or bottom to top. In both conditions, the air inlet is through a simulated 20 x 30 mm duct and the air exhaust is though the simulated 14.5 x 202 mm duct.

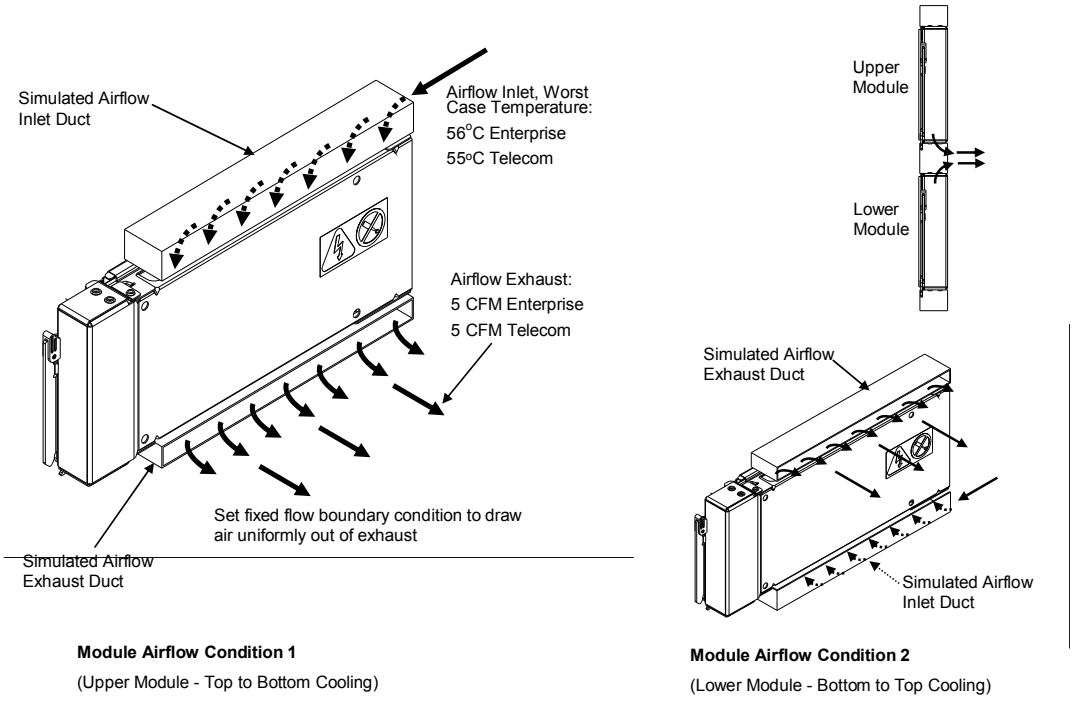


Figure 6-5 - Thermal Model Definition (Airflow)

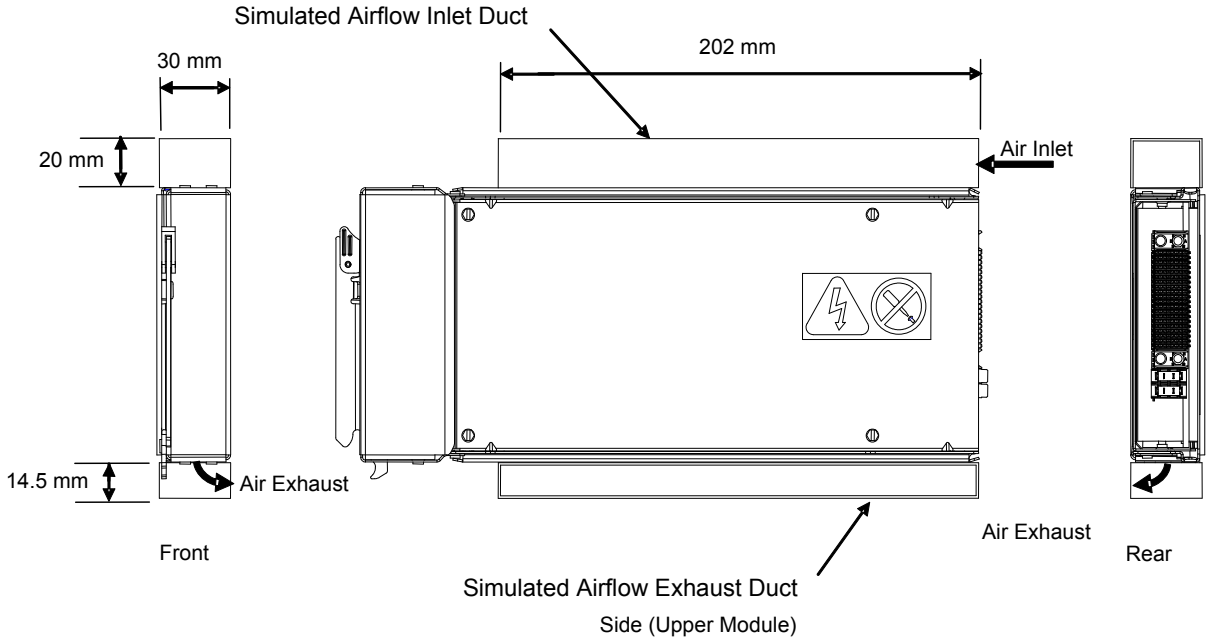


Figure 6-6 - Thermal Model Definition (Duct Size)

6.4.2 4X Switch (HSSM) Chassis and Airflow Overview

The budgeted thermal load for the High Speed Switch Module (HSSM) is set to a maximum of 75 watts. These switches are located in the rear of the 14-blade 4X chassis and in the front of the 12-blade 4X chassis. In the 14-blade 4X chassis, the HSSM modules receive their cooling from upstream components, which results in preheated airflow. The general airflow direction in the 14-blade 4X chassis is from the midplane connector side to the I/O panel face, whereas in the 12-blade 4X chassis, the HSSM modules receive no upstream preheat and the airflow direction is from the I/O panel face to the midplane connector side.

6.4.2.1 Cooling Requirements in the 14-blade 4X chassis

The figure below shows the expected cooling path for the HSSM's in the 14-blade 4X chassis. The table on the following page shows the expected airflow and inlet conditions for the various normal operating and component failure conditions. All conditions should be evaluated and modeled to predict worst case temperatures.

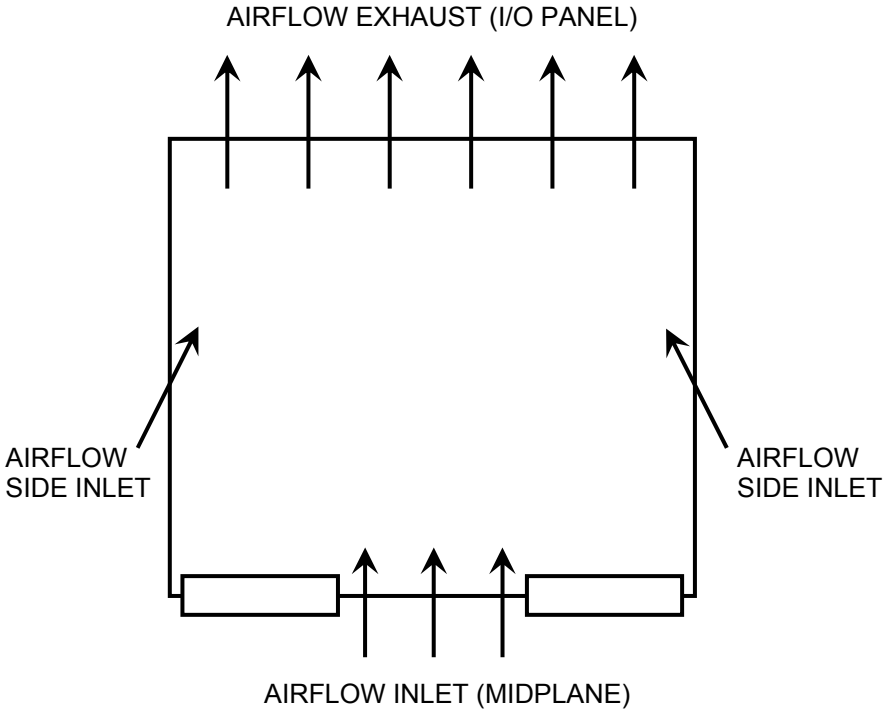


Figure 6-7 - HSSM Cooling in 14 Blade 4X Chassis

Environment @ 8-80% RH	Fan Speed	Avg. Air Temp. (^oC) Left/Right	Airflow Front Inlet (CFM)	Airflow Side Inlet (CFM) Left/Right	Airflow Total (CFM)
25 ^oC/2133m	Low Speed Normal	40.5	4.7	1.5/1.5	7.7
35 ^oC/914m	High Speed Normal	45.0	7.5	2.3/2.3	12.0
35 ^oC/914m	Upstream Component Fan Failure	45.0/48.0[1,3]	6.6	2.3/1.7	10.6
35 ^oC/914m	Component or Building Redundant Power Service Failure	45.0/60.0[2,3]	7.5	2.3/2.3	12.1
Note 1: Entry airflow temperature distribution is a result of a fan failure in an upstream cooling component. Higher inlet temperature is coupled to the lower side inlet airflow.					
Note 2: Maximum temperature unevenly distributed because of uneven power distribution on upstream cooling components.					
Note 3: For front inlet air, the temperature varies linearly from left to right (right to left)					

Table 6-2 - HSSM Operational Environment in 14 Blade 4X Chassis

The inlet air temperature and airflow rates shown above are for single high HSSM solutions. Both single high and double high HSSM solutions must comply with the impedance curve requirements (equations shown below). Double high solutions should assume (2X) the airflow for given pressure drop requirements at (1X) the flow. Accordingly, the expected net airflow for a double high HSSM, should be assumed to be (2X) of that stated in the flow table.

The governing equations for the switch impedance are:

$$\text{Lower Bound: } \Delta p = 5.13 \times 10^{-4} \times CFM^{1.95}$$

$$\text{Upper Bound: } \Delta p = 5.67 \times 10^{-4} \times CFM^{1.96}$$

Pressure is expressed in units of Inches of H_2O.

When designing to match the stated impedance requirements of the switch, it is imperative that these modifications occur on the I/O panel face plate only. The mechanical enclosure on the side and midplane connector end inlet openings must be left unchanged, as this is required to guarantee flow distribution for upstream chassis component cooling

In addition, any portion of the switch exit temperature is not to exceed 60 degrees C, based on UL touch temperature limits for metal, which may be used as a carrying point when a High Speed Switch Module is removed from the chassis.

6.4.2.2 Cooling Requirements in the 12-blade 4X chassis

HSSM bays are located in the front of the 12-blade 4X chassis. The resulting airflow is from front to rear (I/O panel face to midplane connector) and it receives fresh air. There is no upstream component cooling pre-heating effect.

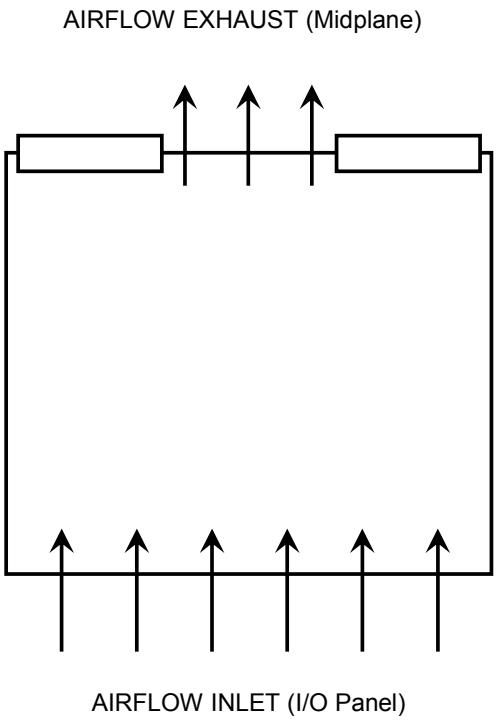


Figure 6-8 - HSSM Cooling in 12 Blade 4X Chassis

The table below shows the expected airflow and inlet conditions for the various normal operating and fan failure conditions.

Environment @ 5-85% RH	Fan Speed	Avg. Air Temp. (^{o}C)	Airflow Total (CFM)
25 ^{o}C/1800m	Low Speed Normal	25	5.6
40 ^{o}C/1800m	High Speed Normal	40	13.8
55 ^{o}C/1800m	High Speed (short term[1] environmental temp. excursion)	55	13.8
40 ^{o}C/1800m	Fan Failure	40	12.8

Table 6-3 - HSSM Operational Environment in 12 Blade 4X Chassis

[1] Per Telcordia GR-63-CORE, "short-term" refers to a period of not more than 96 consecutive hours and a total of not more than 15 days in 1 year. This refers to a total of 360 hours in any given year, but, no more than 15 occurrences during that 1-year period.

6.4.3 Shipping and Storage Temperature, Humidity, and Altitude

	Enterprise	Telecom (NEBS/ETSI)
Shipping temperature	-40C to +60C	-40C to +70C
Shipping relative humidity	5% to 100%	Uncontrolled
Storage Temperature	+1C to +60C	-40C to +70C
Storage relative humidity	5% to 80%	Uncontrolled
Storage altitude	0 to 2133 m (6998 ft)	Unspecified

Table 6-4 – Shipping and Storage Temperature, Humidity, and Altitude

6.4.4 Component Temperature Reporting

In order to enable a utility such as IBM Director to gather temperatures throughout the BladeServer chassis it is necessary that each pluggable component provide adequate temperature sensing capability. Visibility of the actual internal temperatures and the general location of the sensor associated with each temperature sensor is required for chassis-level analysis.

This architecture specifies the addition of up to two temperature sensors per BladeServer component. Both temperature sensors must provide temperature readings accurate to within +/- 1° C over the entire operating range. Typically, inlet and exhaust temperatures range from -5°C to 65°C and heatsink or ASIC temperatures range from 10°C to 125°C.

All temperature devices and component designs must report temperature values that are repeatable. That is, even if the sensor itself is reporting +/- 1° then the component must report +/- 1° across the entire range of temperatures reported by that component.

Each BladeServer module must report its exhaust temperature. A 2nd temperature sensor may optionally be placed at either the ambient, exhaust or another location deemed prudent by the switch module provider.

It is understood that a variety of different temperature sensing technologies exist and that their placement on the board and within a chip package (e.g., as part of the silicon, within a heat sink, in downstream air flow, etc) greatly influences the temperature readings that the sensor produces. Here, it is assumed that the consumers of all temperature readings will be familiar with the specifics of sensor placement and technology being used for each component.

The following guidelines are provided to give direction to component designers, which will help maximize the usefulness of the temperature sensor data when the temperature readings are used to perform chassis-level thermal analysis.

- Sensors should be embedded within critical components. Designs should strive to place temperature sensors in the ASIC itself. If this cannot be achieved then a sensor should be located on the heat sink of the ASIC. Sensors should not be placed near critical components, with the intent of correlating to actual chip temperatures, as the accuracy and precision of this solution does not produce meaningful information. It is strongly recommended that Blade Server components use ASICs that provide an on-chip temperature measurement.

- When adding a sensor that is not located in an ASIC or heat sink, the n the sensor should be located such that it is thermally neutral to adjacent components and is indicative of the average temperature of that area.
  - Consistent with the above, an exhaust port sensor should be located at the hottest point within the exhaust port.
- Aggregate inlet air temperature sensing is optional.
- For 1X Switch Modules, consideration must be given to where the direction of airflow may depend upon where they are placed in the BladeServer chassis. For example, a temperature sensor located near the top of a switch will measure the air inlet temperature to the switch when the switch is placed in a top bay, however the same sensor will measure the air inlet temperature plus the temperature rise across the Switch Modules (i.e., essentially the outlet air temp) when the switch is placed in a bottom bay. Clearly, this data is representative of two very different scenarios. One way to deal with this situation may be to include 2 temperature sensors so that one is guaranteed to have visibility of the temperature rise of the module regardless of airflow direction. Another way may be to enable one of the 2 temperature sensors as a function of the top/bottom orientation of the I/O module. This will allow the 2nd sensor to be used in the inlet, ASIC or heatsink locations.

7 Mid-Plane Pin Assignment and Signal Description

For additional information of the SERDES high-speed signals, please see the *Blade Server Base Specification and Design Guide for SERDES High Speed Electrical Signaling.*

7.1 1X Switch Module

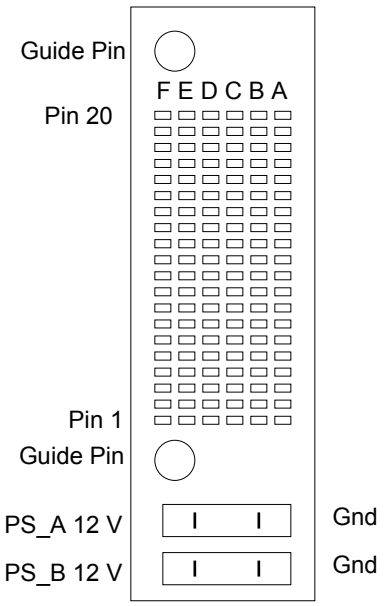
7.1.1 1X Switch Module Connector Description and Pin Assignment

The connector description and part numbers for the connector assembly that is applied to the 1X switch as well as the mating connectors that are present on the midplane are shown in the table below. The three mating connectors on the midplane are grouped together in order to plug with the connector assembly on the 1X switch module.

Table 7-1 - 1X Switch Module (1xSM) Connectors

Connector Description	Source A		Source B		Note
	Vendor	Part Number	Vendor	Part Number	
VHDM/Power Connector Assembly	Molex	74030-9972	Amphenol	AV600-00076	Part of 1xSM
Mating VHDM Connector on Midplane (1 of 2)	Molex	74074-9987	Amphenol	498-5010-022	Part of midplane
Mating VHDM Connector on Midplane (2 of 2)	Molex	74074-9976	Amphenol	498-5110-022	Part of midplane
Mating Power Connector on Midplane	Molex	74029-6998	Amphenol	437-6050-000	Part of midplane
Note: Refer to *BladeServer_Connectors_20090506.pdf* located on the Blade Open Spec Support Center website (http://www-03.ibm.com/systems/bladecenter/resources/openspecs.html) for most up to date connector list.					

The following tables describe the mid-plane power and signal connector pin assignments and signal information for the Switch Module connector. Switches implementing fewer than 14 blade ports should use the lower numbered TX/RX SERDES pairs.



View of the switch connector looking from the mid-plane to the back of the switch

Pin	A	B	C	D	E	F
21	-	Gnd	Gnd	-	12V_B	12V_B
22	-	Gnd	Gnd	-	12V_B	12V_B
23	-	Gnd	Gnd	-	12V_A	12V_A
24	-	Gnd	Gnd	-	12V_A	12V_A

Table 7-2 - Power Connector Pin Assignment

Pin	G	H	J	K	L
1	Gnd	Gnd	Gnd	Gnd	Gnd
2	Gnd	Gnd	Gnd	Gnd	Gnd
3	Gnd	Gnd	Gnd	Gnd	Gnd
4	Gnd	Gnd	Gnd	Gnd	Gnd
5	Gnd	Gnd	Gnd	Gnd	Gnd
6	Gnd	Gnd	Gnd	Gnd	Gnd
7	Gnd	Gnd	Gnd	Gnd	Gnd
8	Gnd	Gnd	Gnd	Gnd	Gnd
9	Gnd	Gnd	Gnd	Gnd	Gnd
10	Gnd	Gnd	Gnd	Gnd	Gnd
11	Gnd	Gnd	Gnd	Gnd	Gnd
12	Gnd	Gnd	Gnd	Gnd	Gnd
13	Gnd	Gnd	Gnd	Gnd	Gnd
14	Gnd	Gnd	Gnd	Gnd	Gnd
15	Gnd	Gnd	Gnd	Gnd	Gnd
16	Gnd	Gnd	Gnd	Gnd	Gnd
17	Gnd	Gnd	Gnd	Gnd	Gnd
18	Gnd	Gnd	Gnd	Gnd	Gnd
19	Gnd	Gnd	Gnd	Gnd	Gnd
20	Gnd	Gnd	Gnd	Gnd	Gnd

Table 7-3 - Signal Connector Shield Row Pin Assignment

Pin	A	B	C	D	E	F
20	NC	NC	NC	NC	Reserved	Reserved
19	PRES_BITz_N	Gnd	Gnd	Gnd	Gnd	NC
18	MM_SELECT_A	MM_SELECT_B	I^2C_RESET_N	ADDR0_x	ADDR1_x	ADDR2_x
17	SDA_SWA	SCL_SWA	SW_I^2C_INTA	SDA_SWB	SCL_SWB	SW_I^2C_INTB
16	Gnd	Mb_RxN_Bx	Mb_RxP_Bx	Gnd	Mb_TxN_Bx	Mb_TxP_Bx
15	Mb_RxN_Ax	Mb_RxP_Ax	Gnd	Mb_TxN_Ax	Mb_TxP_Ax	Gnd

14	Gnd	RxN1_x	RxP1_x	Gnd	TxN1_x	TxP1_x
13	RxN2_x	RxP2_x	Gnd	TxN2_x	TxP2_x	Gnd
12	Gnd	RxN3_x	RxP3_x	Gnd	TxN3_x	TxP3_x
11	RxN4_x	RxP4_x	Gnd	TxN4_x	TxP4_x	Gnd
10	Gnd	RxN5_x	RxP5_x	Gnd	TxN5_x	TxP5_x
9	RxN6_x	RxP6_x	Gnd	TxN6_x	TxP6_x	Gnd
8	Gnd	RxN7_x	RxP7_x	Gnd	TxN7_x	TxP7_x
7	RxN8_x	RxP8_x	Gnd	TxN8_x	TxP8_x	Gnd
6	Gnd	RxN13_x	RxP13_x	Gnd	TxN13_x	TxP13_x
5	RxN14_x	RxP14_x	Gnd	TxN14_x	TxP14_x	Gnd
4	Gnd	RxN11_x	RxP11_x	Gnd	TxN11_x	TxP11_x
3	RxN12_x	RxP12_x	Gnd	TxN12_x	TxP12_x	Gnd
2	Gnd	RxN9_x	RxP9_x	Gnd	TxN9_x	TxP9_x
1	RxN10_x	RxP10_x	Gnd	TxN10_x	TxP10_x	Gnd

Table 7-4 - Signal Connector Signal Row Pin Assignment

7.1.2 1X Switch Module Signal Descriptions

Signal	Signal Type	Impedance/Coupling	Description
RxNyy_x RxPyy_x	INPUT SerDes	100 ohms +/- 10% differential	Negative and positive receive signal of diff pair N from blade position 1 to 14 (yy = 1 .. 14). Refer to specific Switch/technology description for signal specification (ie. Gbit Ethernet, Fibre Channel, etc)
TxNyy_x TxPyy_x	OUTPUT SerDes	100 ohms +/- 10% differential	Negative and positive transmit signal of diff pair N from blade position 1 to 14 (yy = 1 .. 14). Refer to specific Switch/technology description for signal specification (ie. Gbit Ethernet, Fibre Channel, etc)
GND	NA	NA	Logic ground
I^2C_RESET_N	INPUT 5V pullup on midplane	55+/-10%	Shared line that when asserted by either Mgmt Module forces the Switch Module to clear its I^2C bus protocol unit (deasserts all SDA & SCL lines). Active Low signal. SWITCH MUST NOT USE PULLUP RESISTOR
SW_I^2C_INTA,B	OUTPUT 5V pullup on midplane	55+/-10%	Switch I^2C Interrupt Lines to management Modules A & B (refer to Switch Module I^2C Control Register definition). Switch Module provides open collector. Active low signals. SWITCH MUST NOT USE PULLUP RESISTOR
SCL_SWA,B	INPUT 5V pullup on midplane	55+/-10%	100 KHz I^2C Serial Clock Lines from management Modules A & B (signals are multiplexed, refer to I^2C section of this document) SWITCH MUST NOT USE PULLUP RESISTOR
SDA_SWA,B	BIDIRECTIONAL 5V pullup on midplane	55+/-10%	100 Khz I^2C Serial Data Lines from Management Modules A & B(signals are multiplexed, refer to I2C section of this document) SWITCH MUST NOT USE PULLUP RESISTOR
MM_SELECTA,B	INPUT 5V pullup on midplane	55+/-10%	I^2C Bus control lines from MM's A & B (see Table 5.1 for decode) SWITCH MUST NOT USE PULLUP RESISTOR
Mb_RxP_A,Bx Mb_RxN_A,Bx	INPUT "Transformerless" ENET	100 ohms +/- 10% (refer to Figure 4.1)	Negative and positive receive signal of MM A & B 100 Mbit ENET connection (refer to the text below this table)
Mb_TxP_A,Bx Mb_TxN_A,Bx	OUTPUT "Transformerless" ENET	100 ohms +/- 10% (refer to Figure 4.1)	Negative and positive transmit signal of MM A & B 100 Mbit ENET connection (refer to the text below this table)
NC	NA	NA	No Connect
PRES_BITz_N	OUTPUT (5V with 4.7K pullup on midplane)	NA	Presence pin. Switch Module grounds through 100 ohm resistor to indicate presence to Management Modules.
ADDR0,1,2_x	INPUT (Switch provides pullup)	NA	Three midplane inputs to the Switch Module to determine address. Refer to Table 2 for decode of signals (0,1,2=A0,A1,A2). SWITCH MUST PROVIDE VOLTAGE PULLUP (low signals are 100 ohm pulldown to ground on midplane, high signals are not connected on midplane).
Reserved	NA	NA	Do not wire - special function/future use.

Table 7-5 - Midplane Connector Signal Description

Processor blades which connect to switch I/O modules using the Ethernet interface should use ceramic capacitors to capacitively couple the transmit and receive signals of the Ethernet connection. Rather than isolation transformers as the means to connect the two interfaces together, ceramic chip capacitors are recommended for this connectivity because the impedance and signal characteristics can be closely controlled in the BladeServer environment. The midplane characteristics provide a substantial margin for error-free operation. The error-free margin includes connectors, vias, and all other associated non-ideal elements of the midplane technology.

7.1.3 1X / 4X SM Ethernet Connection to Management Module

Figure 7-1 shows how to connect the Ethernet signals in a typical backplane application to the management module. Both transmit and receive differential pairs are capacitively coupled at both ends. This provides DC protection in case there is a DC voltage difference between each end. Also each end is terminated with 100 ohms differential impedance.

The following rules apply to wiring the Ethernet signals.

1. Capacitors are 0.1 uf, 16V ceramic capacitors
2. Resistors are 49.9 ohms 1%, 1/10 watt
3. Place termination resistor as close as physically possible to the PHY chips
4. Termination resistors must be tied directly to a 3.3V VDD plane with trace lengths kept as short as possible. Note, on the Switch Module, biasing may be different based on PHY requirements.
5. Ensure the board differential impedance is kept as close to 100 ohms as possible
6. Multiple differential pairs have a spacing three times the line width spacing, e.g. if the differential pair traces are 6 mils apart, the differential pair spacing should be 18 mils
7. Port group spacing should be as large as possible

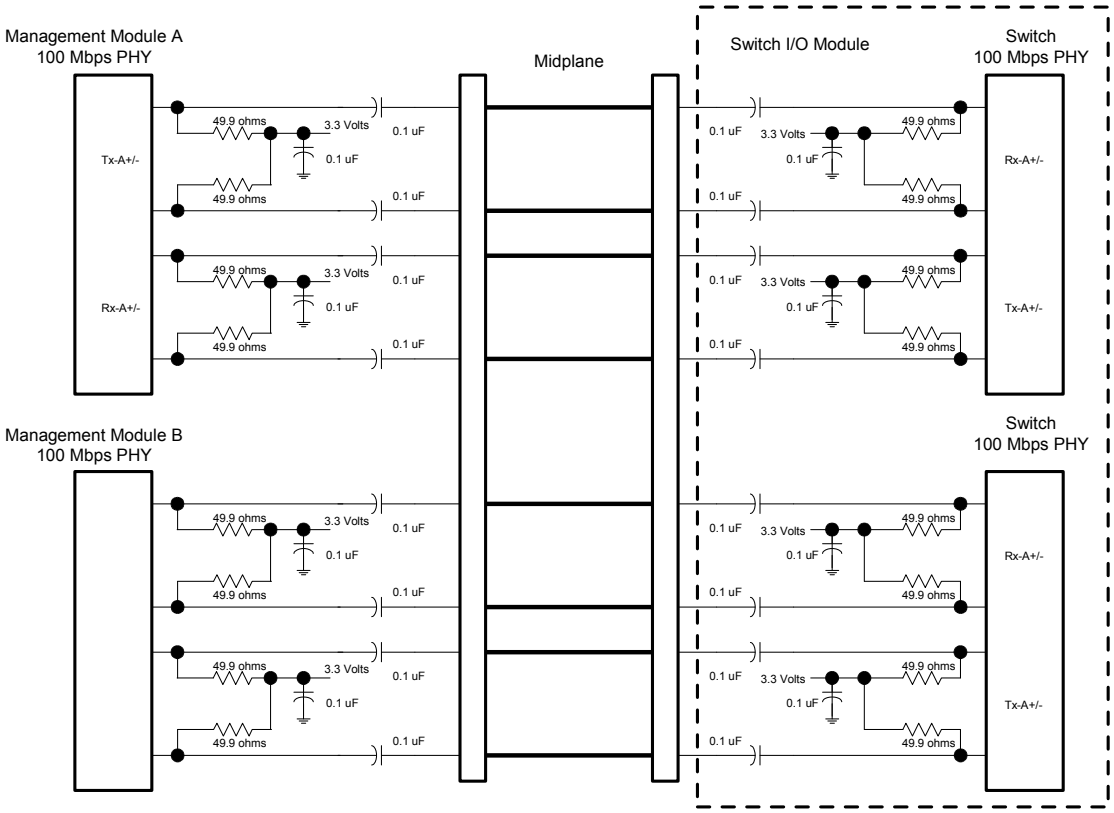


Figure 7-1 - Ethernet links to Management Module

Note: On the Switch Module, the 49.9 ohm / 3.3V biasing network may be replaced dependent upon the switch PHY requirements.

4X Switch Module

7.1.4 4X Switch Module Connector Description

The connectors used on the HSSM to interface with the mid-plane are GbX Enhanced high speed connectors capable of data rates above 6.25 Gbps. These are differential pair connectors with 2 sets of differential pair contacts per column of connector. The differential pairs are separated by a ground shield and the GbX Enhanced connector also makes use of additional shielding features within the connector housing. With 5.55 mm long pins on the midplane, the nominal pin wipe is 2.0 mm. There are 2 connector assemblies, a left and right, used on the switch. Each connector assembly has 40 columns of differential pairs for a total of 80 differential pairs per assembly. This totals 160 differential pairs for the HSSM to mid-plane interface. Part numbers are shown below in Table below for the assemblies.

Table 7-6 - 4X Switch Module (4xSM) and Midplane connectors

Connector Description	Source A		Source B		Note
	Vendor	Part Number	Vendor	Part Number	
GbX, 2 pair x 40 column, R/A, receptacle, guide block, right	Amphenol	AG822-00001	Molex	75874-0001	Part of 4xSM
GbX, 2 pair x 40 column, R/A, receptacle, guide block, left	Amphenol	AG822-00002	Molex	75874-0002	Part of 4xSM
Mating connector on Midplane for 4xSM – left guide pin	Molex	75834-3205	Amphenol	325-4120-025	Part of midplane
Mating connector on Midplane for 4xSM – end wall right	Molex	75834-5805	Amphenol	326-4320-025	Part of midplane
Mating connector on Midplane for 4xSM – end wall left	Molex	75834-3805	Amphenol	326-4420-025	Part of midplane
Mating connector on Midplane for 4xSM – right guide pin	Molex	75834-5205	Amphenol	325-4020-025	Part of midplane
Note: Refer to *BladeServer_Connectors_20090506.pdf* located on the Blade Open Spec Support Center website (http://www-03.ibm.com/systems/bladecenter/resources/openspecs.html) for most up to date connector list.					

The insertion force for the connector is shown in Table 7-7.

Table 7-7 - Calculated insertion force for 4xSM connectors

Maximum insertion force	94 N (21.1 lb_f)
Nominal insertion force	62 N (14 lb_f)
Minimum insertion force	46 N (10.5 lb_f)

Pin numbering and orientation for the HSSM connectors is from the perspective of looking through the mid-plane toward the HSSM bay and is shown in the figures below. Note that the switch port to blade bay associations are different between the 14-blade chassis and the 12-blade chassis.

Black Box = Female Pin

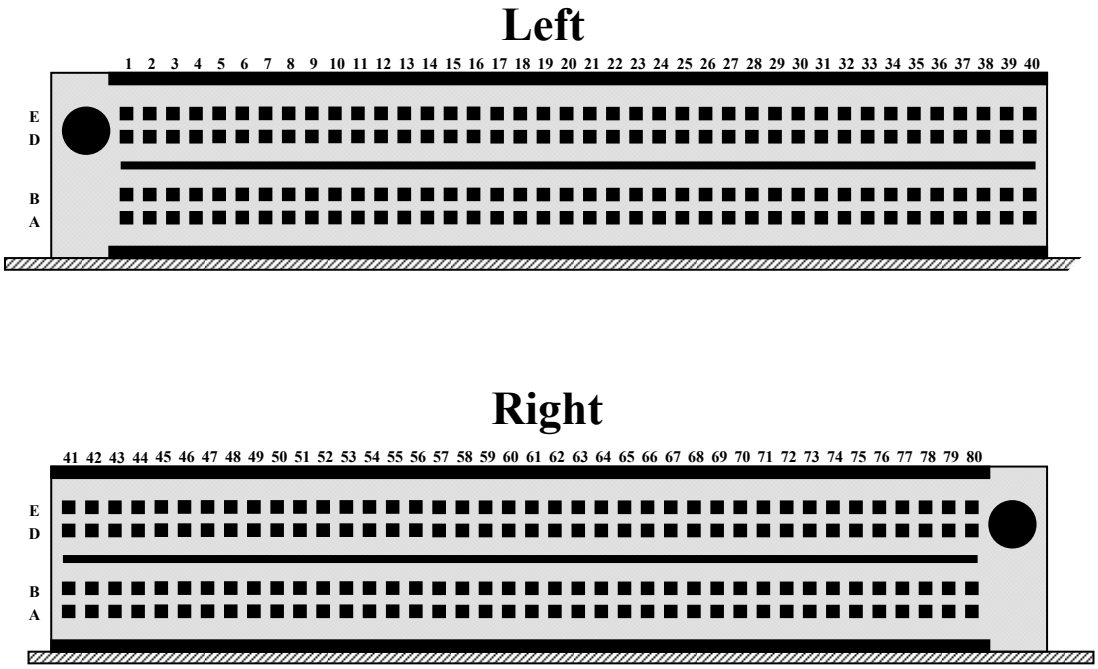


Figure 7-2 - High Speed Switch Module Connectors

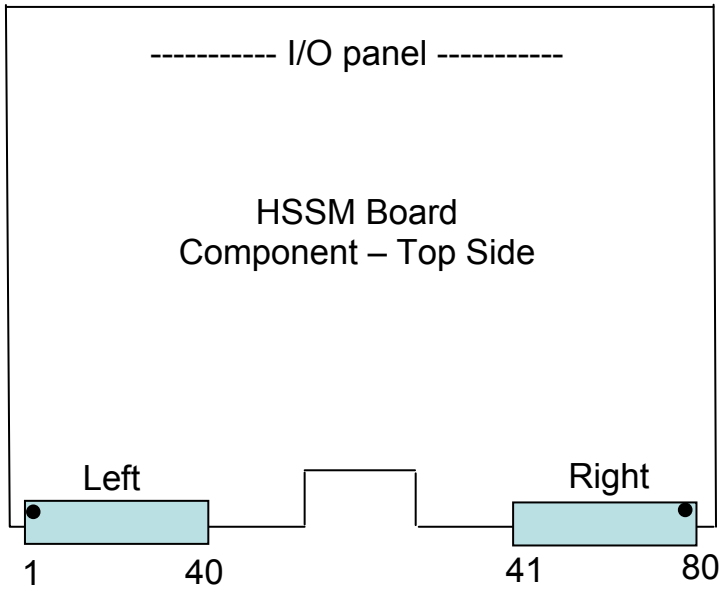


Figure 7-3 - HSSM Board Component

7.1.5 4XSM Ethernet Connection to Management Module

Ethernet connection to the Management Module is the same as for the 1XSM. Reference section 7.1.3.

7.1.6 4X Switch Module pin assignment and signal description – 14-blade 4X chassis

The following table describes the mid-plane connector pin assignments and signal pin information for the HSSM.

Pin	Name	Direction	Description	Transmitter	Receiver
A1	RX_B1_LN1_P	in	4X Fabric from Blade 1: Lane 1, Sense P	BLADE	HSSM
B1	RX_B1_LN1_N	in	4X Fabric from Blade 1: Lane 1, Sense N	BLADE	HSSM
D1	TX_B1_LN1_P	out	4X Fabric to Blade 1: Lane 1, Sense P	HSSM	BLADE
E1	TX_B1_LN1_N	out	4X Fabric to Blade 1: Lane 1, Sense N	HSSM	BLADE
A2	RX_B1_LN2_P	in	4X Fabric from Blade 1: Lane 2, Sense P	BLADE	HSSM
B2	RX_B1_LN2_N	in	4X Fabric from Blade 1: Lane 2, Sense N	BLADE	HSSM
D2	TX_B1_LN2_P	out	4X Fabric to Blade 1: Lane 2, Sense P	HSSM	BLADE
E2	TX_B1_LN2_N	out	4X Fabric to Blade 1: Lane 2, Sense N	HSSM	BLADE
A3	RX_B1_LN3_P	in	4X Fabric from Blade 1: Lane 3, Sense P	BLADE	HSSM
B3	RX_B1_LN3_N	in	4X Fabric from Blade 1: Lane 3, Sense N	BLADE	HSSM
D3	TX_B1_LN3_P	out	4X Fabric to Blade 1: Lane 3, Sense P	HSSM	BLADE
E3	TX_B1_LN3_N	out	4X Fabric to Blade 1: Lane 3, Sense N	HSSM	BLADE
A4	RX_B1_LN4_P	in	4X Fabric from Blade 1: Lane 4, Sense P	BLADE	HSSM
B4	RX_B1_LN4_N	in	4X Fabric from Blade 1: Lane 4, Sense N	BLADE	HSSM
D4	TX_B1_LN4_P	out	4X Fabric to Blade 1: Lane 4, Sense P	HSSM	BLADE
E4	TX_B1_LN4_N	out	4X Fabric to Blade 1: Lane 4, Sense N	HSSM	BLADE
A5	RX_B2_LN1_P	in	4X Fabric from Blade 2: Lane 1, Sense P	BLADE	HSSM
B5	RX_B2_LN1_N	in	4X Fabric from Blade 2: Lane 1, Sense N	BLADE	HSSM
D5	TX_B2_LN1_P	out	4X Fabric to Blade 2: Lane 1, Sense P	HSSM	BLADE
E5	TX_B2_LN1_N	out	4X Fabric to Blade 2: Lane 1, Sense N	HSSM	BLADE
A6	RX_B2_LN2_P	in	4X Fabric from Blade 2: Lane 2, Sense P	BLADE	HSSM
B6	RX_B2_LN2_N	in	4X Fabric from Blade 2: Lane 2, Sense N	BLADE	HSSM
D6	TX_B2_LN2_P	out	4X Fabric to Blade 2: Lane 2, Sense P	HSSM	BLADE
E6	TX_B2_LN2_N	out	4X Fabric to Blade 2: Lane 2, Sense N	HSSM	BLADE
A7	RX_B2_LN3_P	in	4X Fabric from Blade 2: Lane 3, Sense P	BLADE	HSSM
B7	RX_B2_LN3_N	in	4X Fabric from Blade 2: Lane 3, Sense N	BLADE	HSSM
D7	TX_B2_LN3_P	out	4X Fabric to Blade 2: Lane 3, Sense P	HSSM	BLADE
E7	TX_B2_LN3_N	out	4X Fabric to Blade 2: Lane 3, Sense N	HSSM	BLADE
A8	RX_B2_LN4_P	in	4X Fabric from Blade 2: Lane 4, Sense P	BLADE	HSSM
B8	RX_B2_LN4_N	in	4X Fabric from Blade 2: Lane 4, Sense N	BLADE	HSSM
D8	TX_B2_LN4_P	out	4X Fabric to Blade 2: Lane 4, Sense P	HSSM	BLADE
E8	TX_B2_LN4_N	out	4X Fabric to Blade 2: Lane 4, Sense N	HSSM	BLADE
A9	RX_MM1_P	in	Mgmt Fabric from Management Module 1: Sense P	MM	HSSM
B9	RX_MM1_N	in	Mgmt Fabric from Management Module 1: Sense N	MM	HSSM
D9	TX_MM1_P	out	Mgmt Fabric to Management Module 1: Sense P	HSSM	MM
E9	TX_MM1_N	out	Mgmt Fabric to Management Module 1: Sense N	HSSM	MM
A10	RX_MM2_P	in	Mgmt Fabric from Management Module 2: Sense P	MM	HSSM
B10	RX_MM2_N	in	Mgmt Fabric from Management Module 2: Sense N	MM	HSSM
D10	TX_MM2_P	out	Mgmt Fabric to Management Module 2: Sense P	HSSM	MM
E10	TX_MM2_N	out	Mgmt Fabric to Management Module 2: Sense N	HSSM	MM
A11	RX_BM3/4_LN4_P	in	4X Fabric from Bridge Module 3/4: Lane 4, Sense P	BM	HSSM

Pin	Name	Direction	Description	Transmitter	Receiver
B11	RX_BM3/4_LN4_N	in	4X Fabric from Bridge Module 3/4: Lane 4, Sense N	BM	HSSM
D11	TX_BM3/4_LN1_P	out	4X Fabric to Bridge Module 3/4: Lane 1, Sense P	HSSM	BM
E11	TX_BM3/4_LN1_N	out	4X Fabric to Bridge Module 3/4: Lane 1, Sense N	HSSM	BM
A12	RX_BM3/4_LN3_P	in	4X Fabric from Bridge Module 3/4: Lane 3, Sense P	BM	HSSM
B12	RX_BM3/4_LN3_N	in	4X Fabric from Bridge Module 3/4: Lane 3, Sense N	BM	HSSM
D12	TX_BM3/4_LN2_P	out	4X Fabric to Bridge Module 3/4: Lane 2, Sense P	HSSM	BM
E12	TX_BM3/4_LN2_N	out	4X Fabric to Bridge Module 3/4: Lane 2, Sense N	HSSM	BM
A13	RX_BM3/4_LN2_P	in	4X Fabric from Bridge Module 3/4: Lane 2, Sense P	BM	HSSM
B13	RX_BM3/4_LN2_N	in	4X Fabric from Bridge Module 3/4: Lane 2, Sense N	BM	HSSM
D13	TX_BM3/4_LN3_P	out	4X Fabric to Bridge Module 3/4: Lane 3, Sense P	HSSM	BM
E13	TX_BM3/4_LN3_N	out	4X Fabric to Bridge Module 3/4: Lane 3, Sense N	HSSM	BM
A14	RX_BM3/4_LN1_P	in	4X Fabric from Bridge Module 3/4: Lane 1, Sense P	BM	HSSM
B14	RX_BM3/4_LN1_N	in	4X Fabric from Bridge Module 3/4: Lane 1, Sense N	BM	HSSM
D14	TX_BM3/4_LN4_P	out	4X Fabric to Bridge Module 3/4: Lane 4, Sense P	HSSM	BM
E14	TX_BM3/4_LN4_N	out	4X Fabric to Bridge Module 3/4: Lane 4, Sense N	HSSM	BM
A15	RX_B3_LN1_P	in	4X Fabric from Blade 3: Lane 1, Sense P	BLADE	HSSM
B15	RX_B3_LN1_N	in	4X Fabric from Blade 3: Lane 1, Sense N	BLADE	HSSM
D15	TX_B3_LN1_P	out	4X Fabric to Blade 3: Lane 1, Sense P	HSSM	BLADE
E15	TX_B3_LN1_N	out	4X Fabric to Blade 3: Lane 1, Sense N	HSSM	BLADE
A16	RX_B3_LN2_P	in	4X Fabric from Blade 3: Lane 2, Sense P	BLADE	HSSM
B16	RX_B3_LN2_N	in	4X Fabric from Blade 3: Lane 2, Sense N	BLADE	HSSM
D16	TX_B3_LN2_P	out	4X Fabric to Blade 3: Lane 2, Sense P	HSSM	BLADE
E16	TX_B3_LN2_N	out	4X Fabric to Blade 3: Lane 2, Sense N	HSSM	BLADE
A17	RX_B3_LN3_P	in	4X Fabric from Blade 3: Lane 3, Sense P	BLADE	HSSM
B17	RX_B3_LN3_N	in	4X Fabric from Blade 3: Lane 3, Sense N	BLADE	HSSM
D17	TX_B3_LN3_P	out	4X Fabric to Blade 3: Lane 3, Sense P	HSSM	BLADE
E17	TX_B3_LN3_N	out	4X Fabric to Blade 3: Lane 3, Sense N	HSSM	BLADE
A18	RX_B3_LN4_P	in	4X Fabric from Blade 3: Lane 4, Sense P	BLADE	HSSM
B18	RX_B3_LN4_N	in	4X Fabric from Blade 3: Lane 4, Sense N	BLADE	HSSM
D18	TX_B3_LN4_P	out	4X Fabric to Blade 3: Lane 4, Sense P	HSSM	BLADE
E18	TX_B3_LN4_N	out	4X Fabric to Blade 3: Lane 4, Sense N	HSSM	BLADE
A19	12V_1	in	12V In from Source 1		
B19	12V_1	in	12V In from Source 1		
D19	GND		GND		
E19	GND		GND		
A20	12V_1	in	12V In from Source 1		
B20	12V_1	in	12V In from Source 1		
D20	GND		GND		
E20	GND		GND		
A21	12V_1	in	12V In from Source 1		
B21	12V_1	in	12V In from Source 1		
D21	GND		GND		
E21	GND		GND		
A22	12V_1	in	12V In from Source 1		
B22	12V_1	in	12V In from Source 1		
D22	GND		GND		
E22	GND		GND		

Pin	Name	Direction	Description	Transmitter	Receiver
A23	12V_1	in	12V In from Source 1		
B23	12V_1	in	12V In from Source 1		
D23	GND		GND		
E23	GND		GND		
A24	BAY_ID_BIT0	in	Switch Bay ID, Least Significant Bit	chassis	HSSM
B24	BAY_ID_BIT1	in	Switch Bay ID, Middle Significant Bit	chassis	HSSM
D24	BAY_ID_BIT2	in	Switch Bay ID, Most Significant Bit	chassis	HSSM
E24	SELECT_A	in	Control to Enable "A" Signals and Buses	MM	HSSM
A25	RX_B4_LN1_P	in	4X Fabric from Blade 4: Lane 1, Sense P	BLADE	HSSM
B25	RX_B4_LN1_N	in	4X Fabric from Blade 4: Lane 1, Sense N	BLADE	HSSM
D25	TX_B4_LN1_P	out	4X Fabric to Blade 4: Lane 1, Sense P	HSSM	BLADE
E25	TX_B4_LN1_N	out	4X Fabric to Blade 4: Lane 1, Sense N	HSSM	BLADE
A26	RX_B4_LN2_P	in	4X Fabric from Blade 4: Lane 2, Sense P	BLADE	HSSM
B26	RX_B4_LN2_N	in	4X Fabric from Blade 4: Lane 2, Sense N	BLADE	HSSM
D26	TX_B4_LN2_P	out	4X Fabric to Blade 4: Lane 2, Sense P	HSSM	BLADE
E26	TX_B4_LN2_N	out	4X Fabric to Blade 4: Lane 2, Sense N	HSSM	BLADE
A27	RX_B4_LN3_P	in	4X Fabric from Blade 4: Lane 3, Sense P	BLADE	HSSM
B27	RX_B4_LN3_N	in	4X Fabric from Blade 4: Lane 3, Sense N	BLADE	HSSM
D27	TX_B4_LN3_P	out	4X Fabric to Blade 4: Lane 3, Sense P	HSSM	BLADE
E27	TX_B4_LN3_N	out	4X Fabric to Blade 4: Lane 3, Sense N	HSSM	BLADE
A28	RX_B4_LN4_P	in	4X Fabric from Blade 4: Lane 4, Sense P	BLADE	HSSM
B28	RX_B4_LN4_N	in	4X Fabric from Blade 4: Lane 4, Sense N	BLADE	HSSM
D28	TX_B4_LN4_P	out	4X Fabric to Blade 4: Lane 4, Sense P	HSSM	BLADE
E28	TX_B4_LN4_N	out	4X Fabric to Blade 4: Lane 4, Sense N	HSSM	BLADE
A29	RX_B5_LN1_P	in	4X Fabric from Blade 5: Lane 1, Sense P	BLADE	HSSM
B29	RX_B5_LN1_N	in	4X Fabric from Blade 5: Lane 1, Sense N	BLADE	HSSM
D29	TX_B5_LN1_P	out	4X Fabric to Blade 5: Lane 1, Sense P	HSSM	BLADE
E29	TX_B5_LN1_N	out	4X Fabric to Blade 5: Lane 1, Sense N	HSSM	BLADE
A30	RX_B5_LN2_P	in	4X Fabric from Blade 5: Lane 2, Sense P	BLADE	HSSM
B30	RX_B5_LN2_N	in	4X Fabric from Blade 5: Lane 2, Sense N	BLADE	HSSM
D30	TX_B5_LN2_P	out	4X Fabric to Blade 5: Lane 2, Sense P	HSSM	BLADE
E30	TX_B5_LN2_N	out	4X Fabric to Blade 5: Lane 2, Sense N	HSSM	BLADE
A31	RX_B5_LN3_P	in	4X Fabric from Blade 5: Lane 3, Sense P	BLADE	HSSM
B31	RX_B5_LN3_N	in	4X Fabric from Blade 5: Lane 3, Sense N	BLADE	HSSM
D31	TX_B5_LN3_P	out	4X Fabric to Blade 5: Lane 3, Sense P	HSSM	BLADE
E31	TX_B5_LN3_N	out	4X Fabric to Blade 5: Lane 3, Sense N	HSSM	BLADE
A32	RX_B5_LN4_P	in	4X Fabric from Blade 5: Lane 4, Sense P	BLADE	HSSM
B32	RX_B5_LN4_N	in	4X Fabric from Blade 5: Lane 4, Sense N	BLADE	HSSM
D32	TX_B5_LN4_P	out	4X Fabric to Blade 5: Lane 4, Sense P	HSSM	BLADE
E32	TX_B5_LN4_N	out	4X Fabric to Blade 5: Lane 4, Sense N	HSSM	BLADE
A33	RX_B6_LN1_P	in	4X Fabric from Blade 6: Lane 1, Sense P	BLADE	HSSM
B33	RX_B6_LN1_N	in	4X Fabric from Blade 6: Lane 1, Sense N	BLADE	HSSM
D33	TX_B6_LN1_P	out	4X Fabric to Blade 6: Lane 1, Sense P	HSSM	BLADE
E33	TX_B6_LN1_N	out	4X Fabric to Blade 6: Lane 1, Sense N	HSSM	BLADE
A34	RX_B6_LN2_P	in	4X Fabric from Blade 6: Lane 2, Sense P	BLADE	HSSM
B34	RX_B6_LN2_N	in	4X Fabric from Blade 6: Lane 2, Sense N	BLADE	HSSM
D34	TX_B6_LN2_P	out	4X Fabric to Blade 6: Lane 2, Sense P	HSSM	BLADE

Pin	Name	Direction	Description	Transmitter	Receiver
E34	TX_B6_LN2_N	out	4X Fabric to Blade 6: Lane 2, Sense N	HSSM	BLADE
A35	RX_B6_LN3_P	in	4X Fabric from Blade 6: Lane 3, Sense P	BLADE	HSSM
B35	RX_B6_LN3_N	in	4X Fabric from Blade 6: Lane 3, Sense N	BLADE	HSSM
D35	TX_B6_LN3_P	out	4X Fabric to Blade 6: Lane 3, Sense P	HSSM	BLADE
E35	TX_B6_LN3_N	out	4X Fabric to Blade 6: Lane 3, Sense N	HSSM	BLADE
A36	RX_B6_LN4_P	in	4X Fabric from Blade 6: Lane 4, Sense P	BLADE	HSSM
B36	RX_B6_LN4_N	in	4X Fabric from Blade 6: Lane 4, Sense N	BLADE	HSSM
D36	TX_B6_LN4_P	out	4X Fabric to Blade 6: Lane 4, Sense P	HSSM	BLADE
E36	TX_B6_LN4_N	out	4X Fabric to Blade 6: Lane 4, Sense N	HSSM	BLADE
A37	RX_B7_LN1_P	in	4X Fabric from Blade 7: Lane 1, Sense P	BLADE	HSSM
B37	RX_B7_LN1_N	in	4X Fabric from Blade 7: Lane 1, Sense N	BLADE	HSSM
D37	TX_B7_LN1_P	out	4X Fabric to Blade 7: Lane 1, Sense P	HSSM	BLADE
E37	TX_B7_LN1_N	out	4X Fabric to Blade 7: Lane 1, Sense N	HSSM	BLADE
A38	RX_B7_LN2_P	in	4X Fabric from Blade 7: Lane 2, Sense P	BLADE	HSSM
B38	RX_B7_LN2_N	in	4X Fabric from Blade 7: Lane 2, Sense N	BLADE	HSSM
D38	TX_B7_LN2_P	out	4X Fabric to Blade 7: Lane 2, Sense P	HSSM	BLADE
E38	TX_B7_LN2_N	out	4X Fabric to Blade 7: Lane 2, Sense N	HSSM	BLADE
A39	RX_B7_LN3_P	in	4X Fabric from Blade 7: Lane 3, Sense P	BLADE	HSSM
B39	RX_B7_LN3_N	in	4X Fabric from Blade 7: Lane 3, Sense N	BLADE	HSSM
D39	TX_B7_LN3_P	out	4X Fabric to Blade 7: Lane 3, Sense P	HSSM	BLADE
E39	TX_B7_LN3_N	out	4X Fabric to Blade 7: Lane 3, Sense N	HSSM	BLADE
A40	RX_B7_LN4_P	in	4X Fabric from Blade 7: Lane 4, Sense P	BLADE	HSSM
B40	RX_B7_LN4_N	in	4X Fabric from Blade 7: Lane 4, Sense N	BLADE	HSSM
D40	TX_B7_LN4_P	out	4X Fabric to Blade 7: Lane 4, Sense P	HSSM	BLADE
E40	TX_B7_LN4_N	out	4X Fabric to Blade 7: Lane 4, Sense N	HSSM	BLADE
A41	RX_B8_LN1_P	in	4X Fabric from Blade 8: Lane 1, Sense P	BLADE	HSSM
B41	RX_B8_LN1_N	in	4X Fabric from Blade 8: Lane 1, Sense N	BLADE	HSSM
D41	TX_B8_LN1_P	out	4X Fabric to Blade 8: Lane 1, Sense P	HSSM	BLADE
E41	TX_B8_LN1_N	out	4X Fabric to Blade 8: Lane 1, Sense N	HSSM	BLADE
A42	RX_B8_LN2_P	in	4X Fabric from Blade 8: Lane 2, Sense P	BLADE	HSSM
B42	RX_B8_LN2_N	in	4X Fabric from Blade 8: Lane 2, Sense N	BLADE	HSSM
D42	TX_B8_LN2_P	out	4X Fabric to Blade 8: Lane 2, Sense P	HSSM	BLADE
E42	TX_B8_LN2_N	out	4X Fabric to Blade 8: Lane 2, Sense N	HSSM	BLADE
A43	RX_B8_LN3_P	in	4X Fabric from Blade 8: Lane 3, Sense P	BLADE	HSSM
B43	RX_B8_LN3_N	in	4X Fabric from Blade 8: Lane 3, Sense N	BLADE	HSSM
D43	TX_B8_LN3_P	out	4X Fabric to Blade 8: Lane 3, Sense P	HSSM	BLADE
E43	TX_B8_LN3_N	out	4X Fabric to Blade 8: Lane 3, Sense N	HSSM	BLADE
A44	RX_B8_LN4_P	in	4X Fabric from Blade 8: Lane 4, Sense P	BLADE	HSSM
B44	RX_B8_LN4_N	in	4X Fabric from Blade 8: Lane 4, Sense N	BLADE	HSSM
D44	TX_B8_LN4_P	out	4X Fabric to Blade 8: Lane 4, Sense P	HSSM	BLADE
E44	TX_B8_LN4_N	out	4X Fabric to Blade 8: Lane 4, Sense N	HSSM	BLADE
A45	RX_B9_LN1_P	in	4X Fabric from Blade 9: Lane 1, Sense P	BLADE	HSSM
B45	RX_B9_LN1_N	in	4X Fabric from Blade 9: Lane 1, Sense N	BLADE	HSSM
D45	TX_B9_LN1_P	out	4X Fabric to Blade 9: Lane 1, Sense P	HSSM	BLADE
E45	TX_B9_LN1_N	out	4X Fabric to Blade 9: Lane 1, Sense N	HSSM	BLADE
A46	RX_B9_LN2_P	in	4X Fabric from Blade 9: Lane 2, Sense P	BLADE	HSSM
B46	RX_B9_LN2_N	in	4X Fabric from Blade 9: Lane 2, Sense N	BLADE	HSSM

Pin	Name	Direction	Description	Transmitter	Receiver
D46	TX_B9_LN2_P	out	4X Fabric to Blade 9: Lane 2, Sense P	HSSM	BLADE
E46	TX_B9_LN2_N	out	4X Fabric to Blade 9: Lane 2, Sense N	HSSM	BLADE
A47	RX_B9_LN3_P	in	4X Fabric from Blade 9: Lane 3, Sense P	BLADE	HSSM
B47	RX_B9_LN3_N	in	4X Fabric from Blade 9: Lane 3, Sense N	BLADE	HSSM
D47	TX_B9_LN3_P	out	4X Fabric to Blade 9: Lane 3, Sense P	HSSM	BLADE
E47	TX_B9_LN3_N	out	4X Fabric to Blade 9: Lane 3, Sense N	HSSM	BLADE
A48	RX_B9_LN4_P	in	4X Fabric from Blade 9: Lane 4, Sense P	BLADE	HSSM
B48	RX_B9_LN4_N	in	4X Fabric from Blade 9: Lane 4, Sense N	BLADE	HSSM
D48	TX_B9_LN4_P	out	4X Fabric to Blade 9: Lane 4, Sense P	HSSM	BLADE
E48	TX_B9_LN4_N	out	4X Fabric to Blade 9: Lane 4, Sense N	HSSM	BLADE
A49	RX_B10_LN1_P	in	4X Fabric from Blade 10: Lane 1, Sense P	BLADE	HSSM
B49	RX_B10_LN1_N	in	4X Fabric from Blade 10: Lane 1, Sense N	BLADE	HSSM
D49	TX_B10_LN1_P	out	4X Fabric to Blade 10: Lane 1, Sense P	HSSM	BLADE
E49	TX_B10_LN1_N	out	4X Fabric to Blade 10: Lane 1, Sense N	HSSM	BLADE
A50	RX_B10_LN2_P	in	4X Fabric from Blade 10: Lane 2, Sense P	BLADE	HSSM
B50	RX_B10_LN2_N	in	4X Fabric from Blade 10: Lane 2, Sense N	BLADE	HSSM
D50	TX_B10_LN2_P	out	4X Fabric to Blade 10: Lane 2, Sense P	HSSM	BLADE
E50	TX_B10_LN2_N	out	4X Fabric to Blade 10: Lane 2, Sense N	HSSM	BLADE
A51	RX_B10_LN3_P	in	4X Fabric from Blade 10: Lane 3, Sense P	BLADE	HSSM
B51	RX_B10_LN3_N	in	4X Fabric from Blade 10: Lane 3, Sense N	BLADE	HSSM
D51	TX_B10_LN3_P	out	4X Fabric to Blade 10: Lane 3, Sense P	HSSM	BLADE
E51	TX_B10_LN3_N	out	4X Fabric to Blade 10: Lane 3, Sense N	HSSM	BLADE
A52	RX_B10_LN4_P	in	4X Fabric from Blade 10: Lane 4, Sense P	BLADE	HSSM
B52	RX_B10_LN4_N	in	4X Fabric from Blade 10: Lane 4, Sense N	BLADE	HSSM
D52	TX_B10_LN4_P	out	4X Fabric to Blade 10: Lane 4, Sense P	HSSM	BLADE
E52	TX_B10_LN4_N	out	4X Fabric to Blade 10: Lane 4, Sense N	HSSM	BLADE
A53	I2C_SDA(B)	i/o	I2C Data (B)	MM & HSSM	MM & HSSM
B53	I2C_SCL(B)	i/o	I2C Clock (B)	MM & HSSM	MM & HSSM
D53	SELECT_B	in	Control to Enable "B" Signals and Buses	MM	HSSM
E53	PRESENT_N	out	High Speed Switch Module Present	HSSM	MM
A54	RX_B11_LN1_P	in	4X Fabric from Blade 11: Lane 1, Sense P	BLADE	HSSM
B54	RX_B11_LN1_N	in	4X Fabric from Blade 11: Lane 1, Sense N	BLADE	HSSM
D54	TX_B11_LN1_P	out	4X Fabric to Blade 11: Lane 1, Sense P	HSSM	BLADE
E54	TX_B11_LN1_N	out	4X Fabric to Blade 11: Lane 1, Sense N	HSSM	BLADE
A55	RX_B11_LN2_P	in	4X Fabric from Blade 11: Lane 2, Sense P	BLADE	HSSM
B55	RX_B11_LN2_N	in	4X Fabric from Blade 11: Lane 2, Sense N	BLADE	HSSM
D55	TX_B11_LN2_P	out	4X Fabric to Blade 11: Lane 2, Sense P	HSSM	BLADE
E55	TX_B11_LN2_N	out	4X Fabric to Blade 11: Lane 2, Sense N	HSSM	BLADE
A56	RX_B11_LN3_P	in	4X Fabric from Blade 11: Lane 3, Sense P	BLADE	HSSM
B56	RX_B11_LN3_N	in	4X Fabric from Blade 11: Lane 3, Sense N	BLADE	HSSM
D56	TX_B11_LN3_P	out	4X Fabric to Blade 11: Lane 3, Sense P	HSSM	BLADE
E56	TX_B11_LN3_N	out	4X Fabric to Blade 11: Lane 3, Sense N	HSSM	BLADE
A57	RX_B11_LN4_P	in	4X Fabric from Blade 11: Lane 4, Sense P	BLADE	HSSM
B57	RX_B11_LN4_N	in	4X Fabric from Blade 11: Lane 4, Sense N	BLADE	HSSM
D57	TX_B11_LN4_P	out	4X Fabric to Blade 11: Lane 4, Sense P	HSSM	BLADE
E57	TX_B11_LN4_N	out	4X Fabric to Blade 11: Lane 4, Sense N	HSSM	BLADE
A58	12V_2	in	12V In from Source 2		

Pin	Name	Direction	Description	Transmitter	Receiver
B58	12V_2	in	12V In from Source 2		
D58	GND		GND		
E58	GND		GND		
A59	12V_2	in	12V In from Source 2		
B59	12V_2	in	12V In from Source 2		
D59	GND		GND		
E59	GND		GND		
A60	12V_2	in	12V In from Source 2		
B60	12V_2	in	12V In from Source 2		
D60	GND		GND		
E60	GND		GND		
A61	12V_2	in	12V In from Source 2		
B61	12V_2	in	12V In from Source 2		
D61	GND		GND		
E61	GND		GND		
A62	12V_2	in	12V In from Source 2		
B62	12V_2	in	12V In from Source 2		
D62	GND		GND		
E62	GND		GND		
A63	RX_B12_LN1_P	in	4X Fabric from Blade 12: Lane 1, Sense P	BLADE	HSSM
B63	RX_B12_LN1_N	in	4X Fabric from Blade 12: Lane 1, Sense N	BLADE	HSSM
D63	TX_B12_LN1_P	out	4X Fabric to Blade 12: Lane 1, Sense P	HSSM	BLADE
E63	TX_B12_LN1_N	out	4X Fabric to Blade 12: Lane 1, Sense N	HSSM	BLADE
A64	RX_B12_LN2_P	in	4X Fabric from Blade 12: Lane 2, Sense P	BLADE	HSSM
B64	RX_B12_LN2_N	in	4X Fabric from Blade 12: Lane 2, Sense N	BLADE	HSSM
D64	TX_B12_LN2_P	out	4X Fabric to Blade 12: Lane 2, Sense P	HSSM	BLADE
E64	TX_B12_LN2_N	out	4X Fabric to Blade 12: Lane 2, Sense N	HSSM	BLADE
A65	RX_B12_LN3_P	in	4X Fabric from Blade 12: Lane 3, Sense P	BLADE	HSSM
B65	RX_B12_LN3_N	in	4X Fabric from Blade 12: Lane 3, Sense N	BLADE	HSSM
D65	TX_B12_LN3_P	out	4X Fabric to Blade 12: Lane 3, Sense P	HSSM	BLADE
E65	TX_B12_LN3_N	out	4X Fabric to Blade 12: Lane 3, Sense N	HSSM	BLADE
A66	RX_B12_LN4_P	in	4X Fabric from Blade 12: Lane 4, Sense P	BLADE	HSSM
B66	RX_B12_LN4_N	in	4X Fabric from Blade 12: Lane 4, Sense N	BLADE	HSSM
D66	TX_B12_LN4_P	out	4X Fabric to Blade 12: Lane 4, Sense P	HSSM	BLADE
E66	TX_B12_LN4_N	out	4X Fabric to Blade 12: Lane 4, Sense N	HSSM	BLADE
A67	RX_B13_LN1_P	in	4X Fabric from Blade 13: Lane 1, Sense P	BLADE	HSSM
B67	RX_B13_LN1_N	in	4X Fabric from Blade 13: Lane 1, Sense N	BLADE	HSSM
D67	TX_B13_LN1_P	out	4X Fabric to Blade 13: Lane 1, Sense P	HSSM	BLADE
E67	TX_B13_LN1_N	out	4X Fabric to Blade 13: Lane 1, Sense N	HSSM	BLADE
A68	RX_B13_LN2_P	in	4X Fabric from Blade 13: Lane 2, Sense P	BLADE	HSSM
B68	RX_B13_LN2_N	in	4X Fabric from Blade 13: Lane 2, Sense N	BLADE	HSSM
D68	TX_B13_LN2_P	out	4X Fabric to Blade 13: Lane 2, Sense P	HSSM	BLADE
E68	TX_B13_LN2_N	out	4X Fabric to Blade 13: Lane 2, Sense N	HSSM	BLADE
A69	I2C_SDA(A)	i/o	I2C Data (A)	MM & HSSM	MM & HSSM
B69	I2C_RESET_N	in	I2C Reset	MM	HSSM
D69	I2C_INT_N(A)	out	I2C Interrupt (A)	HSSM	MM
E69	I2C_INT_N(B)	out	I2C Interrupt (B)	HSSM	MM

Pin	Name	Direction	Description	Transmitter	Receiver
A70	I2C_SCL(A)	i/o	I2C Clock (A)	MM & HSSM	MM & HSSM
B70	Reserved		Reserved – do not connect		
D70	Reserved		Reserved – do not connect		
E70	Reserved		Reserved – do not connect		
A71	RX_B13_LN3_P	in	4X Fabric from Blade 13: Lane 3, Sense P	BLADE	HSSM
B71	RX_B13_LN3_N	in	4X Fabric from Blade 13: Lane 3, Sense N	BLADE	HSSM
D71	TX_B13_LN3_P	out	4X Fabric to Blade 13: Lane 3, Sense P	HSSM	BLADE
E71	TX_B13_LN3_N	out	4X Fabric to Blade 13: Lane 3, Sense N	HSSM	BLADE
A72	RX_B13_LN4_P	in	4X Fabric from Blade 13: Lane 4, Sense P	BLADE	HSSM
B72	RX_B13_LN4_N	in	4X Fabric from Blade 13: Lane 4, Sense N	BLADE	HSSM
D72	TX_B13_LN4_P	out	4X Fabric to Blade 13: Lane 4, Sense P	HSSM	BLADE
E72	TX_B13_LN4_N	out	4X Fabric to Blade 13: Lane 4, Sense N	HSSM	BLADE
A73	RX_BM5/6_LN4_P	in	4X Fabric from Bridge Module 5/6: Lane 4, Sense P	BM	HSSM
B73	RX_BM5/6_LN4_N	in	4X Fabric from Bridge Module 5/6: Lane 4, Sense N	BM	HSSM
D73	TX_BM5/6_LN1_P	out	4X Fabric to Bridge Module 5/6: Lane 1, Sense P	HSSM	BM
E73	TX_BM5/6_LN1_N	out	4X Fabric to Bridge Module 5/6: Lane 1, Sense N	HSSM	BM
A74	RX_BM5/6_LN3_P	in	4X Fabric from Bridge Module 5/6: Lane 3, Sense P	BM	HSSM
B74	RX_BM5/6_LN3_N	in	4X Fabric from Bridge Module 5/6: Lane 3, Sense N	BM	HSSM
D74	TX_BM5/6_LN2_P	out	4X Fabric to Bridge Module 5/6: Lane 2, Sense P	HSSM	BM
E74	TX_BM5/6_LN2_N	out	4X Fabric to Bridge Module 5/6: Lane 2, Sense N	HSSM	BM
A75	RX_BM5/6_LN2_P	in	4X Fabric from Bridge Module 5/6: Lane 2, Sense P	BM	HSSM
B75	RX_BM5/6_LN2_N	in	4X Fabric from Bridge Module 5/6: Lane 2, Sense N	BM	HSSM
D75	TX_BM5/6_LN3_P	out	4X Fabric to Bridge Module 5/6: Lane 3, Sense P	HSSM	BM
E75	TX_BM5/6_LN3_N	out	4X Fabric to Bridge Module 5/6: Lane 3, Sense N	HSSM	BM
A76	RX_BM5/6_LN1_P	in	4X Fabric from Bridge Module 5/6: Lane 1, Sense P	BM	HSSM
B76	RX_BM5/6_LN1_N	in	4X Fabric from Bridge Module 5/6: Lane 1, Sense N	BM	HSSM
D76	TX_BM5/6_LN4_P	out	4X Fabric to Bridge Module 5/6: Lane 4, Sense P	HSSM	BM
E76	TX_BM5/6_LN4_N	out	4X Fabric to Bridge Module 5/6: Lane 4, Sense N	HSSM	BM
A77	RX_B14_LN1_P	in	4X Fabric from Blade 14: Lane 1, Sense P	BLADE	HSSM
B77	RX_B14_LN1_N	in	4X Fabric from Blade 14: Lane 1, Sense N	BLADE	HSSM
D77	TX_B14_LN1_P	out	4X Fabric to Blade 14: Lane 1, Sense P	HSSM	BLADE
E77	TX_B14_LN1_N	out	4X Fabric to Blade 14: Lane 1, Sense N	HSSM	BLADE
A78	RX_B14_LN2_P	in	4X Fabric from Blade 14: Lane 2, Sense P	BLADE	HSSM
B78	RX_B14_LN2_N	in	4X Fabric from Blade 14: Lane 2, Sense N	BLADE	HSSM
D78	TX_B14_LN2_P	out	4X Fabric to Blade 14: Lane 2, Sense P	HSSM	BLADE
E78	TX_B14_LN2_N	out	4X Fabric to Blade 14: Lane 2, Sense N	HSSM	BLADE
A79	RX_B14_LN3_P	in	4X Fabric from Blade 14: Lane 3, Sense P	BLADE	HSSM
B79	RX_B14_LN3_N	in	4X Fabric from Blade 14: Lane 3, Sense N	BLADE	HSSM
D79	TX_B14_LN3_P	out	4X Fabric to Blade 14: Lane 3, Sense P	HSSM	BLADE
E79	TX_B14_LN3_N	out	4X Fabric to Blade 14: Lane 3, Sense N	HSSM	BLADE
A80	RX_B14_LN4_P	in	4X Fabric from Blade 14: Lane 4, Sense P	BLADE	HSSM
B80	RX_B14_LN4_N	in	4X Fabric from Blade 14: Lane 4, Sense N	BLADE	HSSM
D80	TX_B14_LN4_P	out	4X Fabric to Blade 14: Lane 4, Sense P	HSSM	BLADE
E80	TX_B14_LN4_N	out	4X Fabric to Blade 14: Lane 4, Sense N	HSSM	BLADE

Table 7-8 High Speed Switch Module Connectors Pin Definitions (14-blade 4X chassis)

HSSM Pin Table Notes:

1. "Transformerless" Ethernet connection (pins A9, B9, D9, E9, A10, B10, D10, E10). See section 7.1.3 for additional details.
2. Three mid-plane inputs to the HSSM (pins A24, B24, D24) used to determine the low order nibble of the switch default IP address. The HSSM MUST provide voltage pull-ups. Low signal levels are provided by 100 ohm pull-downs to ground on the mid-plane, high levels not provided by the mid-plane.
3. 5V pull-up provided on mid-plane for Select_A/B (pins E24, D53), switch must not use pullup resistor. 50 ohms +/-10% impedance.
4. 100 Khz I^2C serial data lines (pins A69, A53). 5V pull-up on mid-plane, switch must not use pullup resistor. 50 ohms +/-10% impedance. Signals multiplexed on the switch , refer to I^2C section of this document for additional details.
5. 100 Khz I^2C serial clock lines (pins A70, B53). 5V pull-up on mid-plane, switch must not use pullup resistor. 50 ohms +/-10% impedance. Signals multiplexed on the switch , refer to I^2C section of this document for additional details.
6. 5V 4.7K pull-up provided on mid-plane for Present_N (pin E53). HSSM grounds through 100 ohm resistor to indicate presence to Management Modules.
7. 5V pull-up provided on mid-plane for I2C Reset_N (pin B69), switch must not use pullup resistor. 50 ohms +/-10% impedance. Shared line that when asserted by either MM forces the HSSM to clear its I^2C bus protocol unit (de-asserts all SDA and SCL lines). Active Low signal.
8. 5V pull-up provided on mid-plane for I2C_Int_N (A/B) (pins D69, E69), switch must not use pullup resistor. 50 ohms +/-10% impedance. Active low signals. HSSM provides open collector.
9. Dedicated bridge module bays 1 & 2 have been renumbered to bays 5 & 6 in version 2.07 and later of this document.
10. When using the HSSM to bridge module lanes, wiring should begin with the logical lowest lane 1. Up to four lanes are available for connectivity between the HSSM and bridge modules.

7.1.7 4X Switch Module pin assignment and signal description – 12-blade 4X chassis

The following table describes the mid-plane connector pin assignments and signal pin information for the HSSM in the 12-blade 4X chassis.

Due to the horizontal transposition of the HSSM from the rear of the 14-blade 4X chassis to the front of the 12-blade 4X chassis, the port assignments are transposed to resolve a "bow tie" affect of reversing the blade port assignments end-to-end. In this transposition, only blade ports are traded with blade ports, and bridge ports with bridge ports. Bridge ports have a slightly different interconnect with the paired HSSM.

Note: Lanes were NOT transposed, nor were the 'P' and 'N' sense to the serdes pairs. Power, ground, and the connections to the Management Modules were also not re-assigned.

The table below described the logical port assignment for High Speed Switch Modules per chassis type.

Table 7-9 - Logical port assignment for 4x Switch Modules per chassis type

Port Naming Convention	14-blade chassis Port Connection				12-blade chassis Port Connection			
INT1	Blade Server Slot 1				Blade Server Slot 12			
INT2	Blade Server Slot 2				Interswitch Link 1			
INT3	Blade Server Slot 3				Blade Server Slot 11			
INT4	Blade Server Slot 4				Interswitch Link 2			
INT5	Blade Server Slot 5				Blade Server Slot 10			
INT6	Blade Server Slot 6				Blade Server Slot 9			
INT7	Blade Server Slot 7				Blade Server Slot 8			
INT8	Blade Server Slot 8				Blade Server Slot 7			
INT9	Blade Server Slot 9				Blade Server Slot 6			
INT10	Blade Server Slot 10				Blade Server Slot 5			
INT11	Blade Server Slot 11				Blade Server Slot 4			
INT12	Blade Server Slot 12				Blade Server Slot 3			
INT13	Blade Server Slot 13				Blade Server Slot 2			
INT14	Blade Server Slot 14				Blade Server Slot 1			
MGT1	Management Module 1				Management Module 1			
MGT2	Management Module 2				Management Module 2			
EXT1-X	External Port 1-X				External Port 1-X			
HSSM Bay →	**7**	**8**	**9**	**10**	**7**	**8**	**9**	**10**
BR1	5	6	5	6	3	2	3	2
BR2	3	4	3	4	4	1	4	1

Note that bridge fabrics between HSSMs are different between the two 4X chassis. Redundant bridge support is obtained as follows:

14-blade 4X chassis: HSSM 7 & 9 obtain redundant bridge connections via BM5 & BM3
HSSM 8 & 10 obtain redundant bridge connections via BM6 & BM4

12-blade 4X chassis: HSSM 7 & 9 obtain redundant bridge connections via BM3 & BM4
HSSM 8 & 10 obtain redundant bridge connections via BM2 & BM1

Detailed HSSM pin assignments in the 12-blade 4X chassis.

Table 7-10 - 4x Switch Module pin assignments in a 12-blade 4X chassis

Pin	Name	Description	Transmitter	Receiver
A1	RX_B12_LN1_P	4X Fabric from Blade 12: Lane 1, Sense P	BLADE	HSSM
B1	RX_B12_LN1_N	4X Fabric from Blade 12: Lane 1, Sense N	BLADE	HSSM
D1	TX_B12_LN1_P	4X Fabric to Blade 12: Lane 1, Sense P	HSSM	BLADE
E1	TX_B12_LN1_N	4X Fabric to Blade 12: Lane 1, Sense N	HSSM	BLADE
A2	RX_B12_LN2_P	4X Fabric from Blade 12: Lane 2, Sense P	BLADE	HSSM
B2	RX_B12_LN2_N	4X Fabric from Blade 12: Lane 2, Sense N	BLADE	HSSM
D2	TX_B12_LN2_P	4X Fabric to Blade 12: Lane 2, Sense P	HSSM	BLADE
E2	TX_B12_LN2_N	4X Fabric to Blade 12: Lane 2, Sense N	HSSM	BLADE
A3	RX_B12_LN3_P	4X Fabric from Blade 12: Lane 3, Sense P	BLADE	HSSM
B3	RX_B12_LN3_N	4X Fabric from Blade 12: Lane 3, Sense N	BLADE	HSSM
D3	TX_B12_LN3_P	4X Fabric to Blade 12: Lane 3, Sense P	HSSM	BLADE
E3	TX_B12_LN3_N	4X Fabric to Blade 12: Lane 3, Sense N	HSSM	BLADE
A4	RX_B12_LN4_P	4X Fabric from Blade 12: Lane 4, Sense P	BLADE	HSSM
B4	RX_B12_LN4_N	4X Fabric from Blade 12: Lane 4, Sense N	BLADE	HSSM
D4	TX_B12_LN4_P	4X Fabric to Blade 12: Lane 4, Sense P	HSSM	BLADE
E4	TX_B12_LN4_N	4X Fabric to Blade 12: Lane 4, Sense N	HSSM	BLADE
x5-x8		Inter-Switch Link (See table below)	HSSM	HSSM
A9	RX_MM1_P	Mgmt Fabric from Management Module 1: Sense P	MM	HSSM
B9	RX_MM1_N	Mgmt Fabric from Management Module 1: Sense N	MM	HSSM
D9	TX_MM1_P	Mgmt Fabric to Management Module 1: Sense P	HSSM	MM
E9	TX_MM1_N	Mgmt Fabric to Management Module 1: Sense N	HSSM	MM
A10	RX_MM2_P	Mgmt Fabric from Management Module 2: Sense P	MM	HSSM
B10	RX_MM2_N	Mgmt Fabric from Management Module 2: Sense N	MM	HSSM
D10	TX_MM2_P	Mgmt Fabric to Management Module 2: Sense P	HSSM	MM
E10	TX_MM2_N	Mgmt Fabric to Management Module 2: Sense N	HSSM	MM
A11	RX_BM4/1_LN4_P	4X Fabric from Bridge Module 4/1: Lane 4, Sense P	BM	HSSM
B11	RX_BM4/1_LN4_N	4X Fabric from Bridge Module 4/1: Lane 4, Sense N	BM	HSSM
D11	TX_BM4/1_LN1_P	4X Fabric to Bridge Module 4/1: Lane 1, Sense P	HSSM	BM
E11	TX_BM4/1_LN1_N	4X Fabric to Bridge Module 4/1: Lane 1, Sense N	HSSM	BM
A12	RX_BM4/1_LN3_P	4X Fabric from Bridge Module 4/1: Lane 3, Sense P	BM	HSSM
B12	RX_BM4/1_LN3_N	4X Fabric from Bridge Module 4/1: Lane 3, Sense N	BM	HSSM
D12	TX_BM4/1_LN2_P	4X Fabric to Bridge Module 4/1: Lane 2, Sense P	HSSM	BM
E12	TX_BM4/1_LN2_N	4X Fabric to Bridge Module 4/1: Lane 2, Sense N	HSSM	BM
A13	RX_BM4/1_LN2_P	4X Fabric from Bridge Module 4/1: Lane 2, Sense P	BM	HSSM
B13	RX_BM4/1_LN2_N	4X Fabric from Bridge Module 4/1: Lane 2, Sense N	BM	HSSM
D13	TX_BM4/1_LN3_P	4X Fabric to Bridge Module 4/1: Lane 3, Sense P	HSSM	BM
E13	TX_BM4/1_LN3_N	4X Fabric to Bridge Module 4/1: Lane 3, Sense N	HSSM	BM
A14	RX_BM4/1_LN1_P	4X Fabric from Bridge Module 4/1: Lane 1, Sense P	BM	HSSM
B14	RX_BM4/1_LN1_N	4X Fabric from Bridge Module 4/1: Lane 1, Sense N	BM	HSSM

D14	TX_BM4/1_LN4_P	4X Fabric to Bridge Module 4/1: Lane 4, Sense P	HSSM	BM
E14	TX_BM4/1_LN4_N	4X Fabric to Bridge Module 4/1: Lane 4, Sense N	HSSM	BM
A15	RX_B11_LN1_P	4X Fabric from Blade 11: Lane 1, Sense P	BLADE	HSSM
B15	RX_B11_LN1_N	4X Fabric from Blade 11: Lane 1, Sense N	BLADE	HSSM
D15	TX_B11_LN1_P	4X Fabric to Blade 11: Lane 1, Sense P	HSSM	BLADE
E15	TX_B11_LN1_N	4X Fabric to Blade 11: Lane 1, Sense N	HSSM	BLADE
A16	RX_B11_LN2_P	4X Fabric from Blade 11: Lane 2, Sense P	BLADE	HSSM
B16	RX_B11_LN2_N	4X Fabric from Blade 11: Lane 2, Sense N	BLADE	HSSM
D16	TX_B11_LN2_P	4X Fabric to Blade 11: Lane 2, Sense P	HSSM	BLADE
E16	TX_B11_LN2_N	4X Fabric to Blade 11: Lane 2, Sense N	HSSM	BLADE
A17	RX_B11_LN3_P	4X Fabric from Blade 11: Lane 3, Sense P	BLADE	HSSM
B17	RX_B11_LN3_N	4X Fabric from Blade 11: Lane 3, Sense N	BLADE	HSSM
D17	TX_B11_LN3_P	4X Fabric to Blade 11: Lane 3, Sense P	HSSM	BLADE
E17	TX_B11_LN3_N	4X Fabric to Blade 11: Lane 3, Sense N	HSSM	BLADE
A18	RX_B11_LN4_P	4X Fabric from Blade 11: Lane 4, Sense P	BLADE	HSSM
B18	RX_B11_LN4_N	4X Fabric from Blade 11: Lane 4, Sense N	BLADE	HSSM
D18	TX_B11_LN4_P	4X Fabric to Blade 11: Lane 4, Sense P	HSSM	BLADE
E18	TX_B11_LN4_N	4X Fabric to Blade 11: Lane 4, Sense N	HSSM	BLADE
A19	12V_1	12V In from Source 1		
B19	12V_1	12V In from Source 1		
D19	GND	GND		
E19	GND	GND		
A20	12V_1	12V In from Source 1		
B20	12V_1	12V In from Source 1		
D20	GND	GND		
E20	GND	GND		
A21	12V_1	12V In from Source 1		
B21	12V_1	12V In from Source 1		
D21	GND	GND		
E21	GND	GND		
A22	12V_1	12V In from Source 1		
B22	12V_1	12V In from Source 1		
D22	GND	GND		
E22	GND	GND		
A23	12V_1	12V In from Source 1		
B23	12V_1	12V In from Source 1		
D23	GND	GND		
E23	GND	GND		
A24	BAY_ID_BIT0	Switch Bay ID, Least Significant Bit	Chassis	HSSM
B24	BAY_ID_BIT1	Switch Bay ID, Middle Significant Bit	Chassis	HSSM
D24	BAY_ID_BIT2	Switch Bay ID, Most Significant Bit	Chassis	HSSM
E24	SELECT_A	Control to Enable "A" Signals and Buses	MM	HSSM
x25-x28		Inter-Switch Link (See table below)	HSSM	HSSM
A29	RX_B10_LN1_P	4X Fabric from Blade 10: Lane 1, Sense P	BLADE	HSSM

B29	RX_B10_LN1_N	4X Fabric from Blade 10: Lane 1, Sense N	BLADE	HSSM
D29	TX_B10_LN1_P	4X Fabric to Blade 10: Lane 1, Sense P	HSSM	BLADE
E29	TX_B10_LN1_N	4X Fabric to Blade 10: Lane 1, Sense N	HSSM	BLADE
A30	RX_B10_LN2_P	4X Fabric from Blade 10: Lane 2, Sense P	BLADE	HSSM
B30	RX_B10_LN2_N	4X Fabric from Blade 10: Lane 2, Sense N	BLADE	HSSM
D30	TX_B10_LN2_P	4X Fabric to Blade 10: Lane 2, Sense P	HSSM	BLADE
E30	TX_B10_LN2_N	4X Fabric to Blade 10: Lane 2, Sense N	HSSM	BLADE
A31	RX_B10_LN3_P	4X Fabric from Blade 10: Lane 3, Sense P	BLADE	HSSM
B31	RX_B10_LN3_N	4X Fabric from Blade 10: Lane 3, Sense N	BLADE	HSSM
D31	TX_B10_LN3_P	4X Fabric to Blade 10: Lane 3, Sense P	HSSM	BLADE
E31	TX_B10_LN3_N	4X Fabric to Blade 10: Lane 3, Sense N	HSSM	BLADE
A32	RX_B10_LN4_P	4X Fabric from Blade 10: Lane 4, Sense P	BLADE	HSSM
B32	RX_B10_LN4_N	4X Fabric from Blade 10: Lane 4, Sense N	BLADE	HSSM
D32	TX_B10_LN4_P	4X Fabric to Blade 10: Lane 4, Sense P	HSSM	BLADE
E32	TX_B10_LN4_N	4X Fabric to Blade 10: Lane 4, Sense N	HSSM	BLADE
A33	RX_B9_LN1_P	4X Fabric from Blade 9: Lane 1, Sense P	BLADE	HSSM
B33	RX_B9_LN1_N	4X Fabric from Blade 9: Lane 1, Sense N	BLADE	HSSM
D33	TX_B9_LN1_P	4X Fabric to Blade 9: Lane 1, Sense P	HSSM	BLADE
E33	TX_B9_LN1_N	4X Fabric to Blade 9: Lane 1, Sense N	HSSM	BLADE
A34	RX_B9_LN2_P	4X Fabric from Blade 9: Lane 2, Sense P	BLADE	HSSM
B34	RX_B9_LN2_N	4X Fabric from Blade 9: Lane 2, Sense N	BLADE	HSSM
D34	TX_B9_LN2_P	4X Fabric to Blade 9: Lane 2, Sense P	HSSM	BLADE
E34	TX_B9_LN2_N	4X Fabric to Blade 9: Lane 2, Sense N	HSSM	BLADE
A35	RX_B9_LN3_P	4X Fabric from Blade 9: Lane 3, Sense P	BLADE	HSSM
B35	RX_B9_LN3_N	4X Fabric from Blade 9: Lane 3, Sense N	BLADE	HSSM
D35	TX_B9_LN3_P	4X Fabric to Blade 9: Lane 3, Sense P	HSSM	BLADE
E35	TX_B9_LN3_N	4X Fabric to Blade 9: Lane 3, Sense N	HSSM	BLADE
A36	RX_B9_LN4_P	4X Fabric from Blade 9: Lane 4, Sense P	BLADE	HSSM
B36	RX_B9_LN4_N	4X Fabric from Blade 9: Lane 4, Sense N	BLADE	HSSM
D36	TX_B9_LN4_P	4X Fabric to Blade 9: Lane 4, Sense P	HSSM	BLADE
E36	TX_B9_LN4_N	4X Fabric to Blade 9: Lane 4, Sense N	HSSM	BLADE
A37	RX_B8_LN1_P	4X Fabric from Blade 8: Lane 1, Sense P	BLADE	HSSM
B37	RX_B8_LN1_N	4X Fabric from Blade 8: Lane 1, Sense N	BLADE	HSSM
D37	TX_B8_LN1_P	4X Fabric to Blade 8: Lane 1, Sense P	HSSM	BLADE
E37	TX_B8_LN1_N	4X Fabric to Blade 8: Lane 1, Sense N	HSSM	BLADE
A38	RX_B8_LN2_P	4X Fabric from Blade 8: Lane 2, Sense P	BLADE	HSSM
B38	RX_B8_LN2_N	4X Fabric from Blade 8: Lane 2, Sense N	BLADE	HSSM
D38	TX_B8_LN2_P	4X Fabric to Blade 8: Lane 2, Sense P	HSSM	BLADE
E38	TX_B8_LN2_N	4X Fabric to Blade 8: Lane 2, Sense N	HSSM	BLADE
A39	RX_B8_LN3_P	4X Fabric from Blade 8: Lane 3, Sense P	BLADE	HSSM
B39	RX_B8_LN3_N	4X Fabric from Blade 8: Lane 3, Sense N	BLADE	HSSM
D39	TX_B8_LN3_P	4X Fabric to Blade 8: Lane 3, Sense P	HSSM	BLADE
E39	TX_B8_LN3_N	4X Fabric to Blade 8: Lane 3, Sense N	HSSM	BLADE
A40	RX_B8_LN4_P	4X Fabric from Blade 8: Lane 4, Sense P	BLADE	HSSM

B40	RX_B8_LN4_N	4X Fabric from Blade 8: Lane 4, Sense N	BLADE	HSSM
D40	TX_B8_LN4_P	4X Fabric to Blade 8: Lane 4, Sense P	HSSM	BLADE
E40	TX_B8_LN4_N	4X Fabric to Blade 8: Lane 4, Sense N	HSSM	BLADE
A41	RX_B7_LN1_P	4X Fabric from Blade 7: Lane 1, Sense P	BLADE	HSSM
B41	RX_B7_LN1_N	4X Fabric from Blade 7: Lane 1, Sense N	BLADE	HSSM
D41	TX_B7_LN1_P	4X Fabric to Blade 7: Lane 1, Sense P	HSSM	BLADE
E41	TX_B7_LN1_N	4X Fabric to Blade 7: Lane 1, Sense N	HSSM	BLADE
A42	RX_B7_LN2_P	4X Fabric from Blade 7: Lane 2, Sense P	BLADE	HSSM
B42	RX_B7_LN2_N	4X Fabric from Blade 7: Lane 2, Sense N	BLADE	HSSM
D42	TX_B7_LN2_P	4X Fabric to Blade 7: Lane 2, Sense P	HSSM	BLADE
E42	TX_B7_LN2_N	4X Fabric to Blade 7: Lane 2, Sense N	HSSM	BLADE
A43	RX_B7_LN3_P	4X Fabric from Blade 7: Lane 3, Sense P	BLADE	HSSM
B43	RX_B7_LN3_N	4X Fabric from Blade 7: Lane 3, Sense N	BLADE	HSSM
D43	TX_B7_LN3_P	4X Fabric to Blade 7: Lane 3, Sense P	HSSM	BLADE
E43	TX_B7_LN3_N	4X Fabric to Blade 7: Lane 3, Sense N	HSSM	BLADE
A44	RX_B7_LN4_P	4X Fabric from Blade 7: Lane 4, Sense P	BLADE	HSSM
B44	RX_B7_LN4_N	4X Fabric from Blade 7: Lane 4, Sense N	BLADE	HSSM
D44	TX_B7_LN4_P	4X Fabric to Blade 7: Lane 4, Sense P	HSSM	BLADE
E44	TX_B7_LN4_N	4X Fabric to Blade 7: Lane 4, Sense N	HSSM	BLADE
A45	RX_B6_LN1_P	4X Fabric from Blade 6: Lane 1, Sense P	BLADE	HSSM
B45	RX_B6_LN1_N	4X Fabric from Blade 6: Lane 1, Sense N	BLADE	HSSM
D45	TX_B6_LN1_P	4X Fabric to Blade 6: Lane 1, Sense P	HSSM	BLADE
E45	TX_B6_LN1_N	4X Fabric to Blade 6: Lane 1, Sense N	HSSM	BLADE
A46	RX_B6_LN2_P	4X Fabric from Blade 6: Lane 2, Sense P	BLADE	HSSM
B46	RX_B6_LN2_N	4X Fabric from Blade 6: Lane 2, Sense N	BLADE	HSSM
D46	TX_B6_LN2_P	4X Fabric to Blade 6: Lane 2, Sense P	HSSM	BLADE
E46	TX_B6_LN2_N	4X Fabric to Blade 6: Lane 2, Sense N	HSSM	BLADE
A47	RX_B6_LN3_P	4X Fabric from Blade 6: Lane 3, Sense P	BLADE	HSSM
B47	RX_B6_LN3_N	4X Fabric from Blade 6: Lane 3, Sense N	BLADE	HSSM
D47	TX_B6_LN3_P	4X Fabric to Blade 6: Lane 3, Sense P	HSSM	BLADE
E47	TX_B6_LN3_N	4X Fabric to Blade 6: Lane 3, Sense N	HSSM	BLADE
A48	RX_B6_LN4_P	4X Fabric from Blade 6: Lane 4, Sense P	BLADE	HSSM
B48	RX_B6_LN4_N	4X Fabric from Blade 6: Lane 4, Sense N	BLADE	HSSM
D48	TX_B6_LN4_P	4X Fabric to Blade 6: Lane 4, Sense P	HSSM	BLADE
E48	TX_B6_LN4_N	4X Fabric to Blade 6: Lane 4, Sense N	HSSM	BLADE
A49	RX_B5_LN1_P	4X Fabric from Blade 5: Lane 1, Sense P	BLADE	HSSM
B49	RX_B5_LN1_N	4X Fabric from Blade 5: Lane 1, Sense N	BLADE	HSSM
D49	TX_B5_LN1_P	4X Fabric to Blade 5: Lane 1, Sense P	HSSM	BLADE
E49	TX_B5_LN1_N	4X Fabric to Blade 5: Lane 1, Sense N	HSSM	BLADE
A50	RX_B5_LN2_P	4X Fabric from Blade 5: Lane 2, Sense P	BLADE	HSSM
B50	RX_B5_LN2_N	4X Fabric from Blade 5: Lane 2, Sense N	BLADE	HSSM
D50	TX_B5_LN2_P	4X Fabric to Blade 5: Lane 2, Sense P	HSSM	BLADE
E50	TX_B5_LN2_N	4X Fabric to Blade 5: Lane 2, Sense N	HSSM	BLADE
A51	RX_B5_LN3_P	4X Fabric from Blade 5: Lane 3, Sense P	BLADE	HSSM

B51	RX_B5_LN3_N	4X Fabric from Blade 5: Lane 3, Sense N	BLADE	HSSM
D51	TX_B5_LN3_P	4X Fabric to Blade 5: Lane 3, Sense P	HSSM	BLADE
E51	TX_B5_LN3_N	4X Fabric to Blade 5: Lane 3, Sense N	HSSM	BLADE
A52	RX_B5_LN4_P	4X Fabric from Blade 5: Lane 4, Sense P	BLADE	HSSM
B52	RX_B5_LN4_N	4X Fabric from Blade 5: Lane 4, Sense N	BLADE	HSSM
D52	TX_B5_LN4_P	4X Fabric to Blade 5: Lane 4, Sense P	HSSM	BLADE
E52	TX_B5_LN4_N	4X Fabric to Blade 5: Lane 4, Sense N	HSSM	BLADE
A53	I2C_SDA(B)	I2C Data (B)	MM & HSSM	MM & HSSM
B53	I2C_SCL(B)	I2C Clock (B)	MM & HSSM	MM & HSSM
D53	SELECT_B	Control to Enable "B" Signals and Buses	MM	HSSM
E53	PRESENT_N	High Speed Switch Module Present	HSSM	MM
A54	RX_B4_LN1_P	4X Fabric from Blade 4: Lane 1, Sense P	BLADE	HSSM
B54	RX_B4_LN1_N	4X Fabric from Blade 4: Lane 1, Sense N	BLADE	HSSM
D54	TX_B4_LN1_P	4X Fabric to Blade 4: Lane 1, Sense P	HSSM	BLADE
E54	TX_B4_LN1_N	4X Fabric to Blade 4: Lane 1, Sense N	HSSM	BLADE
A55	RX_B4_LN2_P	4X Fabric from Blade 4: Lane 2, Sense P	BLADE	HSSM
B55	RX_B4_LN2_N	4X Fabric from Blade 4: Lane 2, Sense N	BLADE	HSSM
D55	TX_B4_LN2_P	4X Fabric to Blade 4: Lane 2, Sense P	HSSM	BLADE
E55	TX_B4_LN2_N	4X Fabric to Blade 4: Lane 2, Sense N	HSSM	BLADE
A56	RX_B4_LN3_P	4X Fabric from Blade 4: Lane 3, Sense P	BLADE	HSSM
B56	RX_B4_LN3_N	4X Fabric from Blade 4: Lane 3, Sense N	BLADE	HSSM
D56	TX_B4_LN3_P	4X Fabric to Blade 4: Lane 3, Sense P	HSSM	BLADE
E56	TX_B4_LN3_N	4X Fabric to Blade 4: Lane 3, Sense N	HSSM	BLADE
A57	RX_B4_LN4_P	4X Fabric from Blade 4: Lane 4, Sense P	BLADE	HSSM
B57	RX_B4_LN4_N	4X Fabric from Blade 4: Lane 4, Sense N	BLADE	HSSM
D57	TX_B4_LN4_P	4X Fabric to Blade 4: Lane 4, Sense P	HSSM	BLADE
E57	TX_B4_LN4_N	4X Fabric to Blade 4: Lane 4, Sense N	HSSM	BLADE
A58	12V_2	12V In from Source 2		
B58	12V_2	12V In from Source 2		
D58	GND	GND		
E58	GND	GND		
A59	12V_2	12V In from Source 2		
B59	12V_2	12V In from Source 2		
D59	GND	GND		
E59	GND	GND		
A60	12V_2	12V In from Source 2		
B60	12V_2	12V In from Source 2		
D60	GND	GND		
E60	GND	GND		
A61	12V_2	12V In from Source 2		
B61	12V_2	12V In from Source 2		
D61	GND	GND		
E61	GND	GND		

A62	12V_2	12V In from Source 2		
B62	12V_2	12V In from Source 2		
D62	GND	GND		
E62	GND	GND		
A63	RX_B3_LN1_P	4X Fabric from Blade 3: Lane 1, Sense P	BLADE	HSSM
B63	RX_B3_LN1_N	4X Fabric from Blade 3: Lane 1, Sense N	BLADE	HSSM
D63	TX_B3_LN1_P	4X Fabric to Blade 3: Lane 1, Sense P	HSSM	BLADE
E63	TX_B3_LN1_N	4X Fabric to Blade 3: Lane 1, Sense N	HSSM	BLADE
A64	RX_B3_LN2_P	4X Fabric from Blade 3: Lane 2, Sense P	BLADE	HSSM
B64	RX_B3_LN2_N	4X Fabric from Blade 3: Lane 2, Sense N	BLADE	HSSM
D64	TX_B3_LN2_P	4X Fabric to Blade 3: Lane 2, Sense P	HSSM	BLADE
E64	TX_B3_LN2_N	4X Fabric to Blade 3: Lane 2, Sense N	HSSM	BLADE
A65	RX_B3_LN3_P	4X Fabric from Blade 3: Lane 3, Sense P	BLADE	HSSM
B65	RX_B3_LN3_N	4X Fabric from Blade 3: Lane 3, Sense N	BLADE	HSSM
D65	TX_B3_LN3_P	4X Fabric to Blade 3: Lane 3, Sense P	HSSM	BLADE
E65	TX_B3_LN3_N	4X Fabric to Blade 3: Lane 3, Sense N	HSSM	BLADE
A66	RX_B3_LN4_P	4X Fabric from Blade 3: Lane 4, Sense P	BLADE	HSSM
B66	RX_B3_LN4_N	4X Fabric from Blade 3: Lane 4, Sense N	BLADE	HSSM
D66	TX_B3_LN4_P	4X Fabric to Blade 3: Lane 4, Sense P	HSSM	BLADE
E66	TX_B3_LN4_N	4X Fabric to Blade 3: Lane 4, Sense N	HSSM	BLADE
A67	RX_B2_LN1_P	4X Fabric from Blade 2: Lane 1, Sense P	BLADE	HSSM
B67	RX_B2_LN1_N	4X Fabric from Blade 2: Lane 1, Sense N	BLADE	HSSM
D67	TX_B2_LN1_P	4X Fabric to Blade 2: Lane 1, Sense P	HSSM	BLADE
E67	TX_B2_LN1_N	4X Fabric to Blade 2: Lane 1, Sense N	HSSM	BLADE
A68	RX_B2_LN2_P	4X Fabric from Blade 2: Lane 2, Sense P	BLADE	HSSM
B68	RX_B2_LN2_N	4X Fabric from Blade 2: Lane 2, Sense N	BLADE	HSSM
D68	TX_B2_LN2_P	4X Fabric to Blade 2: Lane 2, Sense P	HSSM	BLADE
E68	TX_B2_LN2_N	4X Fabric to Blade 2: Lane 2, Sense N	HSSM	BLADE
A69	I2C_SDA(A)	I2C Data (A)	MM & HSSM	MM & HSSM
B69	I2C_RESET_N	I2C Reset	MM	HSSM
D69	I2C_INT_N(A)	I2C Interrupt (A)	HSSM	MM
E69	I2C_INT_N(B)	I2C Interrupt (B)	HSSM	MM
A70	I2C_SCL(A)	I2C Clock (A)	MM & HSSM	MM & HSSM
B70	Reserved	RESERVED (Interposer Presence 0)		
D70	Reserved	RESERVED (Interposer Presence 1)		
E70	Reserved	RESERVED		
A71	RX_B2_LN3_P	4X Fabric from Blade 2: Lane 3, Sense P	BLADE	HSSM
B71	RX_B2_LN3_N	4X Fabric from Blade 2: Lane 3, Sense N	BLADE	HSSM
D71	TX_B2_LN3_P	4X Fabric to Blade 2: Lane 3, Sense P	HSSM	BLADE
E71	TX_B2_LN3_N	4X Fabric to Blade 2: Lane 3, Sense N	HSSM	BLADE
A72	RX_B2_LN4_P	4X Fabric from Blade 2: Lane 4, Sense P	BLADE	HSSM
B72	RX_B2_LN4_N	4X Fabric from Blade 2: Lane 4, Sense N	BLADE	HSSM
D72	TX_B2_LN4_P	4X Fabric to Blade 2: Lane 4, Sense P	HSSM	BLADE

E72	TX_B2_LN4_N	4X Fabric to Blade 2: Lane 4, Sense N	HSSM	BLADE
A73	RX_BM3/2_LN4_P	4X Fabric from Bridge Module 3/2: Lane 4, Sense P	BM	HSSM
B73	RX_BM3/2_LN4_N	4X Fabric from Bridge Module 3/2: Lane 4, Sense N	BM	HSSM
D73	TX_BM3/2_LN1_P	4X Fabric to Bridge Module 3/2: Lane 1, Sense P	HSSM	BM
E73	TX_BM3/2_LN1_N	4X Fabric to Bridge Module 3/2: Lane 1, Sense N	HSSM	BM
A74	RX_BM3/2_LN3_P	4X Fabric from Bridge Module 3/2: Lane 3, Sense P	BM	HSSM
B74	RX_BM3/2_LN3_N	4X Fabric from Bridge Module 3/2: Lane 3, Sense N	BM	HSSM
D74	TX_BM3/2_LN2_P	4X Fabric to Bridge Module 3/2: Lane 2, Sense P	HSSM	BM
E74	TX_BM3/2_LN2_N	4X Fabric to Bridge Module 3/2: Lane 2, Sense N	HSSM	BM
A75	RX_BM3/2_LN2_P	4X Fabric from Bridge Module 3/2: Lane 2, Sense P	BM	HSSM
B75	RX_BM3/2_LN2_N	4X Fabric from Bridge Module 3/2: Lane 2, Sense N	BM	HSSM
D75	TX_BM3/2_LN3_P	4X Fabric to Bridge Module 3/2: Lane 3, Sense P	HSSM	BM
E75	TX_BM3/2_LN3_N	4X Fabric to Bridge Module 3/2: Lane 3, Sense N	HSSM	BM
A76	RX_BM3/2_LN1_P	4X Fabric from Bridge Module 3/2: Lane 1, Sense P	BM	HSSM
B76	RX_BM3/2_LN1_N	4X Fabric from Bridge Module 3/2: Lane 1, Sense N	BM	HSSM
D76	TX_BM3/2_LN4_P	4X Fabric to Bridge Module 3/2: Lane 4, Sense P	HSSM	BM
E76	TX_BM3/2_LN4_N	4X Fabric to Bridge Module 3/2: Lane 4, Sense N	HSSM	BM
A77	RX_B1_LN1_P	4X Fabric from Blade 1: Lane 1, Sense P	BLADE	HSSM
B77	RX_B1_LN1_N	4X Fabric from Blade 1: Lane 1, Sense N	BLADE	HSSM
D77	TX_B1_LN1_P	4X Fabric to Blade 1: Lane 1, Sense P	HSSM	BLADE
E77	TX_B1_LN1_N	4X Fabric to Blade 1: Lane 1, Sense N	HSSM	BLADE
A78	RX_B1_LN2_P	4X Fabric from Blade 1: Lane 2, Sense P	BLADE	HSSM
B78	RX_B1_LN2_N	4X Fabric from Blade 1: Lane 2, Sense N	BLADE	HSSM
D78	TX_B1_LN2_P	4X Fabric to Blade 1: Lane 2, Sense P	HSSM	BLADE
E78	TX_B1_LN2_N	4X Fabric to Blade 1: Lane 2, Sense N	HSSM	BLADE
A79	RX_B1_LN3_P	4X Fabric from Blade 1: Lane 3, Sense P	BLADE	HSSM
B79	RX_B1_LN3_N	4X Fabric from Blade 1: Lane 3, Sense N	BLADE	HSSM
D79	TX_B1_LN3_P	4X Fabric to Blade 1: Lane 3, Sense P	HSSM	BLADE
E79	TX_B1_LN3_N	4X Fabric to Blade 1: Lane 3, Sense N	HSSM	BLADE
A80	RX_B1_LN4_P	4X Fabric from Blade 1: Lane 4, Sense P	BLADE	HSSM
B80	RX_B1_LN4_N	4X Fabric from Blade 1: Lane 4, Sense N	BLADE	HSSM
D80	TX_B1_LN4_P	4X Fabric to Blade 1: Lane 4, Sense P	HSSM	BLADE
E80	TX_B1_LN4_N	4X Fabric to Blade 1: Lane 4, Sense N	HSSM	BLADE

Description	From	Pin	To	Pin
Link 1: HSSM 7 - HSSM 9				
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 1, Sense P	SM 9	D5	SM 7	A5
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 1, Sense N	SM 9	E5	SM 7	B5
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 1, Sense P	SM 7	D5	SM 9	A5
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 1, Sense N	SM 7	E5	SM 9	B5
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 2, Sense P	SM 9	D6	SM 7	A6
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 2, Sense N	SM 9	E6	SM 7	B6
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 2, Sense P	SM 7	D6	SM 9	A6
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 2, Sense N	SM 7	E6	SM 9	B6

4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 3, Sense P	SM 9	D7	SM 7	A7
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 3, Sense N	SM 9	E7	SM 7	B7
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 3, Sense P	SM 7	D7	SM 9	A7
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 3, Sense N	SM 7	E7	SM 9	B7
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 4, Sense P	SM 9	B8	SM 7	A8
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 4, Sense N	SM 9	E8	SM 7	B8
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 4, Sense P	SM 7	B8	SM 9	A8
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 4, Sense N	SM 7	E8	SM 9	B8
Link 2: HSSM 7 - HSSM 9 (HSSM 7 - HSSM 9)				
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 1, Sense P	SM 9	D25	SM 7	A25
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 1, Sense N	SM 9	E25	SM 7	B25
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 1, Sense P	SM 7	D25	SM 9	A25
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 1, Sense N	SM 7	E25	SM 9	B25
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 2, Sense P	SM 9	D26	SM 7	A26
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 2, Sense N	SM 9	E26	SM 7	B26
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 2, Sense P	SM 7	D26	SM 9	A26
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 2, Sense N	SM 7	E26	SM 9	B26
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 3, Sense P	SM 9	D27	SM 7	A27
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 3, Sense N	SM 9	E27	SM 7	B27
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 3, Sense P	SM 7	D27	SM 9	A27
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 3, Sense N	SM 7	E27	SM 9	B27
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 4, Sense P	SM 9	B28	SM 7	A28
4X Fabric LINK 1 HSSM 9 to HSSM 7: Lane 4, Sense N	SM 9	E28	SM 7	B28
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 4, Sense P	SM 7	B28	SM 9	A28
4X Fabric LINK 1 HSSM 7 to HSSM 9: Lane 4, Sense N	SM 7	E28	SM 9	B28
Link 1: HSSM 8 - HSSM 10				
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 1, Sense P	SM 10	D5	SM 8	A5
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 1, Sense N	SM 10	E5	SM 8	B5
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 1, Sense P	SM 8	D5	SM 10	A5
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 1, Sense N	SM 8	E5	SM 10	B5
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 2, Sense P	SM 10	D6	SM 8	A6
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 2, Sense N	SM 10	E6	SM 8	B6
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 2, Sense P	SM 8	D6	SM 10	A6
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 2, Sense N	SM 8	E6	SM 10	B6
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 3, Sense P	SM 10	D7	SM 8	A7
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 3, Sense N	SM 10	E7	SM 8	B7
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 3, Sense P	SM 8	D7	SM 10	A7
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 3, Sense N	SM 8	E7	SM 10	B7
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 4, Sense P	SM 10	B8	SM 8	A8
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 4, Sense N	SM 10	E8	SM 8	B8
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 4, Sense P	SM 8	B8	SM 10	A8
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 4, Sense N	SM 8	E8	SM 10	B8
Link 2: HSSM 8 - HSSM 10				
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 1, Sense P	SM 10	D25	SM 8	A25
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 1, Sense N	SM 10	E25	SM 8	B25

4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 1, Sense P	SM 8	D25	SM 10	A25
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 1, Sense N	SM 8	E25	SM 10	B25
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 2, Sense P	SM 10	D26	SM 8	A26
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 2, Sense N	SM 10	E26	SM 8	B26
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 2, Sense P	SM 8	D26	SM 10	A26
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 2, Sense N	SM 8	E26	SM 10	B26
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 3, Sense P	SM 10	D27	SM 8	A27
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 3, Sense N	SM 10	E27	SM 8	B27
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 3, Sense P	SM 8	D27	SM 10	A27
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 3, Sense N	SM 8	E27	SM 10	B27
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 4, Sense P	SM 10	B28	SM 8	A28
4X Fabric LINK 1 HSSM 10 to HSSM 8: Lane 4, Sense N	SM 10	E28	SM 8	B28
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 4, Sense P	SM 8	B28	SM 10	A28
4X Fabric LINK 1 HSSM 8 to HSSM 10: Lane 4, Sense N	SM 8	E28	SM 10	B28

Table 7-11 High Speed Switch Module Connectors Pin Definitions (12-blade 4X chassis)

HSSM Pin Table Notes:

1. "Transformerless" Ethernet connection (pins A9, B9, D9, E9, A10, B10, D10, E10). See section 7.1.3 for additional details.
2. Three mid-plane inputs to the HSSM (pins A24, B24, D24) used to determine the low order nibble of the switch default IP address. The HSSM MUST provide voltage pull-ups. Low signal levels are provided by 100 ohm pull-downs to ground on the mid-plane, high levels not provided by the mid-plane.
3. 5V pull-up provided on mid-plane for Select_A/B (pins E24, D53), switch must not use pullup resistor. 50 ohms +/-10% impedance.
4. 100 Khz I^2C serial data lines (pins A69, A53). 5V pull-up on mid-plane, switch must not use pullup resistor. 50 ohms +/-10% impedance. Signals multiplexed on the switch , refer to I^2C section of this document for additional details.
5. 100 Khz I^2C serial clock lines (pins A70, B53). 5V pull-up on mid-plane, switch must not use pullup resistor. 50 ohms +/-10% impedance. Signals multiplexed on the switch , refer to I^2C section of this document for additional details.
6. 5V 4.7K pull-up provided on mid-plane for Present_N (pin E53). HSSM grounds through 100 ohm resistor to indicate presence to Management Modules.
7. 5V pull-up provided on mid-plane for I2C Reset_N (pin B69), switch must not use pullup resistor. 50 ohms +/-10% impedance. Shared line that when asserted by either MM forces the HSSM to clear its I2C bus protocol unit (de-asserts all SDA and SCL lines). Active Low.
8. 5V pull-up provided on mid-plane for I2C_Int_N (A/B) (pins D69, E69), switch must not use pullup resistor. 50 ohms +/-10% impedance. Active low signals. HSSM provides open collector.
9. When using the HSSM to bridge module lanes, wiring should begin with the logical lowest lane 1. Up to four lanes are available for connectivity between the HSSM and bridge modules.

7.2 Switch Firmware requirements

The switch firmware must perform the following functions to accommodate the transposition:

1. Detect the chassis type in which the switch is installed (14-blade vs. 12-blade) upon power-up. No rebooting or power cycling of the switch must be required to perform the subsequent tasks.

2. Perform the switch-blade port mapping as described in the previous tables via firmware abstraction and adjust the user interface to show the correct blade server mapped to the respective switch port, with blades displayed in ascending order left to right. That is, in the 12-blade 4X chassis display, only twelve (12) blades should be displayed.
3. In the 12-blade chassis, display the status of the inter-switch links separately from the blade server links.
4. Perform the switch-bridge module port mapping as described in the previous tables via firmware abstraction and adjust the user interface to show the actual bridge module chassis bay location. The actual bridge module bay location is different based on chassis type, refer to table 7-17 for the correct bridge module bay numbering to display.

7.3 Bridge Module

7.3.1 Bridge Module Connector Description

The Bridge Module mechanical enclosure is based on a single wide, single high module. It uses a VHDM and a 54 position mezzanine signal connector to interface to the midplane.
Part numbers are shown below in Table below for the assemblies.

Bridge Module and Midplane connectors

Connector Description	Source A		Source B		Note
	Vendor	Part Number	Vendor	Part Number	
VHDM Connector Assembly	Molex	74030-9857	--	--	Part of Bridge Module
Mating VHDM Connector on Midplane	Molex	74074-9987	Amphenol	498-5010-022	Part of midplane
Power Connector	Molex	74030-9860	Amphenol	AC601-00017	Part of Bridge Module
Mating Power Connector on Midplane	Molex	74029-6998	Amphenol	437-6050-000	Part of midplane
Mezzanine Card Conn., 54 pos. Rt. Angle Header (Midplane Connector)	FCI	10039851-101LF	Amphenol	AA230-06100	Part of Bridge Module
Mating Conn. For Mezzanine Card Conn.	FCI	10043546-101LF	Amphenol	AA130-06000	Part of midplane
Note: Refer to *BladeServer_Connectors_20090506.pdf* located on the Blade Open Spec Support Center website (**http://www-03.ibm.com/systems/bladecenter/open_specs.html)** for most up to date connector list.					

Pin numbering and orientation for the Bridge Module connectors is from the perspective of looking through the mid-plane toward the Bridge Module bay and is shown in the figures below.

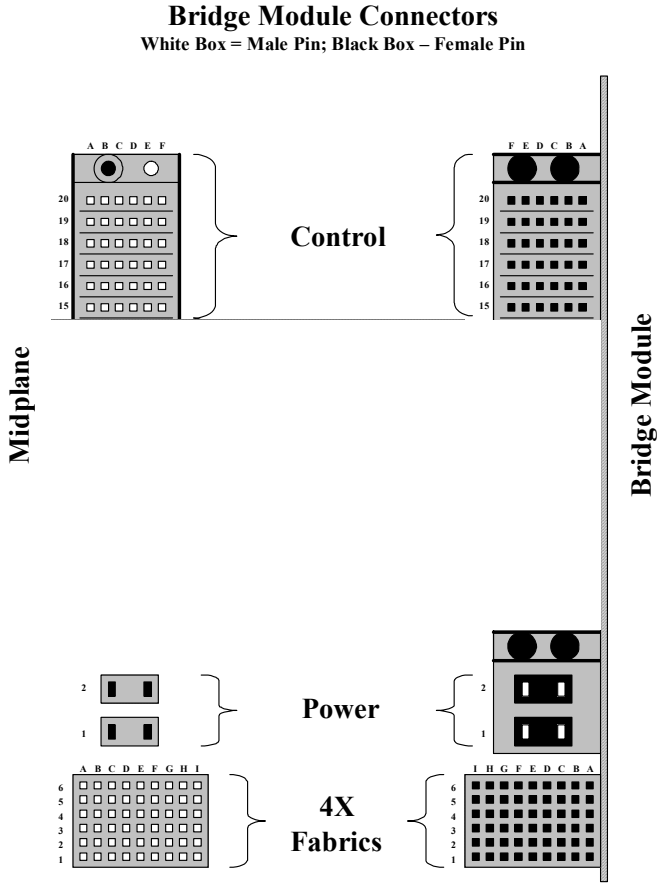


Figure 7-4 - Bridge Module to Midplane Connector

***NOTE: There are no guide pins in the bridge slots of BladeCenter H. The bridge module must still provide a mating guide pin block or sufficient clearance for guide pins in the shared slots.**

7.3.2 Bridge Module Ethernet Connection to Management Module

Ethernet connection to the Management Module is the same as for the 1XSM. Reference section 7.1.3.

7.3.3 Bridge Module pin assignment and signal description

The following table describes the mid-plane connector pin assignments and signal pin information for the bridge module

Pin	Name	Direction	Description	Transmitter	Receiver
A15	RX_MM1_N	in	Mgmt Fabric from Management Module 1: Sense N	MM	BM
B15	RX_MM1_P	in	Mgmt Fabric from Management Module 1: Sense P	MM	BM
C15	GND		GND		
D15	TX_MM1_N	out	Mgmt Fabric to Management Module 1: Sense N	BM	MM
E15	TX_MM1_P	out	Mgmt Fabric to Management Module 1: Sense P	BM	MM
F15	GND		GND		
A16	GND		GND		
B16	RX_MM2_N	in	Mgmt Fabric from Management Module 2: Sense N	MM	BM
C16	RX_MM2_P	in	Mgmt Fabric from Management Module 2: Sense P	MM	BM
D16	GND		GND		
E16	TX_MM2_N	out	Mgmt Fabric to Management Module 2: Sense N	BM	MM
F16	TX_MM2_P	out	Mgmt Fabric to Management Module 2: Sense P	BM	MM
A17	I2C_SDA(A)	i/o	I2C Data (A)	MM & BM	MM & BM
B17	I2C_SCL(A)	i/o	I2C Clock (A)	MM & BM	MM & BM
C17	I2C_INT_N(A)	out	I2C Interrupt (A)	BM	MM
D17	I2C_SDA(B)	i/o	I2C Data (B)	MM & BM	MM & BM
E17	I2C_SCL(B)	i/o	I2C Clock (B)	MM & BM	MM & BM
F17	I2C_INT_N(B)	out	I2C Interrupt (B)	BM	MM
A18	SELECT_A	in	Control to Enable "A" Signals and Buses	MM	BM
B18	SELECT_B	in	Control to Enable "B" Signals and Buses	MM	BM
C18	I2C_RESET_N	in	I2C Reset	MM	BM
D18	BAY_ID_BIT0	in	Switch Bay ID, Least Significant Bit	chassis	BM
E18	BAY_ID_BIT1	in	Switch Bay ID, Middle Significant Bit	chassis	BM
F18	BAY_ID_BIT2	in	Switch Bay ID, Most Significant Bit	chassis	BM
A19	PRESENT_N	out	Bridge Module Present	BM	MM
B19	GND		GND		
C19	GND		GND		
D19	GND		GND		
E19	GND		GND		
F19	N/C		N/C		
A20	N/C		N/C		
B20	N/C		N/C		
C20	N/C		N/C		
D20	N/C		N/C		
E20	N/C		N/C		
F20	N/C		N/C		

Table 7-12: Bridge Module Control Pin Definitions

Pin	Name	Direction	Description
A1	GND		GND
B1	12V_2	in	12V In from Source 2
A2	GND		GND
B2	12V_1	in	12V In from Source 1

Table 7-13: Bridge Module Power Pin Definitions

Pin	Name	Direction	Description	Transmitter	Receiver
A1	RX_HSSM2/4_LN4_P	in	4X Fabric from High Speed Switch Module 2/4: Lane 4, Sense P	HSSM	BM
B1	RX_HSSM2/4_LN4_N	in	4X Fabric from High Speed Switch Module 2/4: Lane 4, Sense N	HSSM	BM
C1	GND		GND		
D1	N/C		N/C		
E1	N/C		N/C		
F1	GND		GND		
G1	RX_HSSM2/4_LN1_P	in	4X Fabric from High Speed Switch Module 2/4: Lane 1, Sense P	HSSM	BM
H1	RX_HSSM2/4_LN1_N	in	4X Fabric from High Speed Switch Module 2/4: Lane 1, Sense N	HSSM	BM
I1	GND		GND		
A2	GND		GND		
B2	RX_HSSM2/4_LN3_P	in	4X Fabric from High Speed Switch Module 2/4: Lane 3, Sense P	HSSM	BM
C2	RX_HSSM2/4_LN3_N	in	4X Fabric from High Speed Switch Module 2/4: Lane 3, Sense N	HSSM	BM
D2	GND		GND		
E2	RX_HSSM2/4_LN2_P	in	4X Fabric from High Speed Switch Module 2/4: Lane 2, Sense P	HSSM	BM
F2	RX_HSSM2/4_LN2_N	in	4X Fabric from High Speed Switch Module 2/4: Lane 2, Sense N	HSSM	BM
G2	GND		GND		
H2	RX_HSSM1/3_LN1_P	in	4X Fabric from High Speed Switch Module 1/3: Lane 1, Sense P	HSSM	BM
I2	RX_HSSM1/3_LN1_N	in	4X Fabric from High Speed Switch Module 1/3: Lane 1, Sense N	HSSM	BM
A3	TX_HSSM1/3_LN1_P	out	4X Fabric to High Speed Switch Module 1/3: Lane 1, Sense P	BM	HSSM
B3	TX_HSSM1/3_LN1_N	out	4X Fabric to High Speed Switch Module 1/3: Lane 1, Sense N	BM	HSSM
C3	GND		GND		
D3	TX_HSSM2/4_LN1_P	out	4X Fabric to High Speed Switch Module 2/4: Lane 1, Sense P	BM	HSSM
E3	TX_HSSM2/4_LN1_N	out	4X Fabric to High Speed Switch Module 2/4: Lane 1, Sense N	BM	HSSM
F3	GND		GND		
G3	RX_HSSM1/3_LN2_P	in	4X Fabric from High Speed Switch Module 1/3: Lane 2, Sense P	HSSM	BM

H3	RX_HSSM1/3_LN2_N	in	4X Fabric from High Speed Switch Module 1/3: Lane 2, Sense N	HSSM	BM
I3	GND		GND		
A4	GND		GND		
B4	TX_HSSM1/3_LN2_P	out	4X Fabric to High Speed Switch Module 1/3: Lane 2, Sense P	BM	HSSM
C4	TX_HSSM1/3_LN2_N	out	4X Fabric to High Speed Switch Module 1/3: Lane 2, Sense N	BM	HSSM
D4	GND		GND		
E4	TX_HSSM2/4_LN2_P	out	4X Fabric to High Speed Switch Module 2/4: Lane 2, Sense P	BM	HSSM
F4	TX_HSSM2/4_LN2_N	out	4X Fabric to High Speed Switch Module 2/4: Lane 2, Sense N	BM	HSSM
G4	GND		GND		
H4	RX_HSSM1/3_LN3_P	in	4X Fabric from High Speed Switch Module 1/3: Lane 3, Sense P	HSSM	BM
I4	RX_HSSM1/3_LN3_N	in	4X Fabric from High Speed Switch Module 1/3: Lane 3, Sense N	HSSM	BM
A5	TX_HSSM1/3_LN3_P	out	4X Fabric to High Speed Switch Module 1/3: Lane 3, Sense P	BM	HSSM
B5	TX_HSSM1/3_LN3_N	out	4X Fabric to High Speed Switch Module 1/3: Lane 3, Sense N	BM	HSSM
C5	GND		GND		
D5	TX_HSSM2/4_LN3_P	out	4X Fabric to High Speed Switch Module 2/4: Lane 3, Sense P	BM	HSSM
E5	TX_HSSM2/4_LN3_N	out	4X Fabric to High Speed Switch Module 2/4: Lane 3, Sense N	BM	HSSM
F5	GND		GND		
G5	RX_HSSM1/3_LN4_P	in	4X Fabric from High Speed Switch Module 1/3: Lane 4, Sense P	HSSM	BM
H5	RX_HSSM1/3_LN4_N	in	4X Fabric from High Speed Switch Module 1/3: Lane 4, Sense N	HSSM	BM
I5	GND		GND		
A6	GND		GND		
B6	TX_HSSM1/3_LN4_P	out	4X Fabric to High Speed Switch Module 1/3: Lane 4, Sense P	BM	HSSM
C6	TX_HSSM1/3_LN4_N	out	4X Fabric to High Speed Switch Module 1/3: Lane 4, Sense N	BM	HSSM
D6	GND		GND		
E6	N/C		N/C		
F6	N/C		N/C		
G6	GND		GND		
H6	TX_HSSM2/4_LN4_P	out	4X Fabric to High Speed Switch Module 2/4: Lane 4, Sense P	BM	HSSM
I6	TX_HSSM2/4_LN4_N	out	4X Fabric to High Speed Switch Module 2/4: Lane 4, Sense N	BM	HSSM

Table 7-14: Bridge Module Connector to 4x High Speed Switches - Pin Definitions

8 I²C Interface Architecture

8.1 Overview

An I²C interface is used by the management Module(s) to internally provide control of the Switch Module and to collect system status and VPD information. The following control and data areas are accessible by the Management Module I²C:

- Vital Product Data EEPROM (VPD)
- Control Register
- Extended Control Register
- Status Register and Extended Status Register
- Diagnostic Register

The I²C resources, control, status and diagnostic registers and the VPD EEPROM are implemented as a single set of resources and are accessible by either I²C Bus A or I²C Bus B, depending upon the state of the signals MM_SELECT_A and MM_SELECT_B (see Table 8-1). Note that the '00'b and '11'b state of MM_SELECT_A and MM_SELECT_B should be considered invalid and, if the condition occurs during an I²C bus transaction, that transaction should be immediately aborted. It will be the responsibility of the management Module to reset the I²C bus and protocol engines (I²C Bus Reset). See Figure 8-1 for a high-level perspective of the I²C resources.

MM_SELECT_A Status	MM_SELECT_B Status	Active I²C Interface
0	0	Degate Bus
1	0	Bus A Active
0	1	Bus B Active
1	1	Degate Bus

Table 8-1 - I²C Interface Control

Notes: 0= 0 V signal; In the 4X chassis, control signals are named SELECT_A, and SELECT_B

The Switch I²C interface is a standard protocol[1], except for the I²C Bus Reset signal and I²C Interrupt Signal. The I²C Bus Reset signal is used to reset the Switch Module's I²C bus interface and protocol states. Refer to the I²C Status Register description for operation of the I²C Interrupt signal. The I²C bus currently operates at 100KHz. Based on the Switch bay and Switch Bay ID described earlier, the read and write addresses for the VPD and registers are given in Table 8-2.

The midplane I²C Bus supports 5 volt signal levels only. Normally, this requires voltage level translation circuitry (LTC4300A-3) to interface to the internal SM I²C bus.

[1] I²C is a two-wire communications bus/protocol developed by Philips (Koninklijke Philips Electronics N.V.). SMBus is a subset of the I²C bus/protocol and was developed by Intel. Implementations of the I²C bus/protocol or the SMBus bus/protocol may require licenses from various entities, including Koninklijke Philips Electronics N.V. and North American Philips Corporation. See www.philips.com/buses/i2c

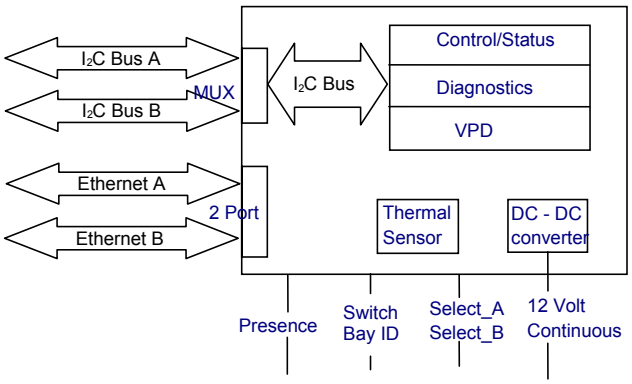


Figure 8-1 - Switch Module I²C Structure

Note: The two Ethernet ports that connect to the Management Module are intended to represent one logical port (one IP address) as opposed to two physical ports or NICs.

Switch Bay Position	Switch Bay ID	VPD I²C Address Read (Note 1)	VPD I²C Address Write (Note 1)	Register I²C Address Read (Note 1)	Register I²C Address Write (Note 1)
1	X'1'	X'A3'	X'A2'	X'B3'	X'B2'
2	X'2'	X'A5'	X'A4'	X'B5'	X'B4'
3	X'4'	X'A9'	X'A8'	X'B9'	X'B8'
4	X'7'	X'AF'	X'AE'	X'BF'	X'BE'
5	X'5'	X'AB'	X'AA'	X'BB'	X'BA'
6	X'6'	X'AD'	X'AC'	X'BD'	X'BC'
Note 1: I²C address conforms to x24C32 PROM for VPD, custom logic address for register implementation. All other addresses are reserved					

Table 8-2 - Switch Module I²C Addresses

Switch Bay Position	**Switch Bay ID**	**VPD I²C Address Read (Note 1)**	**VPD I²C Address Write (Note 1)**	**Register I²C Address Read (Note 1)**	**Register I²C Address Write (Note 1)**
7	X'0'	X'A1'	X'A0'	X'B1'	X'B0'
8	X'2'	X'A1'	X'A0'	X'B1'	X'B0'
9	X'1'	X'A1'	X'A0'	X'B1'	X'B0'
10	X'3'	X'A1'	X'A0'	X'B1'	X'B0'
Note 1: I²C address conforms to x24C32 PROM for VPD, custom logic address for register implementation. All other addresses are reserved.					

Table 8-3 – HSSM I2C Addresses

Because there are multiple registers (Control, Status, Diagnostic, Extended Control, Temperature) the Read and Write I²C addresses in Table 8-2 require an address offset shown in Table 8-4. The offset is passed in the next I²C data byte after the switch address byte. If data is to be written to that register, it should be in the data byte that follows the offset byte. Reserved registers and reserved or unspecified bit positions should return a zero on a Read.

Register	Address Offset
Control Register	X'00'
Status Register	X'01'
Diagnostic Register	X'02'
Reserved	X'03' – X'07'
Extended Control Register	X'08'
Extended Status Register	X'09'
Temp Register 1	X'0A'
Temp Register 2	X'0B'
Reserved	X'0C' – X'FF'

Table 8-4 - Register address offsets

In order to determine its bay, the Switch Module will read the Switch Bay ID using 3 signal pins provided by the mid-plane (see Table 8-5 for values). In order to ensure a unique Switch Management IP address is assigned to each Switch Module, the Switch bay number must be used as the least significant three bits of the default Switch Management IP address recorded in the Switch Module VPD. The Switch Module must use the 3 bit Switch Bay ID as it is provided, without any modification. Table 8-5 indicates the values used by the current chassis types. Different, or additional values may be used in other chassis implementations.Switch Bay ID

Switch Bay	1X Switch Bay ID (F18 E18 D18)	4X Switch Bay ID (D24 B24 A24)
Bay 1	001	
Bay 2	010	
Bay 3	100	
Bay 4	111	
Bay 5	101	
Bay 6	110	
Bay 7		000
Bay 8		010
Bay 9		001
Bay 10		011
Note: 0= 0V signal		

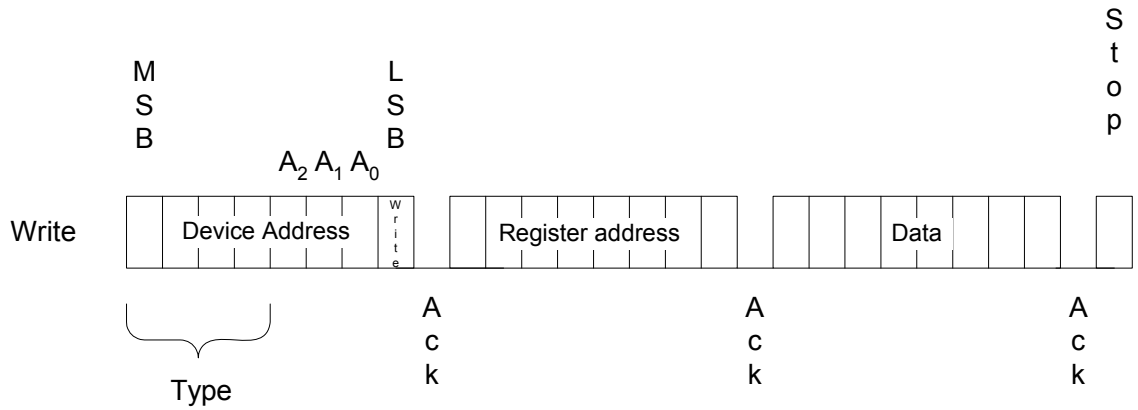
Table 8-5 - BladeServer Switch Switch Bay ID

8.1.1 I^2C Bus Transactions

The following description is provided as background only, as a reference for I^2C transactions from the management module to the I/O modules. Please see the URL in footnote 1 for official information. These I^2C transactions support "random" writes and reads to the device's I^2C address space. In this example, a single byte address is assumed as defined for the I/O modules, e.g. the status register, the control register, etc. Other I^2C attached devices, such as the VPD EEPROM AT24C64 or M24C64, will require two bytes of addressing.. Also, other devices may support sequential reads and page writes. This section does not describe that protocol. The designer must read the appropriate specification.

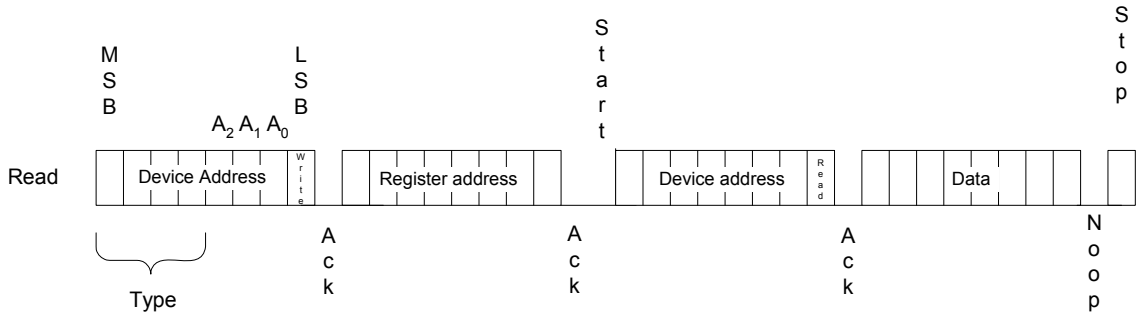
8.1.1.1 Write

The write operation begins with the device address sent serially to the device. There is a four-bit device address field followed by a three-bit address and then the read/write bit. The four-bit address field is common for a class of devices, e.g. a device address of "A" defines serial EEPROMS. The three-bit address selects which one of a multiple similar devices is selected. The write bit denotes the write operation. Inside any device are a number of locations to be written. These can be registers or memory locations in the case of EEPROMs. In our example, a register address is defined. Once the register address has been sent, the data is sent to the device. The device responds to the ACK during each transfer to indicate completion of the byte transfer. The master then indicates completion of the sequence with the STOP sequence.



8.1.1.2 Read

The read operation is a two step process. The first operation is a dummy write operation to set-up the register for a read. This ending of the write operation is indicated by the START sequence. So the first operation sets up the register and the second operation actually performs the read. A NOOP and STOP sequence indicate the end of the read operation.



8.1.1.3 Writing to a Read-only register

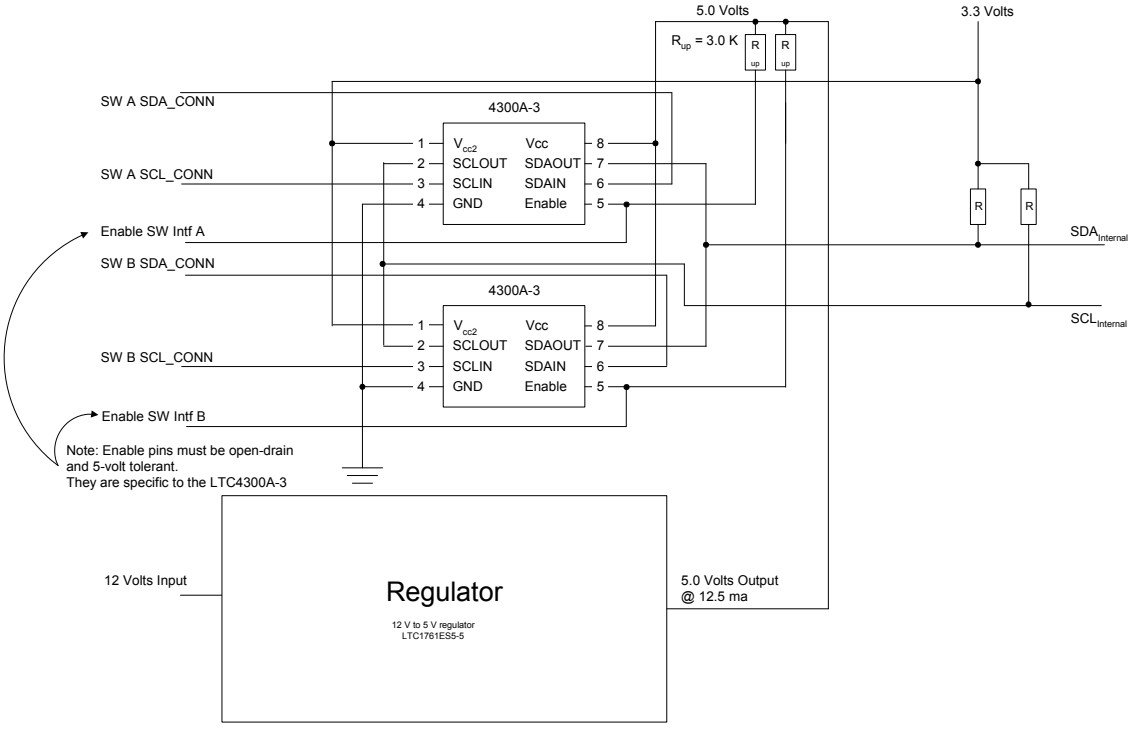
The addresses of both the write and read registers as defined in the BladeServer architecture are separate. There is no way to perform a write operation to a read-only register. If this occurs, the device does not return ACK to the last transfer and the I^2C bus times-out. It is the responsibility of the I^2C master to recover from this condition (in this case the Management Module).

8.1.1.4 Reading from a Write-only register

Since both the write and read address are different, a read from a write-only register results in the device not returning ACK to the transfer. Again, it is the responsibility of the I^2C master to recover from this condition.

Implementation Note:
Current Management Module firmware design does not support multi-master I^2C operation and the Management Module will always attempt to control the I^2C bus as sole master. The Switch Module I^2C design must be able to disconnect from the Management Module interface when it is necessary for the Switch Module to be the I^2C bus master on its local bus (e.g. when the Switch needs to write to its VPD). The maximum amount of time that the Switch Module can disconnect from the Management Module backplane I^2C bus is 250 ms. It is expected that when the Switch Module disconnects from the backplane I^2C bus, it will be an infrequent event so as not to limit Management Module access to the Switch Module's VPD and I^2C register space.

8.2 Reference I^2C Electrical Design



Note: The enable signals must be open drain to allow the external resistors to pull the signal up to 5 volts. This is because the requirement for the LTC4300A for the least positive up level is 4.72 volts in order to ensure that the Enable signal on pin 5 is active.

The enable signals are not wired directly to MM_SELECT_A and MM_SELECT_B.
The enable signals should connect to the outputs of the internal switch signal processor.
The MM_SELECT signals should connect as inputs to the processor.

8.3 I²C VPD Specification

The VPD architecture has three different data type areas:

- Fixed Block Manufacturing Data Area
- Dynamic Block Controller Area - Written by Switch controller
- Dynamic Block System Management Area -Written by System Management Module

The Switch Module must therefore be able to read/write the VPD space during operation and must be able to share/synchronize VPD operations with Management Module accesses.

8.3.1 I²C Bus Definitions for VPD Address Space

- **Current Address Read:** A current address read operation will occur when a read access is directed to a device address without specifying a byte/word address in an immediately previous write operation. The data byte/word returned will be the contents of the last byte/word address accessed by a previous read or write operation, incremented by one.
- **Random Access Read:** Random access read operations will be initiated with a write operation to the device address with a data byte containing the address of the byte/word to be accessed. A subsequent read to the same device address shall result in the corresponding data being returned.
- **Sequential Read Access:** Sequential read operations will occur as a result of either a current address read or a random access read. Sequential data bytes/words will continue to be returned in response to acknowledges and will terminate when a stop condition is encountered.
- **Byte Write Access:** Byte write operations occur when a write access is directed to a device address with a data byte containing the address of the byte/word to be accessed. A subsequent data transfer will result in the data being stored at the previously specified byte/word address. The transfer will terminate on a stop condition.
- **Page Write Access:** Page write operations will be initiated in the same manner as a byte write operation. Up to eight data bytes/words can be transferred during a page write operation. The transfer will terminate on a stop condition.
- **Data Wrap:** Data wrap or roll over will occur on the next access after the last byte/word in the resource has been accessed. For VPD access, this will be the page boundary.
- **Write Protection:** No write protection for the VPD address space.

8.3.2 I²C Bus Operations for VPD Address Space

VPD can be accessed on byte or word boundaries. Three VPD read mode operations will be supported; current address read, random access read and sequential access read. Two types of VPD write mode operations will be supported: byte write access and page write access.

NOTE: The current architected VPD content size requires a minimum of a **64Kb** (8KB) I²C EEPROM. The MM can support an I²C EEPROM up to a maximum size of 512Kb (64KB). The appropriate I²C EEPROM that meets the current architected VPD space requirement and the addressing requirement of the Switch's I²C space is the 24C64 family part. This part requires double byte offset addressing. This interface supports EEPROMs such as Atmel's AT24C64 and STMicro's M24C64 or equivalent family of parts.

NOTE: VPD data byte ordering is MSB (big endian).

8.3.3 I²C VPD Operational Latency

The worst-case latency between I²C VPD value change and completion of intended firmware operation/status indication should be less than 0.5 seconds. This latency is specified from the time any

control register bit is set to the completion of the operation indicated by the associated bit in any status register.

For example, if a user wants to change an IP address, the address is written into the appropriate VPD area. A bit in the control register is then set to indicate an IP address change. Within 0.5 seconds, the status register must be updated to indicate completion of the operation.

8.3.4 VPD Tables

Each subsystem must include Vital Product Data (VPD) information that is accessed by the Chassis Management Module. VPD Data is defined in the document *BladeServer Base Specification for VPD*.

8.4 I²C Register Specification

8.4.1 I²C Bus Operations for Register Address Space

I²C bus operations for register access (Diagnostic, Status and Control) will be on byte boundaries. Read mode operations for register access will be random access read only and write mode operation will be byte write access.

- **Random Access Read:** Random access read operations will be initiated with a write operation to the device address with a data byte containing the address of the byte/word to be accessed. A subsequent read to the same device address shall result in the corresponding data being returned.
- **Byte Write Access:** Byte write operations occur when a write access is directed to a device address with a data byte containing the address of the byte/word to be accessed. A subsequent data transfer will result in the data being stored at the previously specified byte/word address. The transfer will terminate on a stop condition.
- **Write Protection:** The Diagnostic and Status registers will be protected from external writes to avoid corruption.

8.4.2 I²C Register Operational Latency

The worst case latency between I²C register change and completion of intended firmware operation/status indication should be less than 0.5 seconds. This latency is specified from the time a control register bit is set to the completion of the operation indicated by the associated bit in a status register. It is not intended to specify the latency with regards to the operation of the particular bit in the register. For example: In the case of Extended Control Register bit 2, ECR(2) 0 -> 1 transition (IP configuration change), the associated results of the change must be reflected in the designated VPD fields in less than .5 Sec. Another example would be power-on/off or reset: CR(0) transitions (0 - >1 = power on; or 1 ->0 = power off; or 1 ->0 ->1 = reset) in which case the operation must complete in less than .5 Sec. Where the operation involves powering up, completion is determined as a result of Status Register bit 6, SR(6) being set to 0 (this bit would normally be at a 1 state as a result of diagnostics having completed and would be set to a 0 state upon entering diagnostics).

8.5 I²C Register Descriptions

The following I2C register definitions are required to be supported in order for the MM to be able to control and collect status information from the SM. The Control Register (CR) and the Extended Control Register (ECR) allow the MM to signal the SM to perform a requested action. The Status Register (SR), the Extended Status Register (ESR) and the Diagnostic Register (DR) allow the SM to signal the MM that a condition has occurred that the MM must handle. Included in the CR and ECR tables are the default values that the MM will write to these registers when the MM is in a "default"

configuration. The values written by the MM to these registers may be other than the defaults, depending on the user configuration of the MM. Also, note that some CR and ECR bit settings must be used in combination to provide the requested action. These combinations are noted in the tables.

8.5.1 Control Register

A Control Register is accessible on the I^2C interface that is R/W from the system side (MM) and R/O from the Switch side. The format of the register is shown in Table 8-6.

7	6	5	4	3	2	1	0

Bit 7: A "1" in this position indicates bit 7 of the Status Register should be set ("1").
A "0" in this position indicates bit 7 of the Status Register should be reset ("0").
Default value is "0".

Bit 6: A "1" in this position indicates the initial Switch configuration should revert back to the default factory values. This bit will only be set in conjunction with CR(0).
Default value is "0".

Bit 5: A "1" in this position indicates that extended (memory) diagnostics should be bypassed. This bit is ignored by new Switches implemented after 11/2002.
Default value is "0".

Bit 4: A "0" in this position indicates all external Switch Module ports are disabled.
A "1" in this position indicates all external Switch Module ports are enabled.
Default value is "0".

Bit 3: A "0" in this position indicates that the Switch Module can be managed and configured only from the Switch Module's active MM port
A "1" in this position indicates that the Switch Module can be managed and configured through the Switch Module's MM, external and internal ports.
Default value is "0".

Bit 2: A "0" to "1" transition in this position will reset Switch MM ENET port 1.
The Management Module should reset this bit to "0".
Default value is "0".

Bit 1: A "0" to "1" transition in this position will reset Switch MM ENET port 0.
The Management Module should reset this bit to "0".
Default value is "0".

Bit 0: A "1" in this position will power on the Switch Module.
A "0" will power off the Module.
A "1" to "0" to "1" transition provides a reset mechanism for the Switch Module.
Note: Min time in each state is 500ms, max time is not limited.
Default value is "0".

Table 8-6 - I^2C Control Register

Note: See section 13 on 'Switch Module Protect Mode and Switch Stacking Architecture' for additional behavior in regards to these Control Register bits.

8.5.2 Extended Control Register

The Extended Control Register is accessible on the I^2C interface that is R/W from the system side (MM) and R/O from the Switch side. The format of the register is shown in Table 8-7.

7	6	5	4	3	2	1	0

Bit 7: Reserved
Bit 6: Reserved
Bit 5: Reserved
Bit 4: Reserved
Bit 3: Reserved
Bit 2: Management Module sets a "1" in this position to indicate that the Switch Module should read the "IP Acquisition Method" and "Static Assigned IP Address/Subnet/Gateway" of the VPD's "Dynamic Block Systems Management Area" to update Switch IP configuration.
A "0" in this position indicates no change to the IP configuration has been requested.
Default value is "0".
Bits 1,0:Extended Diagnostic Control
00 = Standard Diagnostics
01 = Extended Diagnostics with run time less than 5 minutes
10 = Full Diagnostics with run time less than 12 minutes
11 = Reserved
Default value for these bits will be "00". These bits will only be set in conjunction with CR(0).

Table 8-7 - I^2C Extended Control Register

Note: See section 13 on 'Switch Module Protect Mode and Switch Stacking Architecture' for additional behavior in regards to these Extended Control Register bits.

8.5.3 Status Register

A Status Register is available to present operation status to the Management Module; it is R/O from the system side and R/W from the Switch. The format of the register is shown in Table 8-8.

7	6	5	4	3	2	1	0

Bit 7: Reflects the value of bit 7 in the Control Register
This bit not cleared separately since it reflects the setting of control register bit 7.
Bit 6: Set to "1" on completion of the initialization/diagnostics.
Reset to "0" whenever initialization/diagnostics are initiated.
NOTE (1): If the diagnostics fail to complete (SM hangs), the diagnostic code in the diagnostic register will indicate the test in progress when the SM hang occurred. An automatic retry shall not be attempted by the SM.
NOTE (2): If the SM is in an initialization complete state and, therefore, the value of this bit is "1", the MM must see a transition on the bit from "1" to "0" to "1" whenever the SM performs a subsequent initialization or reset sequence. The transition time on the bit from "1" to "0" to "1" must be a minimum of 5 seconds. This sequence must account for: (a) all mechanisms that can cause the SM to perform a reset (including all external management applications, all management user interfaces, as well as hardware or firmware detected faults that will result in a reset) or (b) whenever a non-disruptive firmware upgrade is performed.
Bit 5: Reserved
Bit 4: Set to "1" to indicate over-current / under-voltage condition in Power Domain 2.
This also causes status register bit 3 to be set.
The power on default state is "0". This bit can only be cleared by 12V power being removed from the SM and then re-applied (removal/re-plug of SM or Chassis power re-cycle).
Bit 4 shall also be set if under-voltage monitoring is optionally implemented in Power Domain 2 and this condition is detected.

Bit 3: Set to "1" when an operational fault occurs during normal operation or if a fault is detected by concurrent diagnostics. Set by both critical and non-critical faults on the transition from a non-fault to a fault condition for any given fault. This excludes link faults during normal operation. The SM shall continue reporting the fault in bit "3" until the fault condition no longer exists. Reset to "0" by the SM as a result of the SM clearing the operational fault condition (due to the removal of the original fault).
Note: The Switch Fault LED shall be turned on by the bit 3 transition from a non-fault to a fault condition and is not turned off by a Management Module read of the status register.

Bit 2: Set to '1' to indicate the Switch Module has updated the "Current IP Acquisition Method" and the "Current IP Address/Subnet/Gateway" of the VPD's "Dynamic Block Controller Area". A '0' in this position indicates no change to the Current IP configuration has been made. Reset to "0" by the Switch Module as a result of a read by the Management Module. For power on reset operation, refer to note 6 below.

Bit 1: Set to "1" when Switch temperature meets/exceeds the second thermal threshold. Reset to "0" when Switch temperature drops below the second thermal threshold. (hysteresis must be provided between set and reset temperature points). It is expected that the thermal monitoring devices will be programmable since thermal thresholds may require adjustment based upon system variables.
Second Threshold = Shutdown Temperature = Maximum Operating Temperature [2]
Note: This bit shall not cause status register bit 3 to be set.

Bit 0: Set to "1" when Switch temperature meets/exceeds the first thermal threshold. Reset to "0" when Switch temperature drops below the first thermal threshold. (hysteresis must be provided between set and reset temperature points)
First Threshold = Warning Temperature = Lower Threshold of Max Operating Range[2]
It is expected that the thermal monitoring devices will be programmable since thermal thresholds may require adjustment based upon system variables.
Note: This bit shall not cause status register bit 3 to be set.

Table 8-8 - I²C Status Register

8.5.4 Extended Status Register

An Extended Status Register is available to present operation status to the Management Module; it is R/O from the system side and R/W from the switch. The format of the register is shown in Table 8-9..

7	6	5	4	3	2	1	0

Bit 7: Reserved
Bit 6: Reserved
Bit 5: Reserved
Bit 4: Reserved
Bit 3: Reserved
Bit 2: Reserved

Bit 1: DualFuseStatus - This informs the MM of the status of the dual fuses at the redundant 12V inputs (+12V_A and +12V_B). This bit indicates if either of the two fuses is open, in which case the actual power feeding the module is non-redundant regardless of power modules installed in the chassis. The transition of bit 1 (1 to 0 or 0 to 1) will cause an Interrupt.
1b = Fuse fault (A or B feed)
0b = Both fuses OK

[2]Maximum Operating and Lower Maximum Threshold are Switch/vendor/technology specific values.

Bit 0: PD2Status – Power Domain 2 Status. This status informs the MM to the On/Off status of power domain 2. The transition of bit 0 (1 to 0 or 0 to 1) will cause an Interrupt.
1b = Power Domain 2 is active or on.
0b = Power Domain 2 is inactive or off.

Table 8-9 - I²C Extended Status Register

Notes about I²C Status Register/Extended Status Register and I²C Interrupt Signal Operation:

1) The Switch Module's I²C Interrupt signal will be activated on a transition and only on a transition (0 -> 1 or 1 -> 0) for:
   a) Bits 0 (first thermal threshold), 1 (second thermal threshold), 2 (IP configuration update), 3 (operational fault), 4 (power domain 2 over-current fault) and 6 (power on/diagnostics completion) of the Status Register.
   b) Bit 0 (PD2 Status) and 1 (DualFuseStatus) of the Extended Status Register.
2) Bit 7 of the Status Register (control register wrap) does not affect the I²C Interrupt Signal and is not cleared since it reflects the setting of control register bit 7.
3) Rewriting the same state to a status bit (1 -> 1) will not activate the I²C Interrupt signal.
4) The I²C Interrupt Signal is cleared on a read of the Status Register and the Extended Status Register.
5) A read of the Status Register or Extended Status Register will not result in loss of a pending interrupt or the associated data due to coincidental read of that resource by the other participant on that I²C bus. (must synchronize – see Implementation note under section 8.1.1.4).
6) During a power on sequence, the Management Module toggles Control Register bit 0 to a '1' and waits for the Switch Module to set the Status Register bit 6 to a '1'. After Status Register bit 6 has been set, the Management Module writes the IP address, subnet mask, gateway IP address, and IP acquisition method to the VPD Dynamic Block System Management Area and sets the Extended Control Register bit 2 to a '1'. On the 0->1 transition of the Extended Control Register bit 2, the Switch Module must examine the "IP Acquisition Method" and the "Static Assigned IP Address/Subnet/Gateway" of the "Dynamic Block Systems Management Area" to determine how the IP address of the Switch should be acquired/configured.
7) The state of bit 0 (PD2Status) and 1 (DualFuseStatus) of the Extended Status Register must always reflect the current state.. Neither bit is cleared on a read.

8.5.5 POST Diagnostic Register

A diagnostic status register is written by the Switch CPU subsystem as it progresses through its initialization process (this register does not display concurrent diagnostics status). The register is R/W from the Switch side and R/O by the Management Module to collect the status. The format of the register is shown in Table 8-10. If a critical error occurs during POST diagnostics then the Switch should not operate. If a non-critical error occurs during POST diagnostics then Switch should remain in the operational state.

7	6	5	4	3	2	1	0

Bits 7:0 Diagnostic Indicator

Table 8-10 - I²C POST Diagnostic Register

Diagnostic Indicator (in Hex)	Failing Functional Area	Failure Criticality
00 – 7F	Base Internal Functions	Critical
80 – 9F	Internal Interface Failures	Non-Critical
A0 – AF	External Interface Errors	Non-Critical
B0 – FE	Reserved	Non-Critical
FF	Switch "Good" Indicator	Operation

Table 8-11 - I²C POST Diagnostic Register defined ranges

Note: Defined error values for specific Switch versions/products to be coordinated between supplier and the manufacturer development contact.

8.5.6 TempRegister1 and TempRegister2

Each Switch Module must provide the following information via I2C Status Registers. The Switch Module will encode the temperature of the 1st temperature sensor in TempRegister1 at I2C address 0Ah and the 2nd temperature sensor in TempRegister2 at I²C address 0Bh. The values placed into the status register are shown in Table 8-12 below.

All reported temperatures must either be accurate at all times or report that the sensor reading is not available at the time it is requested. If for some reason a temperature sensor or related hardware is known to be inaccurate then the HW must report that temperature values are unknown.

Temperature	Comments		
	Binary	Hex	
	0111 1111	7Fh	Reserved
+>125°C	0111 1110	7Eh	Temps => 125.5°C
+125°C	0111 1101	7Dh	
:	:	:	temps between +2.5°C and +124.5°C
+.2.0°C	0000 0010	02h	
+.1.0°C	0000 0001	01h	
0°C	0000 0000	00h	
−1.0°C	1111 1111	FFh	
:	:	:	temps between -1.50°C and -9.5°C
-10.00°C	1111 0110	F6h	Any temp that is -10.00°C or lower
N/A	1000 0011	83h	Status: In POST (default setting caused by PD2 inactive / reset)
	1000 0010	82h	Status: Temperature sensor or a mechanism associated with reading the sensor has failed. Action: Retry
	1000 0001	81h	Status: Temperature sensor or a mechanism associated with reading the sensor has failed solid. Action: Do not retry
	1000 0000	80h	Status: Busy. Action: Retry

Notes:
- All other values reserved.
- TempSensorLoc in VPD @ offset 02ECh in block 1 represents the location of the second temperature sensor including an indication that the 2nd sensor is not implemented.

Table 8-12 - TempRegister1 and TempRegister2 Values

The Management Module relies on the SM Control Point to do the A/D conversion of the sensor itself. Each temperature sensor must be capable of the A/D conversion at least once every 10 - 15 seconds. The SM must indicate support for this function by setting the *Thermal Monitoring Capability* bit (see VPD Block 1 @02A0h Capabilities(11)=1b).

The control point within each Switch Module is responsible to update TempRegister1 and TempRegister2 with specific temperature values and other status information described in this document on a sensor by sensor basis. The MM will typically read the status register(s) when directed by an external or internal application request.

The mandatory exhaust temperature sensor reported in TempRegister1 is 1 byte in length and located at I2C address B3h, B5h, B9h, BFh for 1X switch bays (as a function of the switch bay location) and B1h for HSSMs using I2C offset 0Ah.

The optional exhaust, inlet, ASIC or heatsink temperature sensor reported in TempRegister2 is at offset 0Bh. The *TempSensorLoc* VPD field (see VPD Block 1 @02ECh) indicates the location of the 2nd temperature sensor. This field in VPD indicates that the temperature sensor is either not implemented or located in the inlet air flow, exhaust air flow, within the ASIC or on the heat sink (see the *BladeServer Base Specification for VPD* for additional information).

For Switch Modules the preferred design is that logic required to acquire temperature throughout the component be located on Power Domain 1. If the temperature sensors or associated logic are located in Power Domain 2 then the SM will set the default value of 83h into TempRegister1 and TempRegister2 when Power Domain 2 is inactive (off) or when a switch reset is initiated. Therefore, reads to TempRegister1 or 2 by the MM prior to the Switch Module exiting POST will return 83h. Reads to TempRegister1 or 2 by the MM after the Switch Module exits POST will return a valid temperature.

8.6 Management Module Usage Scenarios

8.6.1 MM Initiated Switch Module Power-On Sequence

When a SM is inserted or detected in the chassis at chassis initialization the following switch initialization occurs:

1. Power is applied to Power Domain 1 (PD1), which includes the I^2C circuitry. The SM activates the presence bit on the midplane, determines its slot address from the midplane, and also determines from the MM_Select pins on the midplane whether to use the A or B I^2C bus and the A or B Ethernet port.
2. The Management Module (MM) detects that the switch has activated the presence bit. The MM writes the history log (that identifies chassis type) into the switch VPD.
3. The MM identifies the switch by reading the VPD data and then cross-validates the switch type (Ethernet, Fibre, Infiniband….etc) in the chassis with the blades and/or expansion cards network port configuration. If an incompatible blade or expansion card interface is detected, the Management Module will post a log and set an indicator, which is visible to the customer. The next step in the sequence is then executed.
4. The MM reads the VPD to determine the maximum power consumed by the SM.
5. The MM writes the configured IP address from the MM's NVRAM into the SM's VPD Dynamic Block System Management Area.
6. The MM sets the Extended Control Register diagnostic bits (bits 0, 1) to define the level of extended diagnostic to be executed.

7. The MM sets the power-on bit in the Control Register (bit 0), which causes the SM to transition from PD1 to PD2.
8. The switch module begins its power-on self test (POST) sequence and executes the correct level of diagnostics. The SM initializes the Diagnostic Register to all zeroes and subsequently writes the appropriate POST codes into the Diagnostic Register as diagnostics are executed. The appropriate diagnostic code must be loaded into this register prior to the execution of the corresponding test.
9. Upon POST completion, the SM must initialized the VPD 'capabilities' field, the appropriate diagnostic code is recorded into the Diagnostic Register and Status Register bit 6 is set to 1 (POST complete). When POST is complete, the SM must also have written to the VPD the default IP address based on the detected slot position from the midplane.
10. The Management Module reads the Status and Diagnostic Registers and, if no critical test error occurred, then the MM executes the IP change protocol sequence. After successful completion of the IP change protocol sequence, the MM will update its internal routing table to provide MM external port connectivity to the switch's internal management Ethernet port.
11. IP traffic can now flow from the SM to the MM.

8.6.2 Management Module POST Timeout Values

The following are the Management Module POST timeouts values that are enforced for switch modules. The MM will start a timer when the power-bit is set on in the CR(0) to begin a POST of the SM. Exceeding these timeout values will cause the Management Module to post an error log and set an indicator which is visible to the customer. The log will contain information that a POST timeout condition has occurred.

POST Diagnostic Level	Management Module Timeout Value
Standard Diagnostics	60 seconds
Extended Diagnostics	300 seconds
Full Diagnostics	720 seconds

8.6.3 IP Address Change Sequences for the SM Control Point

There are fundamentally two different methods in which the switch module control point IP address configuration can be altered. One method is initiated using the I^2C interface from the MM, the other method is initiated from the SM using a SM defined user interface (this interface includes, but is not limited to, a CLI, Web Server, SNMP Agent, or a standalone application).

There are several VPD IP configuration fields used when the IP address is changed at the SM, which includes the following:

- Dynamic Block Controller Area Default IP Address(DBCDIP)
- Dynamic Block Controller Area Current IP acquisition method(DBCCIAQ)
- Dynamic Block Controller Area Current IP Address(DBCCIP)
- Dynamic Block System Management Area IP acquisition method(DBSMIAQ)
- Dynamic Block System Management Area Static IP Address(DBSMSIP)

8.6.3.1 MM Initiated IP Address change using I^2C

The following sequence describes the SM behavior when the MM initiates an IP address change. When CR(3) = 0, the MM is in full control of the IP Address of the SM control point. When the MM wants to change the IP Address of the SM control point, the MM informs the SM by changing CR(3) to 0, thus removing the ability of the SM to be controlled externally. When the MM takes this action, the SM must take into account that the external application may be in the process of changing the IP address.

1. The MM saves the state of CR(3).
2. The MM sets CR(3) = 0, preventing external SM control of the IP address, and initiates a wait of 2.0 seconds. 2.0 seconds is based upon the maximum time the SM requires to complete processing the most complicated IP configuration change initiated externally. This includes the SM setting of SR(2), signaling that an external application has changed the SM's IP Address. The Switch processing time should not exceed 0.5 seconds. Note, this limits the time to 0.5 seconds that the SM has to handle an external SM application (like a CLI) to the SM firmware processing an IP configuration change. The 0.5 sec is used to bound the time after the moment a user does the 'apply'. If a situation occurs where, at the same time the MM is setting CR(3) to a 0, an external application on the SM is executing an IP change request, then the 2 seconds wait after setting CR(3) to zero will cover the maximum of 0.5 sec of SM processing time.
3. If CR(3) was 1, then a 1→0 transition will interrupt the SM and the SM shall prevent any new or additional IP configuration changes from being initiated, unless they come from the MM. If an IP configuration change is in progress when the interrupt is generated, then that operation will be completed as normal. The Switch Module will set SR(2) = 1 when the DBCCIAQ and DBCCIP of the VPD data have been updated by the SM informing the MM. Subsequent IP configuration changes from anywhere other than the MM shall not be accepted when CR(3) = 0. As a result of the I^2C interrupt generated on the SR(2) 0→1 transition indicating that the IP configuration change is complete, the MM will post the normal IP configuration alert. If the Management Module sets CR(3)=0, a telnet interface that has admin mode active for editing any Switch configuration (including IP configuration) will have the admin session immediately cancelled. The user will see an alarm posted in the telnet window that the admin session was cancelled by another user. Whatever operation was in process at that time will be aborted in an orderly manner.

   If CR(3) was 0, then no IP configuration changes from other than the MM would be allowed and hence no change would be in progress. The MM may rewrite CR(3) 0→0, since no I^2C interrupt would be generated at the SM. The 2.0 second wait initiated by the Management Module in step 2.) will expire, by which time the Switch Module must ensure any IP configuration change in progress must have completed, SR(2) must have been set, and no new changes will be initiated by other than the Management Module.
   Since multiple IP configuration parameters may be modified either as one atomic operation or as multiple operations by Switch Module configuration applications, it is the responsibility of the Switch Module and corresponding configuration application to ensure orderly termination in the event a non atomic operation is interrupted as the result of CR(3) 1→0 transition.
   NOTE: Synchronization of the setting of CR(3) between the Management Module and the Switch Module must always be accomplished in this manner.
4. In the event SR(2) was set to 1 as a result of an in progress IP configuration change, the MM will initiate a read of the Switch Module status register, causing SR(2) to be cleared by the Switch Module.

5. Management Module writes IP configuration change data to Switch Module DBSMIAQ and DBSMSIP of the VPD, either as an atomic operation (all parameters to be updated in one transfer) or as multiple operations.
6. The Management Module sets ECR(2) = 1 to signal the Switch Module
    a. that the VPD data transfer from the Management Module is complete
    b. to initiate the change of the IP address
7. The Switch Module responds to the I^2C interrupt generated as a result of ECR(2) 0→1 by reading ECR(2), ensuring the corresponding IP fields DBCCIAQ and DBCCIP in the VPD are updated, and sets SR(2) = 1 indicating successful completion of the transaction.
8. The Management Module, upon receiving the I^2C interrupt resulting from the SR(2) 0→1 transition, initiates a read of the Switch Module status register, causing SR(2) to be cleared by the Switch Module. In addition, the MM will clear ECR(2) after the read of the status register and will post the normal IP configuration alert.
9. If the MM does not receive the SR(2) acknowledgment within 0.5 s, a completion error alert may be posted and ECR(2) will be cleared.
10. The MM will restore the state of CR(3).
11. After successful completion of the IP change protocol sequence, the MM will update its internal routing table to provide MM external port connectivity to the switch's internal management Ethernet port.

Notes:
(1) The assumption is that the IP acquisition method (DBCCIAQ) can change at any time and will not require a restart of the Switch. The DBCCIP fields must be updated by the Switch to reflect the changes.
(2) Refer to the operation of Status Register Bit 2 and Extended Control Register Bit 2 for IP configuration.
(3) The current IP address, Subnet mask, and gateway IP address are retained through power on / reset cycles and are not replaced by the default values.
(4) The SM must protect against concurrent IP configuration changes from both the MM and the SM. When the MM initiates an IP change and sets CR(3) = 0, then the SM has 0.5 s to complete any IP change currently in progress.

8.6.3.2 Switch Module Initiated IP Configuration Change

The Switch Module can initiate an IP change sequence from one of the various user interfaces.

When a SM initiates the IP configuration change the following will happen:

1. The SM will write DBCCIAQ and the DBCCIP areas of VPD and then set SR(2) = 1.
2. The MM, upon receiving the I^2C interrupt resulting from the SR(2) 0→1 transition, will initiate a read of the SM status register, causing SR(2) to be cleared by the SM. The MM will also clear ECR(2) at this time.
3. The Management Module will log and notify the MM end user that the SM IP address has been asynchronously changed.

8.6.3.3 Switch Module Default IP Address Handling

The value of the IP address in the DBCDIP will be assigned as 10.90.90.9x for 1X switches and 10.90.90.8x for 4X switches at switch manufacturing time with "x" set to zero. At Switch Module power on, the IP address value in the DBCDIP is rewritten such that "x" reflects the Switch Module's Switch Bay ID. In addition, the manufacturing default values for the default subnet mask is 255.255.255.0, default gateway address is 0.0.0.0 and the default IP acquisition method will be set to 'static'.

The default value for the IP Address and IP acquisition method will also be set into the DBCCIAQ and DBCCIP of the VPD whenever the SM is set to its manufacturing default configuration. This can happen from the MM when both CR(6) and CR(0) are set to one. This also can happen from the various SM user interfaces when the user selects to reset the configuration back to defaults.

8.6.3.4 IP configuration notes:

1. Whenever the IP address is changed, from either a MM initiated change or a SM initiated change, the MM must be notified by the SM transitioning SR(2) from 0→1. This is true even when the previous IP configuration matches the current IP configuration.
2. The IP addresses must be preserved through power cycles or Switch removal. Also, configuration changes that will result in a new IP address will potentially disrupt existing links to remote management entities and, therefore, must be carefully controlled.

8.6.4 Switch Module Overtemp

The intent of this section of the specification is to specify consistent Over-Temperature behavior between the Switch Module and the Management Module when an over-temperature condition occurs. All SM's shall report Over-Temperature conditions and related behaviors as defined below.

Each SM will notify the MM of the ability to support this Over-Temperature Architecture by setting VPD:Capabilities (*SM_OT_Supported*) bit to 1b within the VPD Dynamic Block Controller area.

The SM shall protect itself from damage by removing power to Power Domain 2 (PD2) when the *Shutdown* over-temperature condition occurs. Associated with this behavior comes the need for the SM to inform the MM of the state of PD2 by setting *ESR bit 0, PD2Status,* which will indicate the current state of PD2. This value shall be accurate regardless of the on/off state of PD2 and therefore shall be implemented in Power Domain 1 (PD1), the Aux or Stand-by power domain in the SM.

Two temperature thresholds from any number of sensors are required in all SM's representing *Warning* and *Shutdown* conditions. When any sensor reaches its threshold value, the SM shall set the I^2C Status Register(SR(0:1)). An SM vendor may have any number of sensors located near critical components throughout the SM. The SM shall analyze each sensor and report the temperature status via SR(0:1) to the MM. Exactly which area or sensor that has reached the threshold is not reported to the MM.

This architecture is based on temperature sensor and associated logic powered in PD1.

The presence and/or failure state of the MM cannot be guaranteed. Therefore, the SM shall protect itself from running outside of its operating range by turning off PD2 when the Shutdown temperature is reached.

SM/MM Over-Temperature Design

The SM shall locate all temperature sensing and reporting logic on PD1 and indicate this capability via VPD:Capabilities (*SM_OT_Supported*) bit to 1b. The definition of the SM Over-Temperature behaviors SR(0), *Warning* and SR(1), *Shutdown* and are described below.

SR(0) - Over-Temperature Warning Sensor & Reporting Logic

The first lower temperature threshold is set to a trip point that is within the operating conditions of the SM and is considered to be the lower threshold of the maximum operating range by the SM vendor. The trip-point value of the sensor is selected by the SM vendor.

The SM sets SR(0)=1b to report the *Warning* temperature status when the SM temperature meets or exceeds the first thermal threshold. When the MM detects a 0b to 1b transition on SR(0) the MM may immediately ramp up the speed of the fans in an attempt to reduce the temperature of the SM. When the MM detects a 1b to 0b transition on SR(0) and no other components are reporting an Over *Warning* Temperature condition then the MM may ramp down the speed of the fans.

The SM resets SR(0)=0b to reset the *Warning* temperature status when the switch temperature drops below the first thermal threshold. Note that hysteresis must be provided between the set and reset temperature points such that SR (0) is not oscillating when the temperature of the SM is close to the *Warning* threshold.

SR(1) - Over-Temperature Shutdown Sensor & Reporting Logic

The second higher temperature threshold sensor is set to a trip point greater than the first threshold and protects the SM from running outside of its maximum reliable operating temperature and from possibly destroying components within the SM. The SM shall protect itself from damage by turning off Power Domain 2 (PD2) when the *Shutdown* temperature condition is detected. The trip-point value of the sensor is selected by the SM vendor. Shutting down PD2 will immediately start the cooling process on the SM.

When the SM temperature meets or exceeds the second thermal threshold then the SM:

- sets Status Register (SR(1)) =1b to report the *Shutdown* temperature status
- shuts down PD2 and sets ESR(*PD2Status*) =0b to indicate PD2 status to the MM.

SR(1) is reset to 0b when the temperature of the SM falls below the *Shutdown* threshold.

When PD2 in the SM is turned on by the MM after the SM is shutdown for an Over-Temperature condition the SM may require some amount of time to acquire the current temperature of the SM. Between the time that the SM powers on and the temperature of the SM is determined the SM shall run in a “low heat generation” mode to avoid the SM from reaching the *Shutdown* threshold without being able to detect the condition preventing the SM from running outside of its upper temperature range (i.e. *Shutdown* threshold). In other words, power cycling the SM is not a guaranteed method of removing the Shutdown condition and the SM is responsible to ensure that the module does not run outside its maximum thermal limit. In the event that the Administrator attempts to power on the switch while SR(1) =1b, the SM shall not turn power back on to the SM and will continue to report ESR(*PD2Status*)

=0b off. Once the temperature falls below the shutdown threshold and SR(1) is reset to 0b, new requests to power on PD2 shall be accepted.

The MM shall turn off PD2 whenever it detects SR(1) = 1b, *Shutdown*.

The conditions that turn on either SR(1) or SR(0) shall be reported independently from SR(3) – *Operational Fault.* Therefore, SR(3) shall not be turned on by the SM due to *Warning* or *Shutdown* temperature conditions.

VPD Requirements

Entries are required in the following VPD fields to support the Over-Temperature design. The first VPD Version/Level to support the Over-Temperature design is 0101h and is located in Block 0, offset 0002h. Reference the *BladeServer Base Specification for VPD*.

Capabilities

Block 1 of VPD contains a Capabilities field which indicates to the MM that the SM has implemented certain functions described in this specification.

- Capabilities (6)
  - 1b - The SM has implemented ESR*(PD2Status)* as defined in ESR(*PD2Status*) below. NOTE: This function is independent of bit 7 so that the function can be used independent of this Over-Temperature design.
  - 0b - The SM does not support ESR*(PD2Status)* or this SM is a legacy SM.
- Capabilities (7)
  - 1b - The SM supports all behaviors stated in this document.
  - 0b – The SM does not support this Over-Temperature design or this SM is a legacy SM.

ESR *(PD2Status)*

ESR*(PD2Status)* indicates the ON/OFF status of Power Domain 2. Only the MM can turn on PD2. Either the MM or the SM can turn off PD2. The SM shall turn off PD2 when a condition is detected that may lead to damage of the card or will prevent the SM from running outside its operating limits if power is not removed. There are a number of reasons why an SM may shut down PD2. This document addresses Shutdown Temperature Threshold reached and the SM or MM turning off PD2. The SM may shut down PD2 for other reasons such as a failure in SM power distribution logic or an Over-Current condition and so on. Regardless of the cause, the SM shall report the status of PD2 in ESR*(PD2Status)*. A 1b to 0b transition on this ESR status bit will cause an Interrupt to the MM. A 1b will represent PD2 being active and a 0b will represent PD2 being inactive.

The SM shall make every effort to report the correct status in ESR*(PD2Status)*. Therefore, all logic associated with reporting *PD2Status* shall be on PD1.

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9 Switch Mechanical

9.1 1X Switch General Description

The Switch Module mechanical enclosure is based on a single wide, single high InfiniBand Module. It uses a Molex / Amphenol VHDM signal connector to interface to the midplane. Depending on the position of the Switch Module, the airflow is from top to bottom or bottom to top.

The Switch enclosure has the following features:

- Width 29 mm, height 112 mm, depth 259.8 mm (longer than InfiniBand)
- Card to card pitch, 30 mm
- Retention: single cam lever with snap latch

It is the responsibility of the developer to ensure all required National and International applicable safety and marketing requirements are met, such as, but not limited to, 240VA limiting and EMC and ESD Standards.

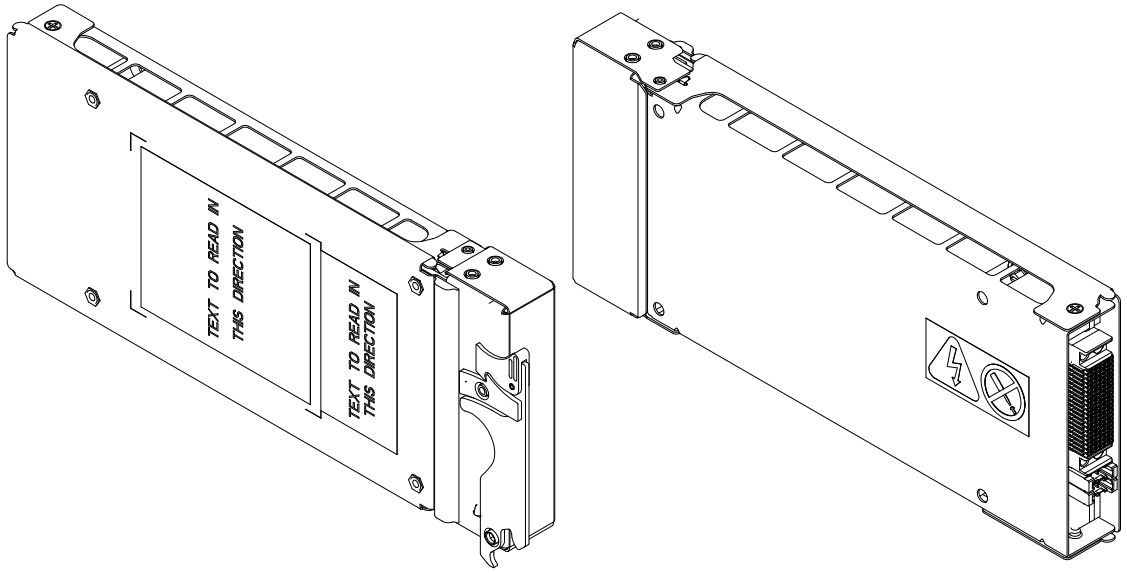

Figure 9-1 - 1X Switch Module – Isometric Views

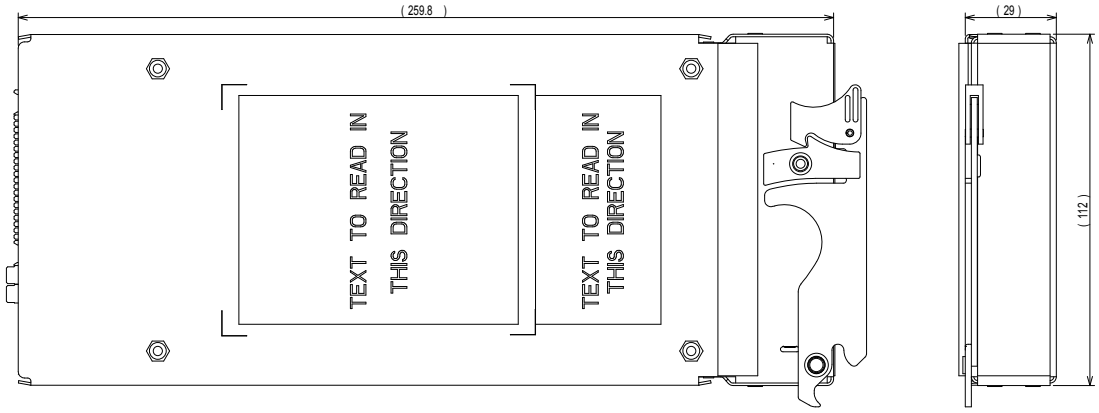

Figure 9-2 - 1X Switch Module - Size

9.2 1X Switch Mechanical Design

A 1X Switch Module Mechanical Design Kit is available at the following URL:

http://www-03.ibm.com/systems/bladecenter/resources/openspecs.html.

This kit will provide data necessary to design the mechanical enclosure and printed circuit card for the switch module. It is recommended that the construction technique described by the design data be followed. However, it may be modified per the application. The mechanical design kit consists of a "Readme" file, a set of 3D CAD models, and PDF files, which provide a base for designing a switch module enclosure. The 3D CAD models are in Pro/ENGINEER design software, IGES, STEP, and an EMN file format. The EMN file of the printed circuit card will define the card outline, connector location, component keep-out areas and component height restrictions. The 2D drawings are provided in Adobe® PDF file format. A bill of material is included in the design kit readme file. Mechanical information in this design kit shall take precedence over the same information contained in this specification.

9.3 1X Switch Module Card Outline

The 1X Switch Module card outline is described below. The following information is for reference purposes only. Refer to the Mechanical Design Kit described above for more details.

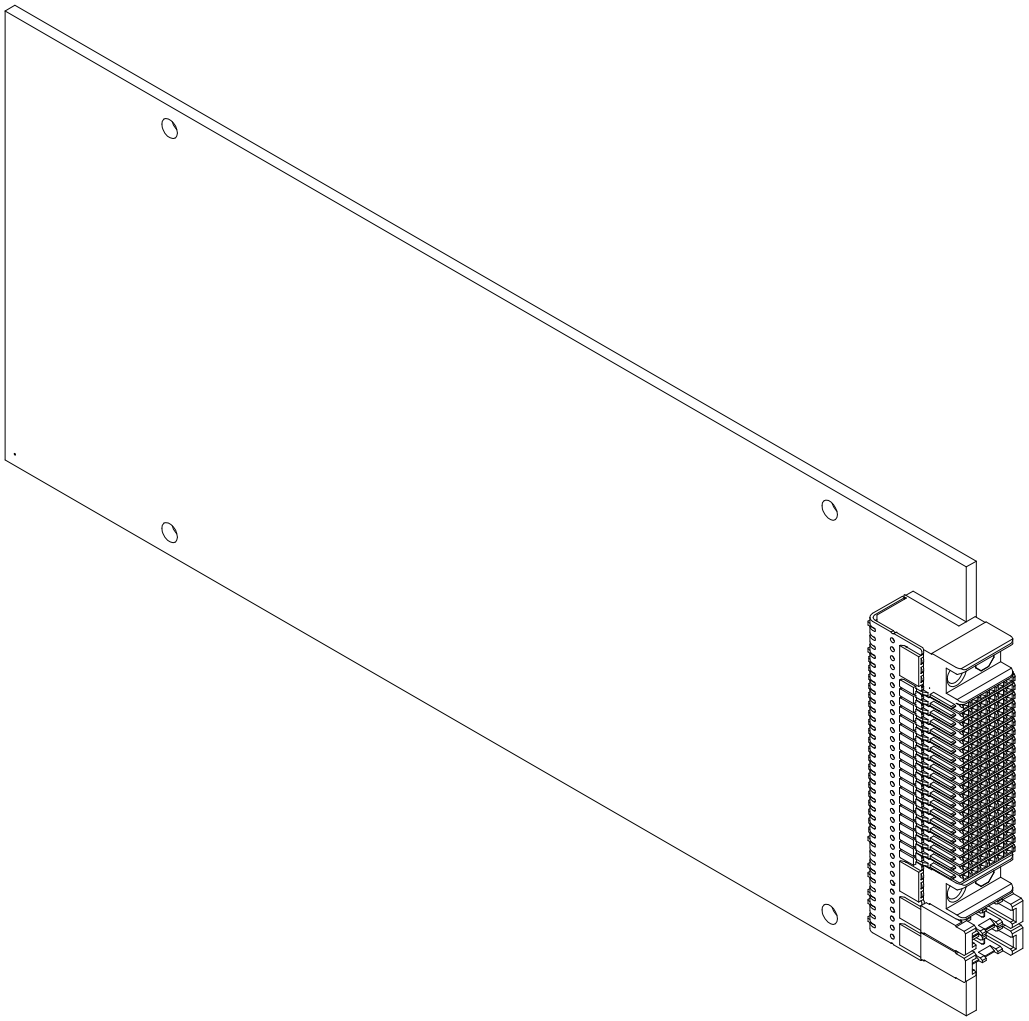

Figure 9-3 - 1X Switch Module Card Isometric View

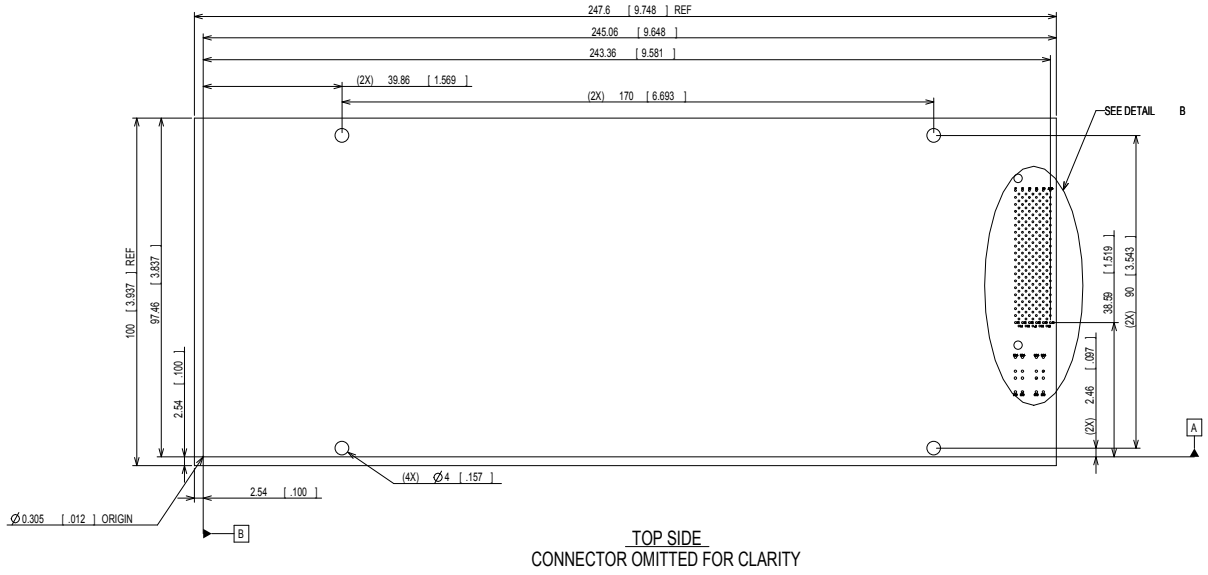

Figure 9-4 - 1X Switch Module Card Dimensions

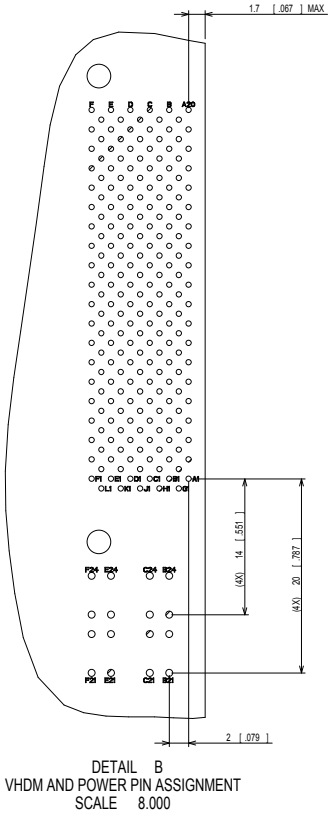

Figure 9-5 - 1X Switch Module Card Connector Signal and Power Pin Locations

9.4 1X Switch Material, Corrosion Resistance and Surface Conductivity

The material for the sheet metal is to be commercial quality hot dipped galvanized sheet steel with minimum spangle. Chemical treatments for corrosion resistance must be free of hexavalent chromium. Corrosion resistance must meet Class 3 requirements for salt spray testing per ASTM B117. Class 3 requires less than 5% white rust after 72 hours of testing. Additionally, good surface conductivity of the sheet steel is important to ensure proper grounding for EMC purposes. For this reason, the sheet metal must have less than 1 mΩ of surface resistance. The preferred resistance meter is a Loresta-EP CP-T360 with type BSP probes. A four point test is performed. A source for hot-dipped galvanized sheet metal which will meet the required corrosion resistance and surface conductivity is Yieh Phui Enterprise Co., LTD, their material code HGCC1-ZSEX. As an alternate metal, electro-galvanized sheet metal may be used. Again, corrosion resistance and surface conductivity requirements must be met. A source for this electro-galvanized sheet metal is Nippon Steel Corporation, their material code Zinkote 21-QS or Zinkote 21-QSK. Whether using hot-dipped or electro-galvanized metal, the sheet metal should have a minimum Rockwell B hardness of 55.

9.5 4X Switch Module General Dimensions

The High Speed Switch Module is designed to be plugged into any of the four high speed module bays in the 4X BladeServer chassis. The form factor of the HSSM (4X Switch Module) is different than the 1X Switch Module form factor. The HSSM is available in two different form factors based on the depth of the connector I/O faceplate from the rear of the chassis. The purpose of having two different depths is necessitated by having to provide strain relief for a subset of cable connectors. Infiniband™ cables terminated with industry standard connectors for copper as well as Infiniband™ cables equipped with an optical transceiver module have been considered for use with Form Factor A (FFA). Other cable types used for data transfer equipped with connectors such as extra small form factor pluggable modules (XFP) and RJ-45 cables are better suited for Form Factor B (FFB). The general outer dimensions of the module are:

- Width = 293.9 mm
- Height = 20.0 mm (Single-High) and 41.0 mm (Double-High)
- Depth (FFA) = 233.72 mm (from faceplate outside surface to mid-plane connector mating face)
- Depth (FFB) = 260.93 mm (from faceplate outside surface to mid-plane connector mating face)

Because of the two different available form factors, there are two different card profiles from which to choose. Requirements such as card layout, I/O connector type, airflow allowance, usability, and human factors should be considered when choosing the most appropriate form factor.

To accommodate the high insertion and extraction forces associated with plugging a HSSM into and out of the 4x chassis midplane, a robust camming mechanism is required. However, because I/O connector space and space for airflow exit are both vying for the faceplate area, the design for the camming mechanism has been done in an effort to minimize intrusion into the faceplate area. The camming mechanism is based on the levers used in the 1X switch modules. For Form Factor B, the camming mechanism requires a component keep out along the front bottom side edge of the card.

Pictorial views of the two module form factors are shown below in Section 9.6.

9.6 4X Switch Mechanical Design

A 4X Switch Module Mechanical Design Kit is available at the following URL:

http://www-03.ibm.com/systems/bladecenter/resources/openspecs.html.

This kit will provide data necessary to design the mechanical enclosure and printed circuit card for the switch module. It is recommended that the construction technique described by the design data be followed. However, it may be modified per the application. The mechanical design kit consists of a "Readme" file, a set of 3D CAD models, and PDF files which provide a base for designing a switch module enclosure. The 3D CAD models are in Pro/ENGINEER design software, IGES, STEP, and an EMN file format. The EMN file of the printed circuit card will define the card outline, connector location, component keep-out areas and component height restrictions. The 2D drawings are provided in Adobe® PDF file format. A bill of material is included in the design kit readme file. Mechanical information in this design kit shall take precedence over the same information contained in this specification. Information describing 240 VA keep-out areas is stated exclusively in this document, not in the Mechanical Design Kit.

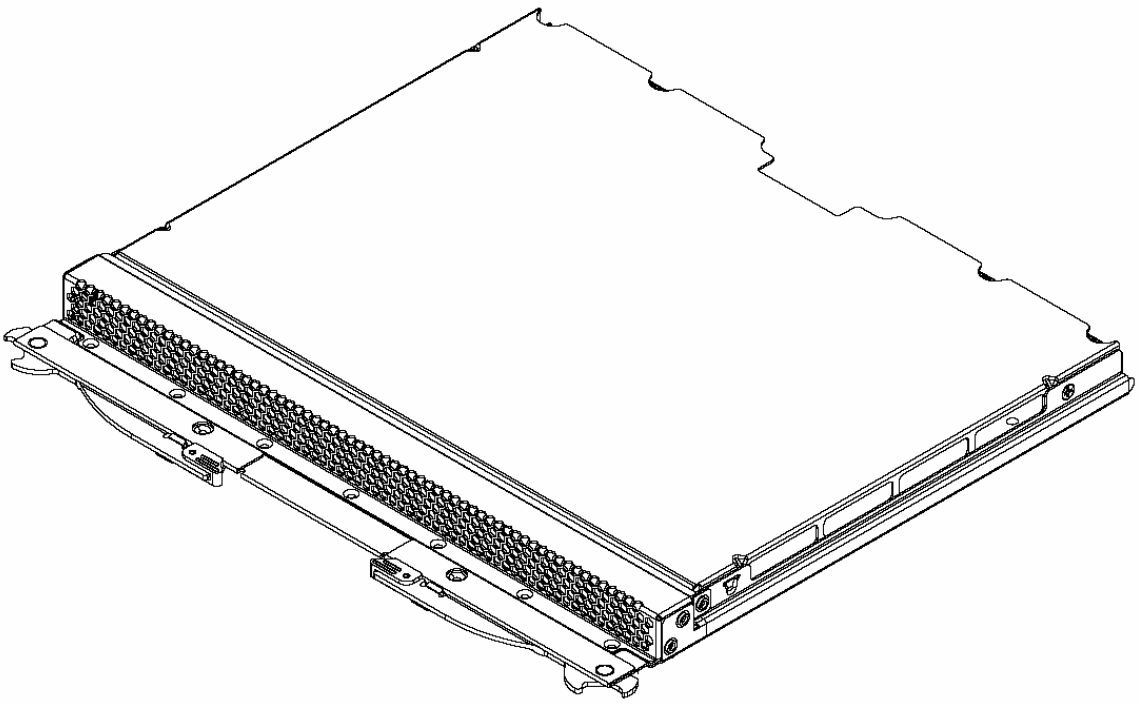

Figure 9-6 - High Speed Switch Module, Single-High, Form Factor A

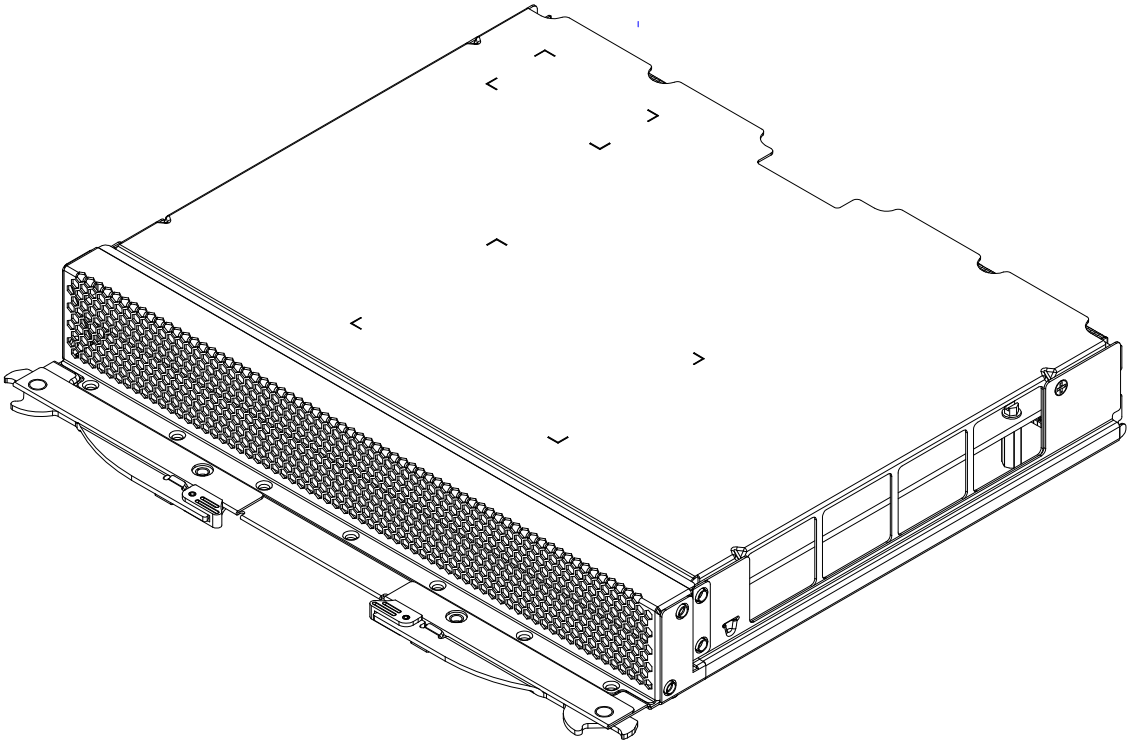

Figure 9-7 - High Speed Switch Module, Double-High, Form Factor A

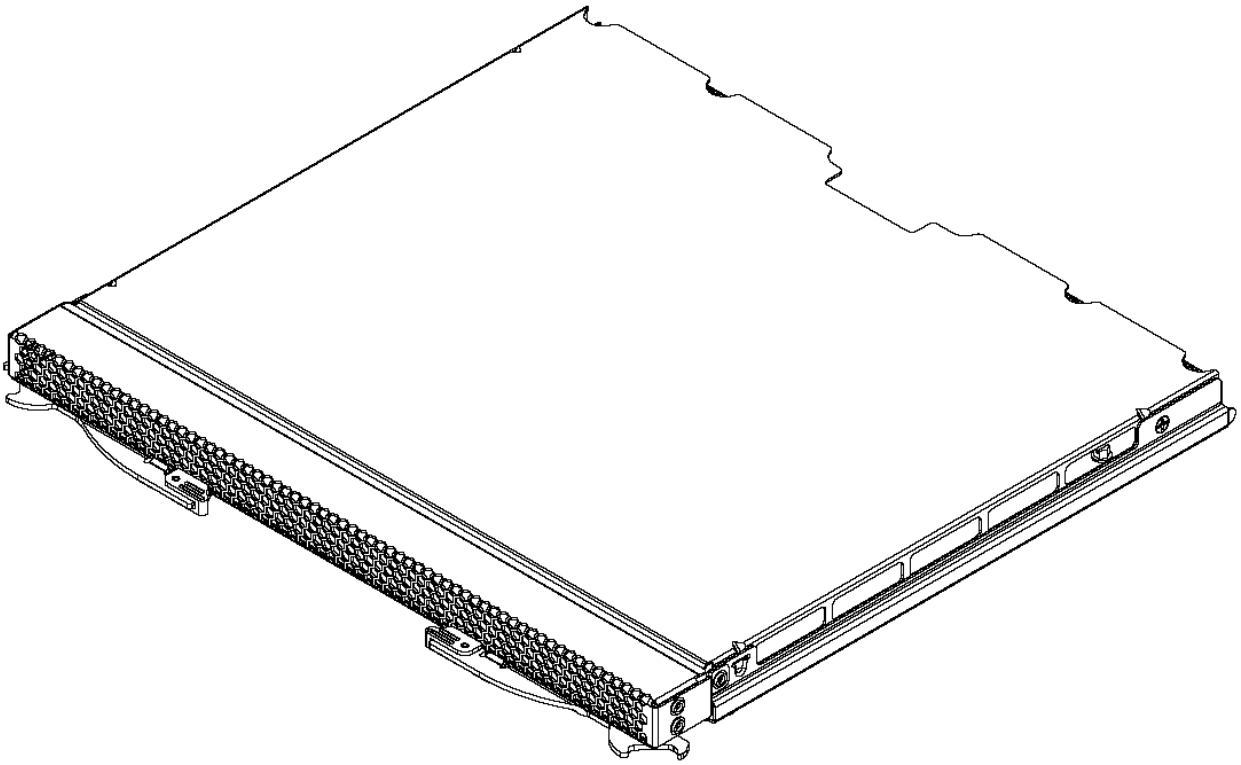

Figure 9-8 - High Speed Switch Module, Single-High, Form Factor B

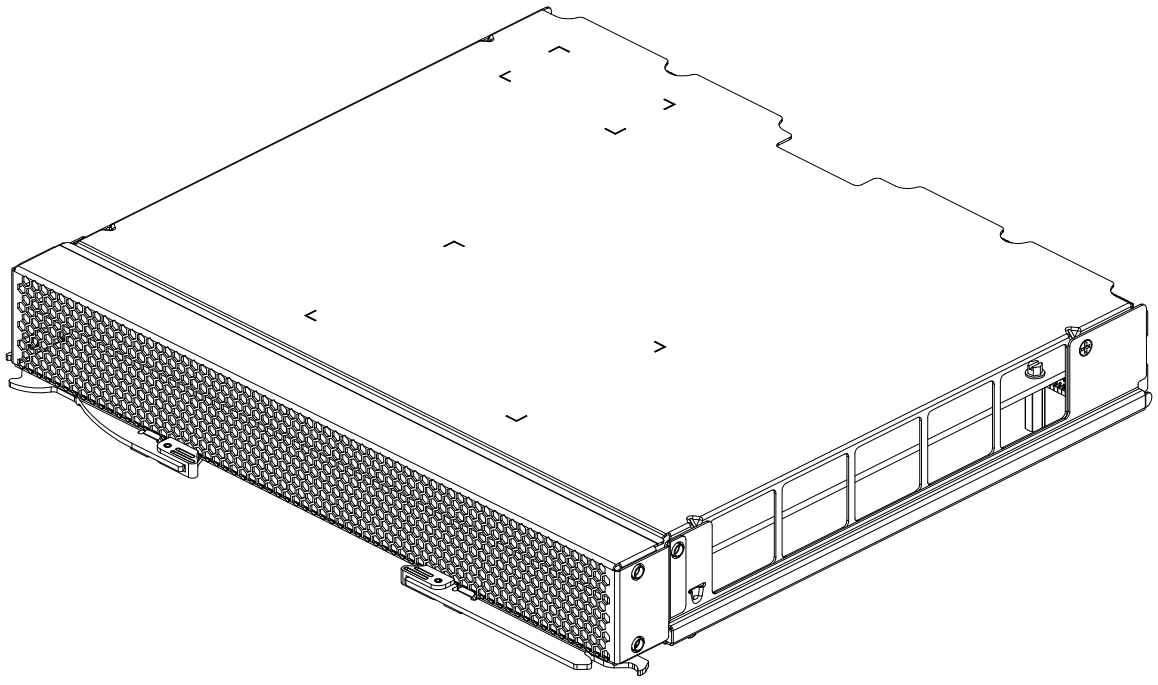

Figure 9-9 - High Speed Switch Module, Double-High, Form Factor B

9.7 4X Switch Card Outlines

Shown below are the profiles for both the card for Form Factor A and the card for Form Factor B. The primary difference between the cards is the additional 27 mm of depth for the Form Factor B card. Mounting holes for the cards are not defined and are application dependent. The following information is for reference purposes only. Refer to the information in the Mechanical Design Kit described above for details.

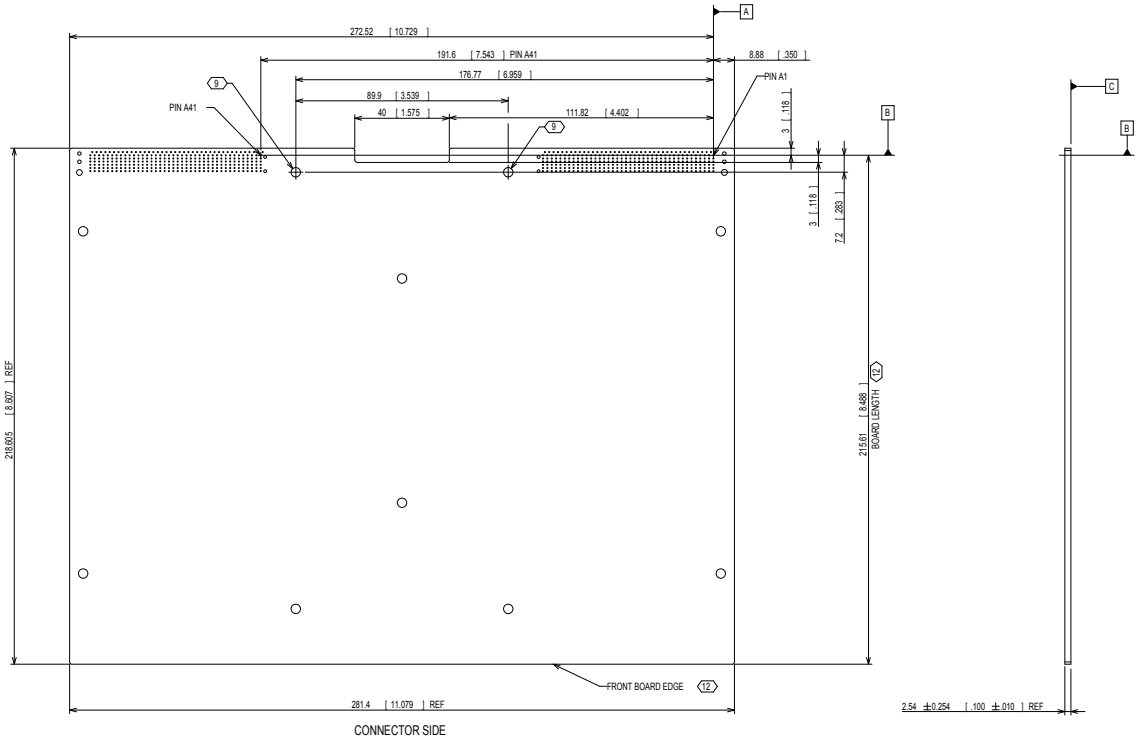

Figure 9-10 - Card Profile, Mounting holes, and Mid-Plane connector for Form Factor A

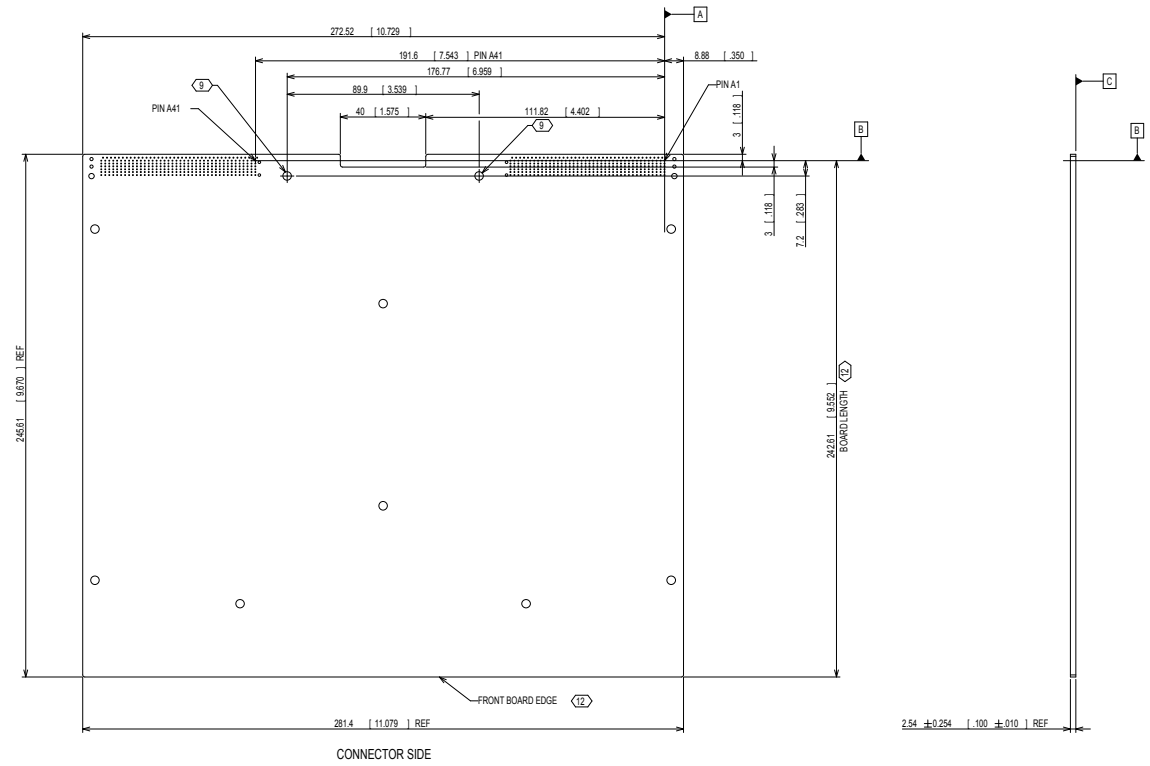

Figure 9-11 - Card Profile, Mounting holes, and Mid-Plane connector for Form Factor B

9.8 4X Switch Module Faceplate Requirements

The two figures below illustrate the available connector exit area on the faceplate for FFA and FFB. Primarily the available locations are dictated by the cam latching levers. The cross hatched area represents the region which must be studied carefully when doing connector placement to ensure that external cabling usability will not be obstructed by the cam levers. Also, refer to Figure 9-17 for vertical clearance for the cam levers.

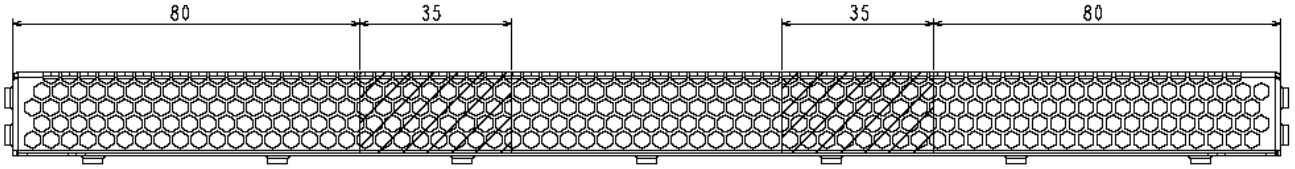

Figure 9-12 - Connector I/O permissible region (FFA)

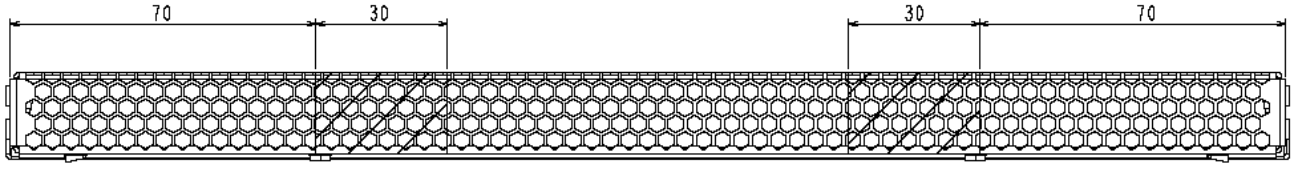

Figure 9-13 - Connector I/O permissible region (FFB)

The two figures below illustrate the overall airflow perforation pattern for the faceplates used for FFA and FFB. Obviously, this perforation pattern is shown occupying the entire front of the faceplate; but consideration should be given to connector placement to try to minimize the disruption of the pattern. The 2.77 mm dimension for FFA and 3.64 mm dimension for FFB must be maintained. This is because of aesthetic requirements as the HSSMs are placed in the front of some BladeServer Chassis. Also, for FFA, there are 5 vertical rows of perforation with the second row starting 2.4 mm from the top surface of the faceplate bracket. This dimension is necessary to allow for the first row of perforations to be divided equally through the upper form of the bracket. This dimension is to the top vertex of the hexagon. For a FFB faceplate, there are again five vertical rows of perforation with the top vertex of the hexagon on the second row being 2.4 mm from the top of the HSSM. Again, this positioning allows for the first horizontal row of perforation to be equally divided across the bend lines.

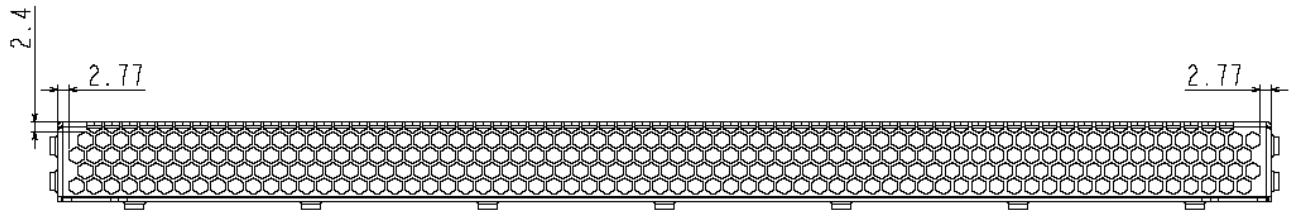

Figure 9-14 - Perforation Pattern for FFA faceplate

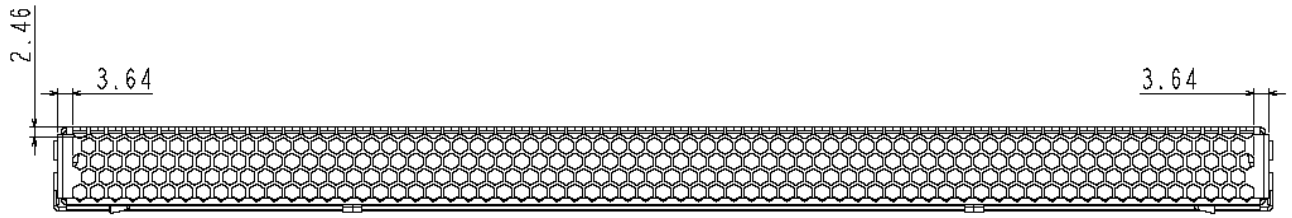

Figure 9-15 - Perforation Pattern for FFB faceplate

Shown in
Figure 9-16 is the detail of the perforation size. This perforation has been chosen based on considerations for mitigation of electromagnetic emissions and for the ability to achieve a large open area for airflow consideration.

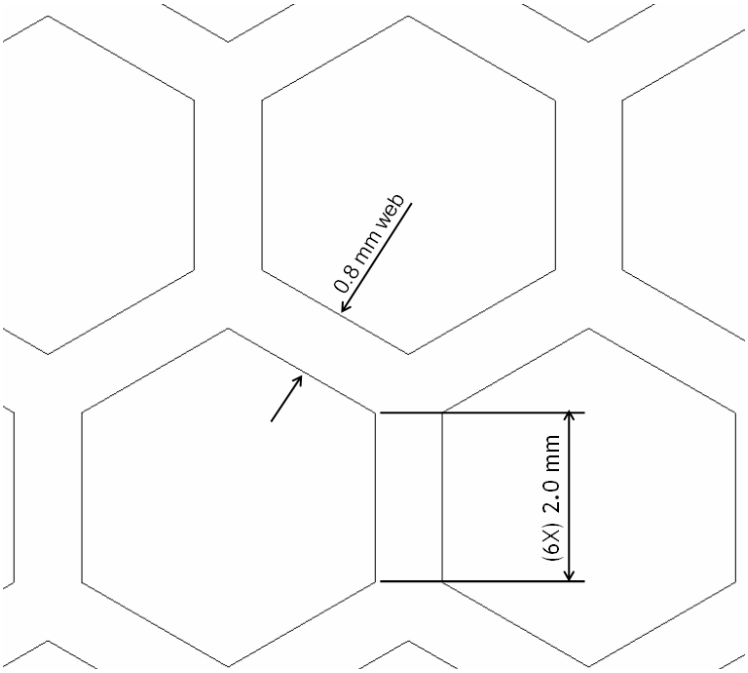

Figure 9-16 - Perforation Geometry

To ensure proper cooling for other subsystems in the chassis, including other HSSMs, it is important that the faceplate open frontal area remaining after making provision for I/O connectors, LEDs, and labeling result in airflow impedance for the enclosure assembly within the bounds as specified in Section 6.4.

9.9 4X Switch Module Tooling

The mechanical enclosure for the HSSM has been designed with the desire to have as much of the hardware as possible be common across various switch designs. The base is common with the exception of the card mounting standoffs. The faceplate itself is a separate item and can be customized as a unique part number for the desired connector I/O and LED/light-pipes. This faceplate bracket is designed to be spin riveted to the common mechanical enclosure assembly. For the FFB module, the mechanical enclosure does not have a separate faceplate as in the case for FFA. However, it is planned that base and the insertion and extraction levers are common and the customizing of the enclosure will involve only the card mounting standoff locations and the cutouts on the faceplate. For this reason it is anticipated that tooling for the FFB switch be setup such that the blanking of the faceplate area will be done in a separate stage of tooling. This has the advantage that only that stage of tooling would need to be created for a new and different faceplate configuration. Shown in Figure 9-17 is a graphic, which illustrates the common and unique mechanical parts for the FFA module mechanical enclosure.

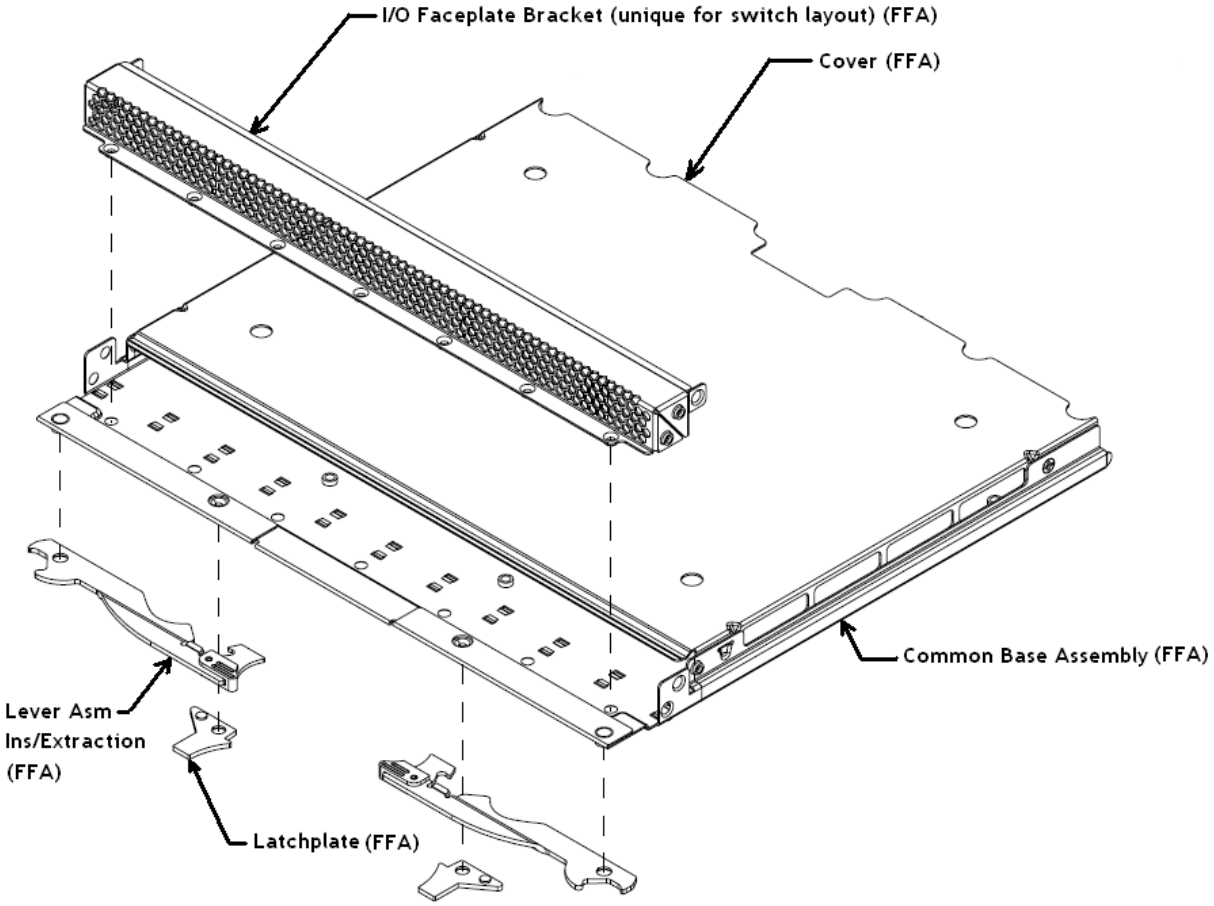

Figure 9-17 - Common Mechanical Enclosure (FFA)

9.10 4X Switch Module Material, Corrosion Resistance and Surface Conductivity

The material for the sheet metal is to be commercial quality hot dipped galvanized sheet steel with minimum spangle. Chemical treatments for corrosion resistance must be free of hexavalent chromium. Corrosion resistance must meet Class 3 requirements for salt spray testing per ASTM B117. Class 3 requires less than 5% white rust after 72 hours of testing. Additionally, good surface conductivity of the sheet steel is important to ensure proper grounding for EMC purposes. For this reason, the sheet metal must have less than 1 mΩ of surface resistance. The preferred resistance meter is a Loresta-EP CP-T360 with type BSP probes. A four point test is performed. A source for hot-dipped galvanized sheet metal which will meet the required corrosion resistance and surface conductivity is Yieh Phui Enterprise Co., LTD, their material code HGCC1-ZSEX. As an alternate metal, electro-galvanized sheet metal may be used. Again corrosion resistance and surface conductivity requirements must be met. A source for this electro-galvanized sheet metal is Nippon Steel Corporation, their material code Zinkote 21-QS or Zinkote 21-QSK. Whether using hot-dipped or electro-galvanized metal, the sheet metal should have a minimum Rockwell B hardness of 55.

9.11 4X Switch Module Cable Strain Relief (FFA)

As previously stated, the Form Factor A high speed switch module is a result of the necessity to have a means for supporting cables such as 4X and 12X InfiniBand™ cables. Figure 9-18 below shows the

vertical distance of the support shelf from the bottom of the enclosure. Also shown is the vertical distance to the top surface of the switch card. With these dimensions, it can be determined if a given cable connector can be accommodated without interference with the support bracket.

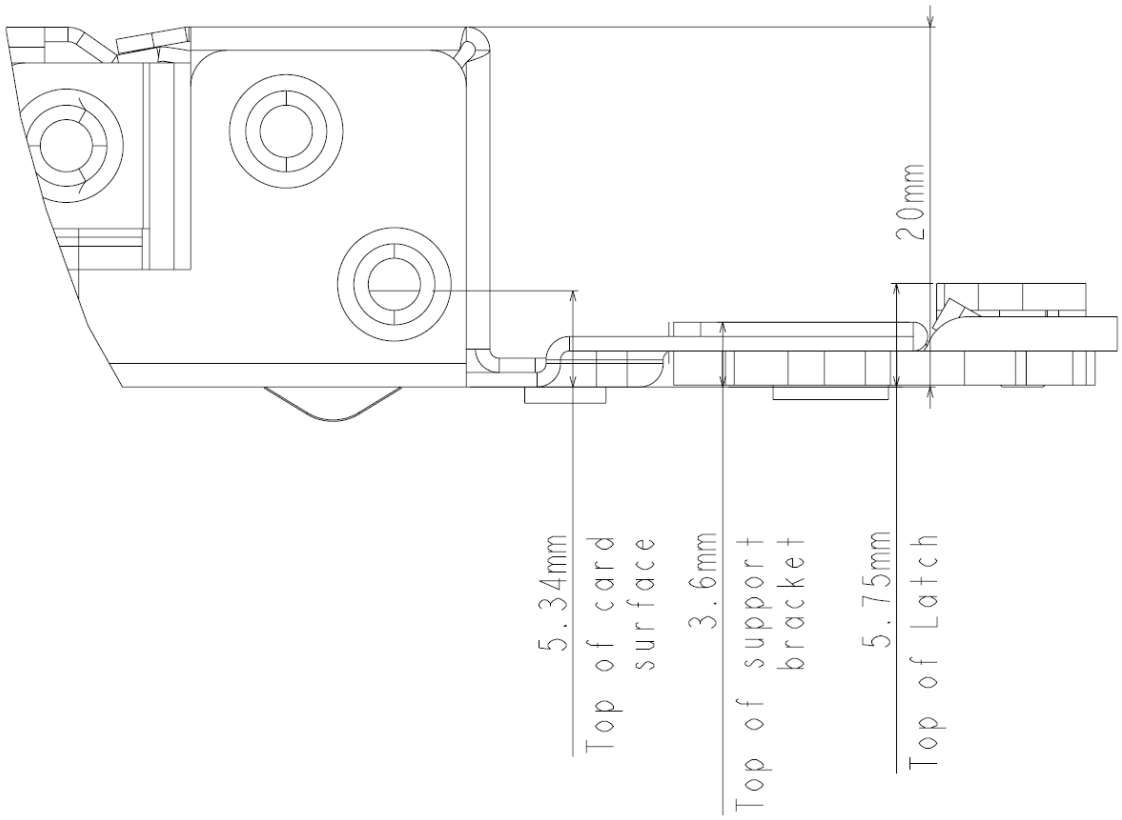

Figure 9-18- Side View, FFA, vertical location of cable connector support bracket

9.12 Bridge Module General Description

The Bridge Module mechanical enclosure is based on a single wide, single high InfiniBand Module. It uses a VHDM and a 54 position mezzanine signal connector to interface to the midplane. Depending on the position of the Bridge Module, the airflow is from top to bottom or bottom to top.

The Bridge enclosure has the following features:

- Width 29 mm, height 112 mm, depth 259.8 mm (same as 1xSM)
- Card to card pitch, 30 mm
- Retention: single cam lever with snap latch
- Enclosure Notch: The notch is designed into the Bridge Module to prevent a similar, but incompatible, 1X switch module from being inserted all the way into a bridge slot. In a dedicated Bridge Bay, in the chassis, there is a post that aligns with this notch to allow the Bridge Module to plug in fully. A 1x Switch Module without this notch would hit the post in the Bridge Bay, thus being prevented from full insertion into the bay. Shared switch/bridge bays do not have the post, so that either module type can be installed. In the 14-blade 4X Chassis, Bays 3 and 4 are shared switch/bridge bays, without the post. Bays 5 and 6 are dedicated bridge bays, and have the post to preclude the incorrect installation of a switch

module. In the 12-blade 4X chassis, Bays 1, 2, 3, and 4 are all shared switch/bridge bays. Refer to the Bridge Module mechanical kit for details.

It is the responsibility of the developer to insure all required National and International applicable safety and marketing requirements are met, such as, but not limited to, 240VA limiting and EMC and ESD Standards.

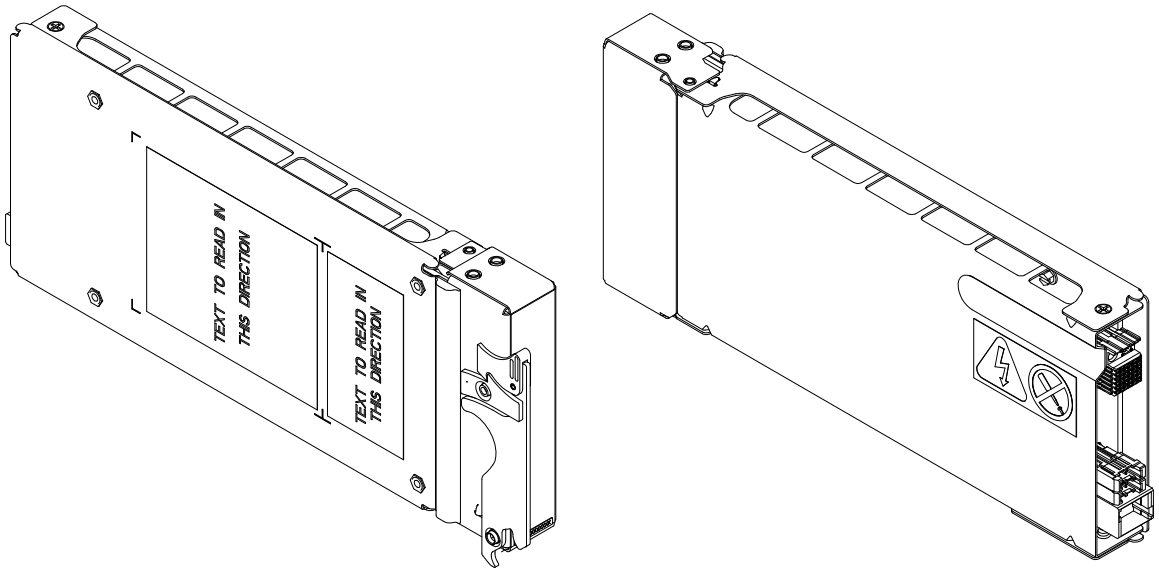

Figure 9-19- Bridge Module – Isometric Views

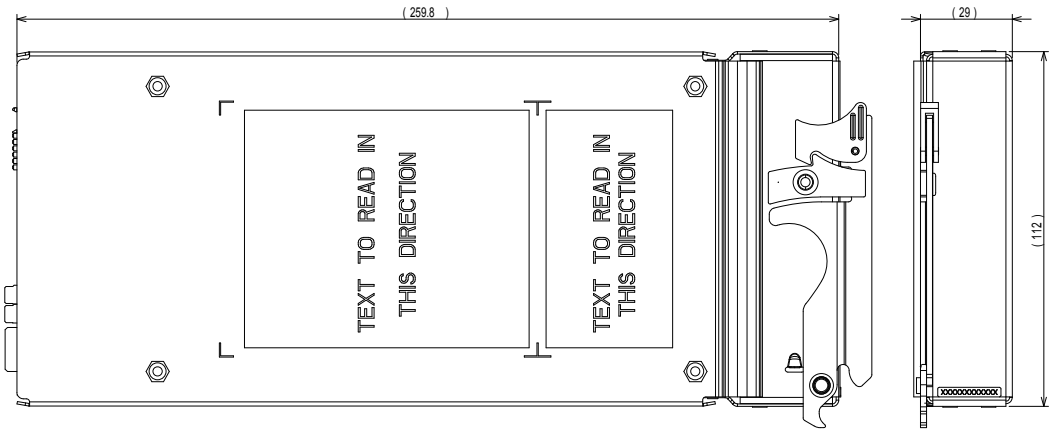

Figure 9-20- Bridge Module - Size

9.13 Bridge Switch Mechanical Design

A Bridge Module Mechanical Design Kit is available at the following URL:

http://www-03.ibm.com/systems/bladecenter/resources/openspecs.html.

This kit will provide data necessary to design the mechanical enclosure and printed circuit card for the switch module. It is recommended that the construction technique described by the design data be followed. However, it may be modified per the application. The mechanical design kit consists of a "Readme" file, a set of 3D CAD models, and PDF files, which provide a base for designing a switch module enclosure. The 3D CAD models are in Pro/ENGINEER design software, IGES, STEP, and an EMN file format. The EMN file of the printed circuit card will define the card outline, connector location, component keep-out areas and component height restrictions. The 2D drawings are provided in Adobe® PDF file format. A bill of material is included in the design kit readme file. Mechanical information in this design kit shall take precedence over the same information contained in this specification.

9.14 Bridge Module Card Outline

The Bridge Module card outline is described below. Refer to the information in the Mechanical Design Kit described above for details.

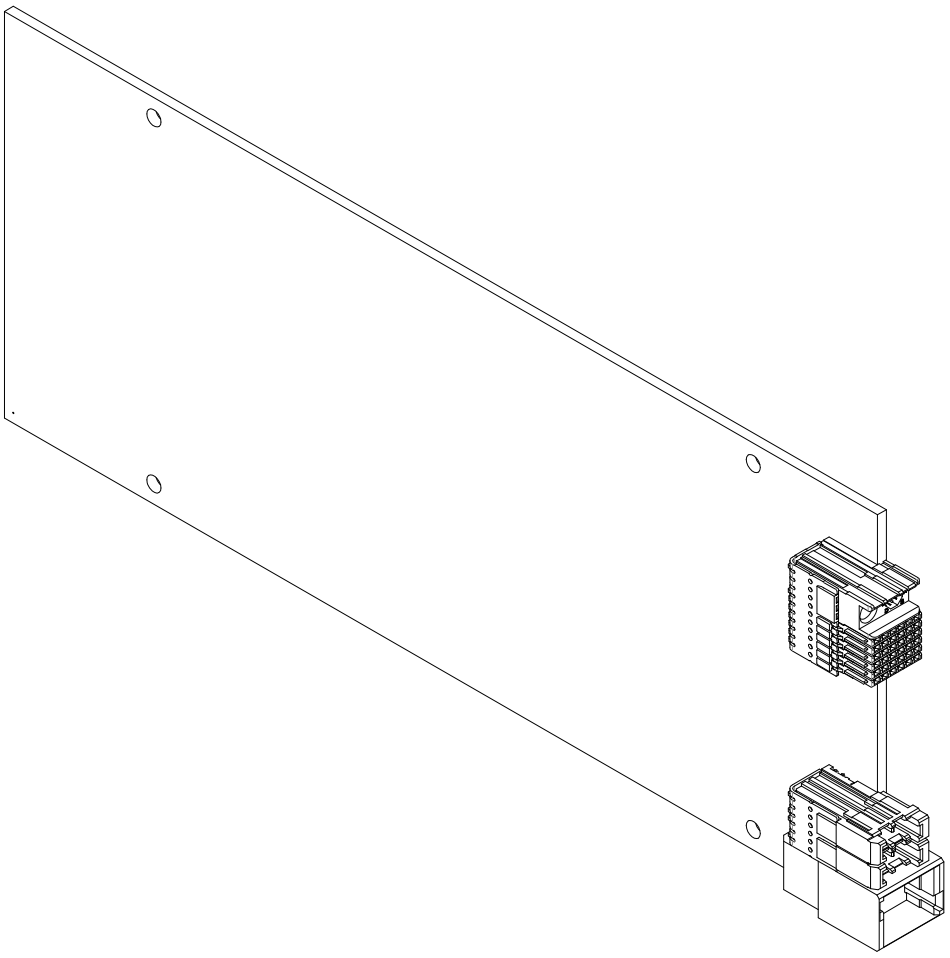

Figure 9-21- Bridge Module Card Isometric View

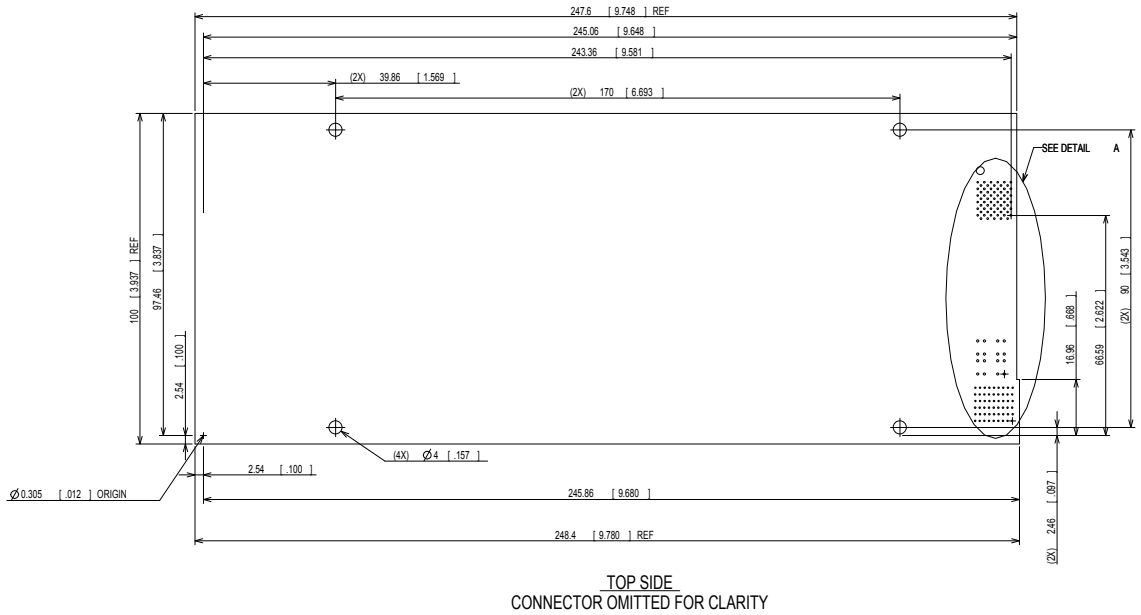

Figure 9-22 - Bridge Module Card Dimensions

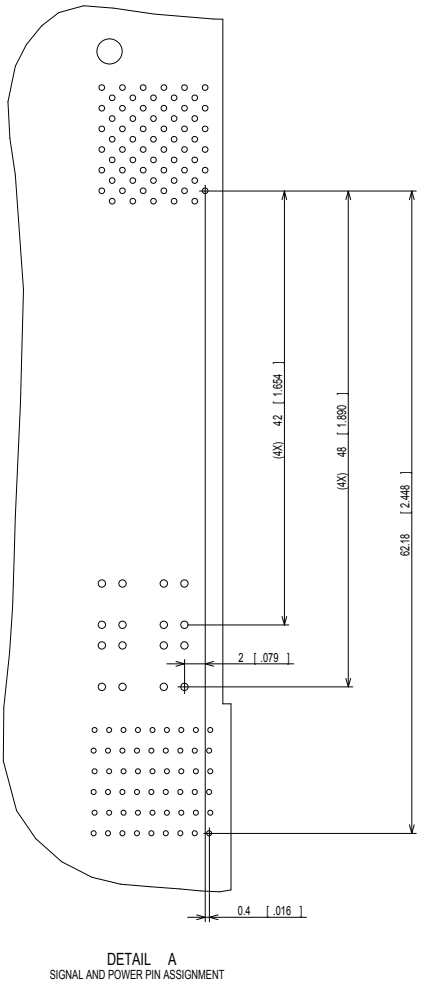

Figure 9-23- Bridge Module Card Connector Signal and Power Pin Locations

9.15 Bridge Module Material, Corrosion Resistance and Surface Conductivity

The material for the sheet metal is to be commercial quality hot dipped galvanized sheet steel with minimum spangle. Chemical treatments for corrosion resistance must be free of hexavalent chromium. Corrosion resistance must meet Class 3 requirements for salt spray testing per ASTM B117. Class 3 requires less than 5% white rust after 72 hours of testing. Additionally, good surface conductivity of the sheet steel is important to ensure proper grounding for EMC purposes. For this reason, the sheet metal must have less than 1 mΩ of surface resistance. The preferred resistance meter is a Loresta-EP CP-T360 with type BSP probes. A four point test is performed. A source for hot-dipped galvanized sheet metal, which will meet the required corrosion resistance and surface conductivity, is Yieh Phui Enterprise Co., LTD, their material code HGCC1-ZSEX. As an alternate metal, electro-galvanized sheet metal may be used. Again, corrosion resistance and surface conductivity requirements must be met. A source for this electro-galvanized sheet metal is Nippon Steel Corporation, their material code Zinkote 21-QS or Zinkote 21-QSK. Whether using hot-dipped or electro-galvanized metal, the sheet metal should have a minimum Rockwell B hardness of 55.

9.16 Reserving Label Space for End User

It is important that an adequate area is available to the end user for applying labels (e.g., asset tag). Therefore, there shall be a customer usable label area that can accommodate a minimum label size of 7mm X 40mm that is visible without removing a switch from a system and will not inadvertently block air flow. The current handle on the 1xSM, Bridge Module, and right handle on the FFB 4xSM, as described in the mechanical design kit, is designed to provide this area (see Figure 9-22). The FFA 4xSM has a larger area provided as a result from the cable strain relief.

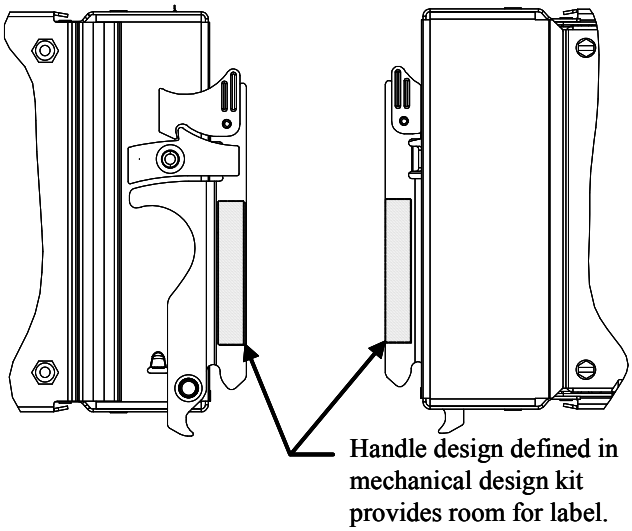

Figure 9-24 - Example of label space on 1xSM

10 Shock and Vibration Requirements

Shock and vibration test levels for switch modules are defined in this section.

10.1 Pass/Fail Criteria

The product shall be inspected for mechanical damage before and after each test. Any noticeable damage is considered a failure. The product shall be operated before and after each test to ensure it functions as designed.

10.2 Test Fixture

10.2.1 Operational Tests

For operational tests, the BladeServer chassis shall be clamped to the test table with rigid fixtures that support the chassis in a manner that simulates the support provided by the intended shipping package. Rack level operational vibration and shock testing is not performed.

10.2.2 Non-Operational Tests

- Fragility (Bare Product) Tests: the product shall be supported and clamped to the test table in a manner that simulates the support provided by the intended shipping package.
- Packaged Tests: the product shall be packaged with accessories as expected for final shipment. For vibration tests, this package should be fixed to the vibration table.
- Rack Tests: the product shall be installed in a BladeServer chassis installed in a Rack as expected for final shipment (including all required shipping brackets). The Rack shall remain attached to the shipping pallet. The pallet shall be fixed to the vibration and/or shock table in a manner that allows for minimal flexing and safe test performance.

10.3 Operational Shock and Vibration

The following operational shock and vibration tests shall be performed on a test table. The tests are not performed in a rack.

10.3.1 Operational Shock

Server on, operational shock

- Vertical Input: 30.0 G for 3ms, half-sine shock pulse
- Horizontal Input: 15.0 G for 3ms, half-sine shock pulse
- Two shock inputs in each axis, one in each direction; six total

10.3.2 Operational Vibration

Server on, operational vibration: 0.27 G RMS at 5Hz to 500Hz for 30 minutes

Power Spectral Density (PSD) for operational vibration tests is provided in Table 10-1.

Frequency	G^2 / Hz (PSD Level)
5.0	$2.0x10^{-5}$
17.0	$3.0x10^{-4}$
45.0	$3.0x10^{-4}$
48.0	$3.0x10^{-4}$
62.0	$3.0x10^{-4}$
65.0	$3.0x10^{-4}$
150.0	$3.0x10^{-4}$
200.0	$8.0x10^{-5}$
500.0	$8.0x10^{-5}$

Table 10-1 Random Vibration PSD Profile for Chassis and Switch Module Operational Unpackaged Test

10.4 Non-operational Shock and Vibration

Non-operational switch module shock and vibration test levels are defined in the sections below. Any one switch module is not required to pass every section of the shock and vibration tests. Multiple samples may be used.

Switch Module non-operational shock and vibration testing includes:

- Switch Module Fragility Tests
  - Shock (10.4.1)
  - Vibration (10.4.3)
- Switch Module installed in BladeServer chassis Fragility Test
  - Shock (10.4.2)
  - Vibration (10.4.3)
- Switch Module Package Tests
  - Drops (10.4.4)
  - Vibration (10.4.5)
- Switch Module installed in BladeServer chassis installed in a Rack Package Tests
  - Drops (10.4.6)
  - Vibration (10.4.7)

If a BladeServer chassis is not available, a rigid chassis test fixture for switch modules may be used. This fixture shall be a rigid structure designed to simulate the support and retention mechanisms of the BladeServer chassis. This structure should have a natural frequency of greater than 200 Hz. It shall provide the same guide channels, latch retention and connector system as a chassis. The signal and power connectors shall be mounted on a board or other structure that will simulate the BladeServer midplane.

10.4.1 Non-operational Fragility Shock – Unpackaged Switch Module

Unpackaged switch modules are to be tested on all six product faces, one impact per face. The shock pulse should have the following characteristics:

- Trapezoidal waveform
- 50 G's
- 4572 mm/sec (180 in/sec) ΔV

10.4.2 Non-operational Fragility Shock – Switch Module installed in an unpackaged BladeServer Chassis

The switch module installed in a BladeServer chassis is to be tested on all six product faces, one impact per face. The shock pulse should have the following characteristics:

- Trapezoidal waveform
- 25 G's
- 3000 mm/sec (118 in/sec) ΔV

Switch modules may be qualified using a rigid chassis test fixture, as described in the test fixture section (10.4) of this document, in lieu of the BladeServer chassis level test described in the section above.

10.4.3 Non-operational Fragility Vibration – Unpackaged Switch Module and Switch Module installed in an unpackaged BladeServer chassis

Fragility random vibration tests are performed in accordance with level in Table 10-2. Testing is to be performed for 15 minutes per face on all six product faces.

If the product fails during random vibration testing, additional sinusoidal vibration and dwell testing shall be used to determine weak areas of the product. The sinusoidal test shall consist of a sweep at 0.5G from 2Hz to 200Hz to determine the most dominant natural frequency then dwell at the natural frequency for 15 minutes. Once improvements are made to the design, the unpackaged random vibration tests shall be re-run to ensure compliance to the test levels.

Frequency	G^2 / Hz (PSD Level)
2.0	0.0010
4.0	0.0300
8.0	0.0300
40.0	0.0030
55.0	0.0100
70.0	0.0100
200.0	0.0010

Table 10-2 1.04 G_{RMS} Random Vibration Spectrum

10.4.4 Non-operational Packaged Drops – Packaged Switch Module

Table 10-3 lists the drop heights for specific weight ranges to be used to test packaged switch modules. Product acceleration response inside the package must be monitored on each axis during the test. The response must be lower than the unpackaged fragility acceleration target (section 10.4.1)

Orientation	Drop Height mm (inches) Packaged Weight < 3 kg (7 lbs)	Drop Height mm (inches) Packaged Weight = 4 kg (8 lbs) to 11 kg (25 lbs)
Critical Corner	1067 (42)	914 (36)
Radiating Edge	1067 (42)	914 (36)
Radiating Edge	1067 (42)	914 (36)
Bottom	1067 (42)	914 (36)

Top	1067 (42)	914 (36)
Right	1067 (42)	914 (36)
Left	1067 (42)	914 (36)
Front	1067 (42)	914 (36)
Rear	1067 (42)	914 (36)

Table 10-3 Non-operational Packaged Switch Module Drop Heights

10.4.5 Non-operational Packaged Vibration – Packaged Switch Module

Packaged random vibration tests are performed in accordance with Table 10-4.

Orientation	G_{RMS}	Duration (minutes)
Top or Bottom	1.04	15
Right or Left	1.04	15
Front or Rear	1.04	15

Table 10-4 Non-operational Packaged Switch Module Vibration

The random vibration test spectrum for non-operational unpackaged testing shall be in accordance with Table 10-2.

10.4.6 Non-operational Rack Drops – Switch Module installed in a BladeServer chassis installed in a Rack

Table 10-5 lists the non-operational rack drop height/shock test levels for a switch module installed in a BladeServer chassis installed in a Rack.

Drop Height mm (in.)	Wave Form	Target ΔV mm/sec (in./sec)	# of Drops	Drop Description
152 (6)	Half Sine	1,730 (68)	2	Bottom Face (Shipping Orientation)
51 (2)	Half Sine	1000 (40)	10	Bottom Face (Shipping Orientation)

Table 10-4 Non-operational Rack Shock Test Levels for Chassis with Blades and Switch Modules Installed

10.4.7 Non-operational Rack Vibration - Switch Module installed in a BladeServer chassis installed in a Rack

The non-operational rack vibration test shall be performed only on the bottom face (shipping orientation) at 1.04 G_{RMS} as described above in table 10-2. The test duration is 15 minutes.

10.5 Telecom Environment

The following telecommunication listings must be supported by the switch server design. The host chassis in a telecom environment will be either the Telco 8U BladeServer or Telco 12U BladeServer chassis.

The BladeServer-T and BladeServer-HT chassis have been designed and tested for compliance to NEBS Level 3, Earthquake Zone 4 criteria as defined by Telcordia SR-3580, as well as ETSI

criteria as defined by various documents released by the European Telecommunications Standards Institute.

NEBS Level 3, Earthquake Zone 4 is considered the minimal level of environmental compatibility to provide maximum assurance of network reliability within the CO environment even under harsh and catastrophic conditions. The Level 3 requirements are based on the following documents:

- Telcordia GR-63-CORE; Physical Protection, Issue 3
- Telcordia GR-78-CORE; Physical Design and Manufacture of Telecommunications Products and Equipment, Issue 1
- Telcordia GR-1089-CORE; Electromagnetic Compatibility and Electrical Safety, Issue 4

Telcordia NEBS standards documents may be purchased from the Telcordia Information Superstore at http://telecom-info.telcordia.com/site-cgi/ido/index.html.

For compliance to European Telecommunications Standards, the following ETSI document should be consulted (may be freely downloaded from http://www.etsi.org):

- **ETSI 300 386 V1.3.3 (2005-04) –** Electromagnetic compatibility and Radio spectrum Matters (ERM); Telecommunication network equipment; ElectroMagnetic Compatibility (EMC) requirements

11 Firmware Upgradeability

The firmware for the Switch Module has the following upgradeability requirements:

- Field upgradeable
    - Field upgrade download time < 5 minutes
    - Field upgrade activation time < 60 seconds
    - Switch management interface should provide status and updates of download and activation process.
- Must be able to reflash firmware even if failure of previous flashing attempt
- Must be supported through various interfaces: Telnet, SSH, Web Server, SNMP and Switch Management Standalone Application. Various methods to upload the firmware to the SM must be provided (should include TFTP and FTP).
- Switch Module SW must update it's VPD 'Code Version' data field after flash is complete and the firmware is activated (refer to the BladeServer Base Specification for VPD for details)
- Ability to distinguish between current and backup firmware versions.
- Newer firmware should work with previous configurations (i.e. the customer will not be taken back to a default configuration as a result of updating the firmware)

12 Agency Compliances

12.1 Restriction of Hazardous Substances (RoHS)

1X and 4X switch assemblies including the mechanical enclosure and the assembled switch card must comply with Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

12.2 Enterprise Server Requirements

The following safety and EMC/EMI certification listings must be supported by switch module design.

Safety Certifications

- US: UL 60950-1, 3rd Edition. Listed Accessory Report
- Canada: CSA C22.2 No. 950 or 60950
- Germany: TUV/VDE IEC 950/EN 60950
  (TUV component report & IEC60950 CB Report and Certificate)
- NOM (Mexico - Safety)

EMC/EMI Certifications

The Switch Module must meet all applicable world wide Class A EMC requirements (-6dB margin is highly recommended).

- FCC - Title 47 CFR Part 15 Subpart B
- Canada - ICES-003
- Australia/New Zealand - C-Tick - AS/NZS 3548:1995, Am.1:1997, Am.2:1997
- CE Mark - EN55022:1998 and EN55024:1998
- VCCI - Japan VCCI V-3/2000.04
- MIC Notice No. 1996-78 (Korea)
- GOST 29216-91 (Russia)
- CISPR 22 Class A
- Taiwan BSMI

12.3 Telecom Industry Standards Requirements List

The following telecommunication listings must be supported by switch module design. Vendor is responsible for obtaining copies of Telcordia and ETSI documents and ensuring design for compliance.

- **Telcordia GR-63-CORE, Issue 3 - NEBS™ Requirements: Physical Protection**
  - NEBS Level 3 per SR-3580, Issue 2 – NEBS™ Criteria Levels
  - Earthquake Zone 4
- **Telcordia GR-78-CORE, Issue 1** – Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment
- **Telcordia GR-1089-CORE, Issue 4** – Electromagnetic Compatibility and Electrical Safety – Generic Criteria for Network Telecommunications Equipment
  - Including Section 4.5.9 Intra-building lightning surge (E/N ports)
- **Labeling requirements**
  - **Telcordia GR-383-CORE, Issue 3** – COMMON LANGUAGE® Equipment Codes (CLEI™ Codes)—Generic Requirements for Product Labels
    - **Type M label, recommended format shown in Figure 7-7**
- **NEBS requirements for fiber optic components (where applicable):**
  - **Telcordia GR-468-CORE, Issue 2** – Generic Reliability Assurance Requirements for Optoelectronic Devices Used in Telecommunications Equipment
  - **Telcordia GR-326-CORE, Issue 3** – Generic Requirements for Singlemode Optical Connectors and Jumper Assemblies
  - **Telcordia GR-20-CORE, Issue 2** – Generic Requirements for Optical Fiber and Optical Fiber Cable
- **ETSI 300 386 –** Electromagnetic compatibility and Radio spectrum Matters (ERM); Telecommunication network equipment; ElectroMagnetic Compatibility (EMC) requirements
  - EN 300 386 V1.3.3 (2005-04)
- **ETSI 300 019** – Environmental conditions and environmental tests for telecommunications equipment;
  - ETS 300 019-2-1: Storage
    - 1.2: Weather protected, not temperature-controlled storage
  - ETS 300 019-2-2: Transportation
    - 2.3: Public transportation
  - ETS 300 019-2-3: Stationary Use at Weather protected Locations
    - 3.1E Temperature-controlled locations, Exceptional Operating Conditions
- **Carrier Checklists**
  - Telecommunications Carrier Group NEBS Checklist
    - VZ.NEBS.TE.NPI.2004.015
    - http://www.verizonnebs.com
  - SBC (AT&T) Checklist, Issue 8a (CO-Level 3)
    - SBC-TP-76200 11092005.doc
    - https://ebiznet.sbc.com/sbcnebs
  - AT&T Network Equipment Development Standards - NEDS
    - AT&T NEDS 9069 v5.00
  - Verizon NEBS Clarification Document
    - SIT.NEBS.RQS.NPI.2004.019
    - http://www.verizonnebs.com

Note: SBC acquisition of AT&T will result in an integration of the two respective carrier checklists into a single set of carrier requirements. Vendors are encouraged to check with AT&T to keep apprised of pending changes.

13 Switch Module Protect Mode and Switch Stacking Architecture

The intent of this architecture is to describe BladeCenter Switch Module behavior for both Switch Protect Mode (PRM) and Switch Stack Mode (STM) architecture. Both PRM and STM will allow for a switch module to enter into a mode in which the level of MM control of the SM will be reduced from what is currently defined in this document. When a SM had entered into PRM and/or STM the chassis administrator will lose the ability to perform certain BladeCenter specific control actions that would normally affect the SM configuration. These modes allow for separation of BladeCenter network and chassis administration such that the network administrator does not need to be concerned that the chassis administrator may have direct control of key functions that would normally disrupt critical switch module operations.

The PRM architecture allows for full control by the chassis administrator to set a chassis policy for the SM bay such that the MM will signal the SM permission to enter into PRM. Once the SM has been granted permission by the chassis administrator to enter into PRM then the network administrator for a SM can enable PRM mode on the SM. As described in further detail below, once the MM grants permission to the SM via the PRM protocol then the network administrator will have control of various PRM functions and the chassis administrator will loose control of those same functions. Once the SM is in PRM control of these functions may not be given back to the chassis administrator unless a network administrator permits or cedes control back to the chassis administrator. In addition, functions normally provided by the chassis administrator such as a reset-to-defaults may no longer be performed by the chassis administrator. Therefore, if the network administrator loses network access to perform this function, physical access to the SM may be required using software tools and connection methods (ex. serial port) unique to that vendor.

In addition to PRM, a new BladeCenter SM feature called ‘Switch Module Stacking’ provides for a method that several SMs can be interconnected (with or without an external cable) to allow for aggregation of bandwidth and management for the members of the stack. This SM feature is being provided for customers that need network redundancy and availability for critical applications. Switch Module Stacking is supported in BladeCenter by a SM implementing the STM architecture described in this document. To prevent a chassis administrator from affecting an SM in STM, the SM must enter into a form of PRM behavior to ensure there is no disruption by the chassis administrator, which affects the SMs that make up the switch stack.

As described above both PRM and STM build off similar notions but are very different in one key attribute. In PRM, the chassis administrator must first grant the SM permission to enter into PRM behavior and then the SM must signal the MM that PRM has been entered. In STM the SM is allowed to enter into PRM behavior without the chassis administrator having explicitly granted permission to do so and then the SM must signal the MM that both PRM and STM has been entered. STM mode can be entered whenever two or more SMs with stack mode capability are plugged into one or more BladeCenter chassis independently of any chassis administrator control. STM provides for a ‘dynamic’ PRM and therefore the chassis administrator’s ability to control certain functions of the SM can asynchronously change as a SM enters into or exits from a switch module stack.

Since STM architecture is built on some key features of PRM architecture this document is organized to first describe the PRM architecture and then discuss the differences with respect to the STM architecture.

13.1 PRM Functions

When the PRM[3] protocol has been completed between the MM and the SM, the chassis administrator will not be allowed to alter various configuration settings[4] of the SM depending on the amount of control ceded to the SM by the MM as described below. MM Permission bits and SM control bits for the various sub-functions of PRM are provided in VPD offer the chassis and network administrators the flexibility to set the granularity to which the MM can control the SM module or conversely how the network administrator wishes to control the SM. The MM permission sub-function bits permit the SM to enter Protect Mode when any of the PRM sub-function bits in the VPD fields labeled VPD.MM_PRM_Permission(x) are set to one. An SM is considered to be in Protect Mode (PRM) when any sub-function bits are set to one in VPD field labeled VPD.SM_PRM_Control(x).

All SMs shall ship from the factory with PRM mode disabled (Non-volatile storage is cleared). A chassis supporting the PRM feature shall have the requirement that both the MM and the SM shall both support PRM mode before the SM can enter PRM mode.

The proper functioning of PRM requires a firmware co-requisite, which results in both the MM and the SM supporting this architecture. Irregular behavior may occur when an SM is in PRM and is operated in a chassis, which contains a MM that does not support PRM. This may occur when the FW on a MM is back-leveled or when a SM is moved into a chassis in which the MM does not support the PRM. This document mandates that the SM shall detect and report this condition.

Once the SM is in PRM, services provided by the chassis administrator such as reset-to-default may no longer be available and if the network administrator can not reconfigure the SM for any reason physical access to the SM may be required using software tools and connection methods (ex. serial port) unique to that vendor.

The MM will inform the SM of the current chassis PRM in affect. When both the MM and the SM are in PRM the MM will prevent all users at any authentication level from changing the state of the SM (the MM will not issue I2C commands) which would conflict with the current chassis PRM policy. The MM is allowed to change the chassis PRM at anytime as long as it does not reclaim function already ceded to the SM as specified in VPD.SM_PRM_Control(0:15). If the SM is not in PRM or the bay is empty then the MM can freely increase or decrease the level of PRM. The SM is allowed to change a SM PRM control setting at anytime as long as the MM has set the bit in VPD.MM_PRM_Permission(0:15) and therefore has already ceded control to the SM.

PRM for each SM in the chassis may be set on a bay basis and will be managed as a bay configuration attribute by the MM. If the SM exceeds the PRM granted to it by the MM (a mismatch in the permission and control bits) then the MM must report this configuration error to the chassis administrator and the SM must report this error to the network administrator. Reasons for the SM to exceed the level of PRM allowed by the MM may be due to the MM discovering a new SM in the chassis and that SM has already been configured at a higher PRM level. For example, if the MM has not ceded control of the IP address change mechanism to the SM then the SM shall not prevent the MM from configuring the IP address of the SM control point with the following exception. If the SM is in this mode due to a non-volatile storage indication saved when a MM authorize the SM[5] to enter this mode then the SM by definition shall not allow the MM to change the IP address of the SM control point.

[3] See 13.1.2.
[4] See VPD.MM_PRM_Permission
[5] For example, the SM was in a bay that ceded control of the IP address change to the SM and has been moved to a bay in which the control of the IP address has not been ceded.

The SM must detect when the MM changes a CR or ECR bit that is protected by the SM[6] and issue a configuration error to the SM network manager indicating that the chassis administrator has attempted to configure the SM and optionally indicate this is possibly due to a back-level MM firmware that does not support PRM. The request to change the configuration of the SM shall be ignored by the SM in as much as the configuration change shall not occur. Specifically in the case when the MM attempts to change the SM IP address configuration and the MM has previously ceded control to the SM (VPD.SM_PRM_Control(10)=1b) then the SM shall prevent the normal SR(2) response. This will allow the MM to detect and indicate the failure to change the IP address.

As mentioned earlier, the SM is considered in PRM mode when SM's NVRam and VPD.SM_PRM_Control(0:15) are updated. When bits 3, 4, 6 or 10 are set in VPD.SM_PRM_Control() the control for these functions has been ceded to the SM. The SM may remember this state across power cycles by writing information in private non-volatile storage (SM NVRam) in the SM. In addition, once the MM cedes control of a PRM sub-function to the SM the SM shall ensure that the MM can take no action which allows the MM to affect control of that sub-function. Returning control back to the chassis administrator is controlled by the network administrator.

13.1.1 PRM Mode Granularity

Understanding the ability of the MM to affect the SM configuration is key to PRM behavior. The granular control ceded to the SM under this architecture is offered for future flexibility. Some implementations of the MM may not turn on any PRM permission bits or turn on a subset of bits or enable all of the bits thereby ceding control to the SM.

There are three facilities that inform the SM of the configuration set by the chassis administrator; the I^2C Control Register (CR), the I^2C Extended Control Register (ECR) and various VPD fields which provide the parameters needed for each function. The summary of the I^2C registers are as follows:

Control Registers
CR(7): SR Diagnostic wrap.
CR(6): Revert to factory default.
CR(5): Reserved set to "0".
CR(4): Enable all external Switch Module ports.
CR(3): Enable SM configuration via external and internal SM ports.
CR(2): A "0" to "1" transition in this position will reset Switch MM ENET port 1.
CR(1): A "0" to "1" transition in this position will reset Switch MM ENET port 0.
CR(0): A "0" to "1" in this position will power on the Switch Module.

Extended Control Registers
ECR(2): SM control point IP Acquisition Method (static/DHCP) and Static IP Address/Subnet/Gateway assignment
ECR(0:1):Extended Diagnostic Control encode

This architecture does not alter the definition or behavior of the SR and ESR registers. Therefore, PRM mode shall not affect the behavior of the SR and ESR registers.

[6] MM has previously ceded control to the SM in this or another chassis

13.1.2 PRM Protocol

The steps needed to put an SM into PRM mode, change the SM to a greater or lesser level of PRM mode, power on in PRM mode or remove PRM modes are described below.

Some of the fundamental mechanisms used for PRM control are:

1. The MM can detect the PRM mode capabilities of the switch by reading VPD.SM_Capabilities(16:31) in block 1 of VPD. This field shall be set by the SM prior to exiting POST complete (SR(6) transitions from 0 to 1).
2. The SM can detect the PRM mode capabilities of the MM by reading VPD.MM_Capabilities(16:31) in block 2 of VPD. This field will be valid prior to the MM issuing a power on sequence to the SM (CR(0) transitions from 0 to 1)
3. The SM can only transition from not being in PRM to being in PRM when the MM has set at least one of the VPD.MM_PRM_Permission(0:15) sub-functions bits in block 2 of VPD.
4. The SM will indicate control of one of the PRM sub-functions that the MM has granted permission for by setting a bit in the VPD.SM_PRM_Control(0:15) in block 1 of VPD. This field shall be set by the SM prior to completing POST (i.e. SR(6) transitions from 0 to 1).
5. The POST complete bit (SR(6)) is used as the PRM signaling mechanism between the SM and the MM.

Important note: As noted above the SM will use SR(6) as the signaling method to the MM. The transition time on the bit from "1" to "0" to "1" must be a minimum of 5 seconds.

Additional behaviors for SM PRM control:

1. The SM is allowed to change the SM PRM control bits at anytime as long as the MM has given permission and ceded control to the SM as specified in VPD.MM_PRM_Permission(0:15). The SM shall not allow a change to the SM PRM which exceeds the PRM level specified in VPD.MM_PRM_Permission(0:15). This field shall be set by the SM prior to exiting POST complete (SR(6) transitions from 0 to 1). The SM must transition SR(6) from 0 to 1 to signal the MM that the SM has changed its PRM state.
2. The SM can reduce or return to a non-PRM mode at anytime by informing the MM of the change using VPD.SM_PRM_Control(0:15) and signaling the MM via SR(6) transitioning from a 0 to 1 causing the MM to initiate a read to VPD.SM_PRM_Control() to obtain the new PRM level. At the time VPD.SM_PRM_Control(0:15) is written the SM cedes back control to the chassis.
3. The SM shall allow the MM to change the configuration for any sub-function which is not active in VPD.SM_PRM_Control(0:15) and signaled to the MM via SR(6) transitioning from 0 to 1. For example, when VPD.SM_PRM_Control(6)=0b then the SM shall not prevent the MM from configuring the SM to factory defaults via CR(6).
4. VPD.SM_PRM_Control and SM NVRam shall be kept in sync by the SM. This will allow the SM to accurately report the PRM mode of the SM as soon as the SM is plugged into a chassis and prior to PD2 becoming active. The SM should atomically write VPD.SM_PRM_Control and SM NVRam only when
    a. SR(6) = 0b and CR(0) =1b (initialization in progress)
    b. Or 250 ms prior to SR(6) transitioning from a 1 to 0 and CR(0) = 1b.

    Note: Some SM implementations prefer to update VPD.SM_PRM_Control and SM NVRam prior to SR(0) transitioning low because this is when the new configuration is applied and defines the start of the SM reset process. While the SM implementation should write VPD.SM_PRM_Control and SM NVRam atomically the updates to each facility should occur

as close in time as possible. An unexpected loss of power in the chassis during the window between a write to each of these facilities would cause these facilities to differ on the next power on reset of the SM causing the MM to detect one PRM mode and the SM another.

Described below in Figure 13-1 - I2C Exchange is a typical case when a PRM capable SM is discovered by the MM and subsequently powered on. Figure 13-1 also describes how a network administrator request to change the PRM level is communicated to the MM.

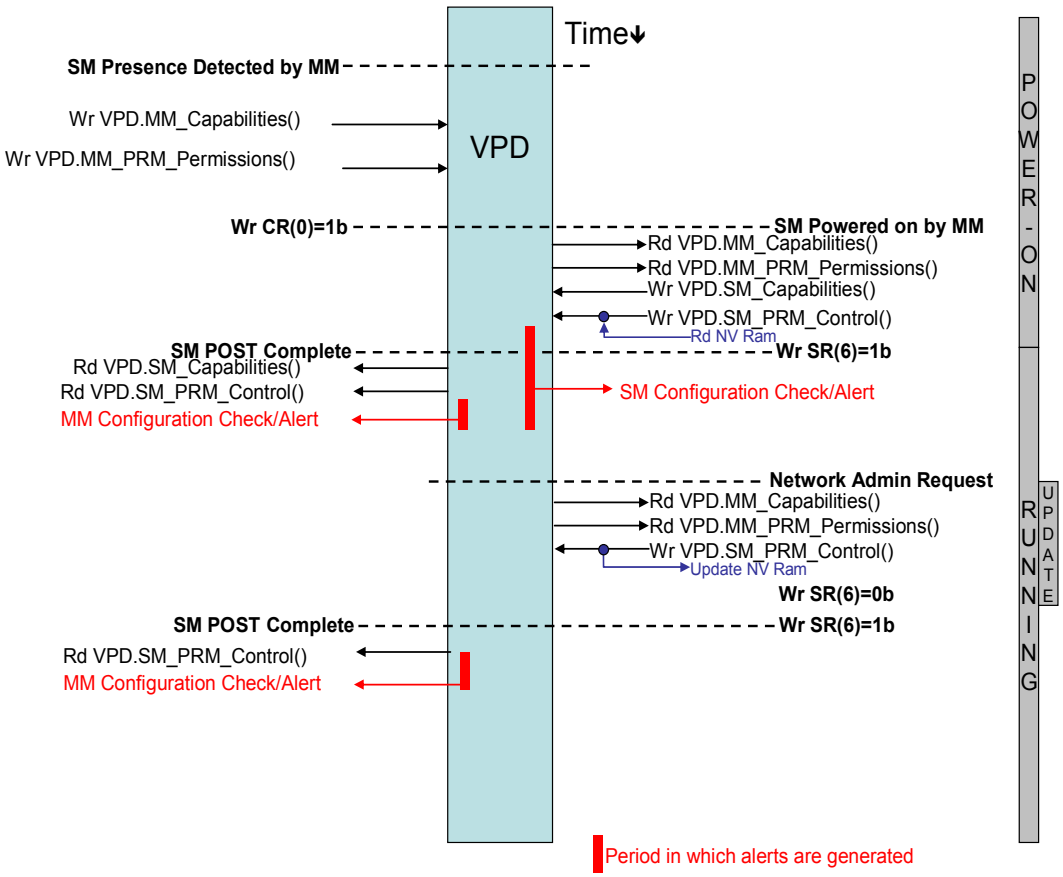

Figure 13-1 - I2C Exchange

1. When the MM detects SM presence the MM will write:
   a. The capability of the MM to manage protect mode via VPD.MM_Capability(1)
   b. The PRM permissions for this SM bay via VPD.MM_PRM_Permission()
2. The MM will them power on the SM via CR(0) transitioning from a 0 → 1.
3. Prior to the SM signaling POST complete the SM will:
   a. Read the PRM capabilities of the MM via VPD.MM_Capabilities(1)
   b. Read the PRM permissions of the SM bay via VPD.MM_PRM_Permissions(0:15) set by the MM
   c. Write the PRM capabilities of the SM via VPD.SM_PRM_Capabilities(16:31)
   d. The SM signals the MM as to the specific sub-functions that the SM will take control of via VPD.SM_PRM_Control(0:15). This value may or may not be saved in the NVRam of the SM,

4. The SM will signal POST complete when SR(6) transitions from a 0 to 1.
    a. The red bar labeled SM configuration Check/Alert in Figure 13-1 indicates that the SM should report a mismatch to the network administrator if the SM PRM level is greater than the MM PRM. The method of reporting back to the network administrator is outside of the scope of this document.
5. Also shown in Figure 13-1 is the ability of the network administrator to update or change the PRM level of a SM that is limited by the permissions granted by the MM. Assume the network administrator desires to change the current PRM level of the switch (increase or decrease in PRM). After the network admin informs the SM of the new PRM state request, the SM must check to determine if this is an increase in PRM (MM allowed less SM PRM configuration control) or a decrease in PRM (MM allowed more SM PRM configuration control).
    a. If this is a decrease in PRM function then the SM will accept the decrease.
    b. If the network administrator desires to increase the PRM function then the SM must check the current PRM level of the chassis by testing VPD.MM_PRM_Permission(0:15) in VPD and the new requested SM PRM level request by the network administrator.
        i. If the chassis PRM level does not allow the control of any PRM sub-function as described in VPD.MM_PRM_Permission(0:15) then the SM shall reject the request from the SM network administrator.
        ii. If the MM PRM permission allows for the corresponding increase in PRM then the SM shall write the new PRM mode into NVRam and VPD.SM_PRM_Control(0:15) and then set SR(6) to 0 and then set SR(6) to 1 to initiate the notification to the MM.

13.1.2.1 Mismatch in PRM level

In the case where a SM is physically moved from one switch bay to another or when the MM's chassis policy for a switch bay mismatches in the PRM level as detected by the SM, then the resultant behavior by both the MM and SM must be understood and followed.

This mismatch can only happen at power-on of the SM since the SM rejects all attempts to enable a PRM sub-function greater than the sub-functions set in the VPD.MM_PRM_Permission(0:15) by the MM.

The red blocks in Figure 13-1 describe when the SM and MM should report this configuration failure to the network administrator and chassis administrator. Since SMs can be configured in one chassis and moved to another chassis then this error is expected to occur. The SM's NVRam may save the PRM state of the SM across power cycles. The SM may allow the NVRam setting to take precedence over the chassis PRM policy and if this occurs the SM will ignore the PRM sub-functions and therefore certain I2C commands from the MM. If the MM is at a firmware level that supports PRM then the MM will report the mismatch to the chassis administrator. Regardless of the MM firmware level the SM must always report this mismatch to the network administrator.

13.1.2.2 VPD Access

Both the MM and the SM must perform atomic writes/reads to VPD.MM_PRM_Permission(0:15) and VPD.SM_PRM_Control(0:15) to prevent the MM or SM from reading a partially written VPD field.

The MM can set VPD.MM_PRM_Permission(0:15) at any time. If a change to VPD.MM_PRM_Permission(0:15) is in flight then the SM may not actually be responding to the new chassis policy but to the old policy. If the network admin changes the PRM of the SM at the same time that the MM is changing the chassis policy[7] then it is acceptable for the SM to respond to the network administrator using either the old or new chassis policy. As mentioned earlier, both the MM and the SM will report a configuration error when either detect a difference between chassis PRM and SM PRM whenever either policy changes. To ensure the chassis PRM configuration error is reported to both the chassis and network administrators the MM and the SM shall both compare the chassis policy (VPD.MM_PRM_Permission(0:15)) to the SM mode (VPD.SM_PRM_Control(0:15)).

13.1.3 PRM Recommendations on SM NVRam Handling

The SM is responsible to save PRM mode and sub-function information across power cycles. Power cycles may occur when the AC power to the chassis is cycled or a SM is unplugged from a bay in one chassis and plugged into another bay be it in the same chassis or another chassis. The SM shall ensure that VPD.SM_PRM_Control(0:15) accurately reflect the state of NVRam at all times including when PD2 is off. VPD.SM_PRM_Control(0:15) shall be written when NVRam is changed to ensure these fields are kept in sync.

13.1.4 PRM I2C Registers and VPD Field Descriptions

Below is a description of the various PRM definitions with respect to both the I^2C bus registers and VPD fields. When a SM is in PRM the MM will be prevented from affecting certain switch configuration and behaviors that are provided via the SM I^2C bus registers as a function of the control that has been ceded to the SM. Table 13-1 lists the VPD fields used in this architecture and Table 13-2 lists the detailed PRM VPD field definitions.

Note: The information in these tables is for reference purposes for the reader and for the most up to date information refer to the 'BladeServer Base Specification for VPD'.

VPD Field Name	VPD blockX:offset	Implementation	Reason
VPD_Version	block0:0x0002	VPD version must be >= 0x0104	Used to determine if the SM is at the correct VPD version to support PRM. If this is true then the SM capability field will be valid.
Code_Level_2_version	block1:0x002A	Date field of the format mm/dd/yyyy must specify a month and year after 12/2006	Used to determine that the SM has the correct VPD version(1) to support PRM is at the minimum IOM firmware version to support PRM. Note: SM will update this field to a value of month/year less than 12/06 when PRM is not supported.
SM_Capabilities	block1:0x02A0 (bits 16:31)	A bit set to 1 by the SM will indicate to the MM that the SM has the **capability** to support a given SM_PRM_Control bit. This indicates to the MM that the SM can control this function independent of the setting of the	Used to determine when the SM is at the correct VPD version level and the correct firmware level version this field will determine what PRM functions the SM supports

[7] This would be the case when the chassis administrator and the network administrator were both modifying the PRM of a bay or SM respectively within 250ms of one another.

VPD Field Name	VPD blockX:offset	Implementation	Reason
		CR/ECR bit. A bit set to 0 will indicate to the MM that this function must be controlled by the MM setting of the CR/ECR bit.	*Note: This places a requirement on the SM that this field is set to properly indicate what the capabilities of the SM are with respect to the version of firmware that is active on the SM. For example, if the SM firmware is upgraded and does not support a certain capability then as per VPD base specification a given SM capability bit must be set to zero.*
MM_Capabilities	Block2:0x02B0 (bits 16:31)	A bit set to 1 by the MM will indicate to the SM that the MM has the **capability** to support a given MM_PRM_Permision bit. This indicates to the SM that the MM will allow control of this function independent of the setting of the CR/ECR bit. A bit set to 0 by the MM will indicate to the SM that the MM does not support the capability to allow the SM to control the CR/ECR bit.	Will be set by the MM in the SM's VPD to indicate what capabilities the MM supports.
SM_PRM_Control	Block1:0x02C0 (bits 0:15)	A bit set to 1 indicates the SM currently is ignoring the setting of the MM for a given CR/ECR bit. Note: this can only happen after the appropriate MM_PRM_Permission bit has been set to 1 by the MM. A bit set to 0 indicates the MM is in control of the behavior of this bit in the CR/ECR.	When the SM at the correct VPD version level this field will determine what PRM functions the SM will support to take control of a given function away from the MM Note: Block1:0x02C0 is a 2 byte field
MM_PRM_Permission	Block2:0x02BC (bits 0:15)	A bit set to 1 indicates the MM has granted permission to the SM to ignore the setting of the given CR/ECR bit. A bit set to 0 indicates the MM has not granted permission to the SM to ignore the setting of the given CR/ECR bit.	When the SM is at the correct VPD version level this field will determine what PRM functions the MM has granted permission to the SM. Note: Block2:0x02BC is a 2 byte field

Table 13-1 PRM VPD Field Descriptions

Control Reg (x), Extended Control Reg (x) MM_Capabilities (x), MM_PRM_Permission (x), SM_PRM_Control (x) **,** SM_Capabilities (x)	**Controlled by Protect Mode**	**Definitions**
CR(0) MM_Capabilities(16) MM_PRM_Permission (0) SM_PRM_Control (0) SM_Capabilities (16)	No	MM to SM Power-on/off – this function is not available to be controlled by the protect mode architecture. MM_Capabilities (16) is set to 0 and is reserved MM_PRM_Permission (0) is set to 0 and is reserved SM_PRM_Control (0) is set to 0 and is reserved, SM_Capabilities (16) is set to 0 and is reserved
		MM to SM Ethernet port reset.– **this function is not available to be controlled by the**

CR(1:2) MM_Capabilities(17:18) MM_PRM_Permission (1:2) SM_PRM_Control (1:2) SM_Capabilities (17:18)	No	**protect mode architecture** MM_Capabilities(17:18) set to 00b and is reserved MM_PRM_Permission (1:2) set to 00 and is reserved SM_PRM_Control (1:2) is set to 00b and is reserved SM_Capabilities (17:18) is set to 00b and is reserved
CR(3) MM_Capabilities(19) MM_PRM_Permission(3) SM_PRM_Control (3) SM_Capabilities (19)	Yes	MM_Capabilities(19) informs SM if MM is capable of supporting MM_PRM_Permission (3) • A 0b indicates that the MM does not support this sub-function. • A 1b indicates that the MM does support this sub-function. MM_PRM_Permission (3) informs the SM of the current chassis policy which allows the MM to control configuration over the SM external ports and internal blade ports. • A 0b indicates that chassis policy is that the SM shall use CR(3) to determine which ports to accept management traffic (MM only or MM and SM External and Internal ports). • A 1b indicates that chassis policy is that the SM may ignore the CR(3) value. SM_PRM_Control (3) informs the MM of the current SM protect mode setting for configuration over the SM's external ports and internal blade ports. • A 0b in this position indicates that the SM shall use CR(3) to determine which ports to accept management traffic (MM only or MM and SM External and Internal ports) • A 1b in this position indicates that the SM is controlling management using the SM's external and internal ports independent of CR(3). SM_Capabilities (19) informs the MM if this SM is capable of supporting SM_PRM_Control (3) • A 0b indicates that the SM does not support this sub-function. • A 1b indicates that the SM does support this sub-function.
CR(4) MM_Capabilities(20) MM_PRM_Permission(4) SM_PRM_Control (4) SM_Capabilities (20)	Yes	MM_Capabilities(20) informs SM f this MM is capable of supporting MM_PRM_Permission (4) • A 0b indicates that the MM does not support this sub-function. • A 1b indicates that the MM does support this sub-function. MM_PRM_Permission (4) informs the SM of the current chassis policy which allows the MM to control SM external port enablement. • A 0b indicates that chassis policy is that the SM shall use CR(4) to determine to determine if SM external ports are enabled. • A 1b indicates that chassis policy is that the SM may ignore the CR(4) value. SM_PRM_Control (4) informs the MM of the current SM protect mode setting for SM external port enablement. • A 0b in this position indicates that the SM shall use CR(4) to determine if SM external ports are enabled. • A 1b in this position indicates that the SM is controlling enablement of SM external ports independent of CR(4) SM_Capabilities (20) informs the MM if this SM is capable of supporting SM_PRM_Control (4) • A 0b indicates that the SM does not support this sub-function. • A 1b indicates that the SM does support this sub-function.
CR(5) MM_Capabilities(21) MM_PRM_Permission(5) SM_PRM_Control (5) SM_Capabilities (21)	No	Reserved - this function is not available to be controlled by the protect mode architecture MM_Capabilities (21) is set to 0 and is reserved MM_PRM_Permission(5) set to 0 and is reserved, SM_PRM_Control (5) set to 0 and is reserved SM_Capabilities (21) set to 0 and is reserved
CR(6) MM_Capabilities(22) MM_PRM_Permission(6)	Yes	MM_Capabilities(22) informs SM f this MM is capable of supporting MM_PRM_Permission (6) • A 0b indicates that the MM does not support this sub-function. • A 1b indicates that the MM does support this sub-function.

SM_PRM_Control (6) SM_Capabilities (22)		MM_PRM_Permission (6) informs the SM of the current chassis policy which allows the MM to control reset to factory default. • A 0b indicates that chassis policy is that the SM shall use CR(6) to determine if SM will reset to factory default. • A 1b indicates that chassis policy is that the SM may ignore the CR(6) value.
		SM_PRM_Control (6) informs MM of the current SM protect mode setting for reset to factory default under control of CR(6) • A 0b indicates that the SM shall reset to factory default when CR(6) is set to 1 and CR(0) transitions from 0→1. • A 1b indicates that the SM shall not reset to factory default when CR(6) is set to 1 and CR(0) transitions from 0→1
		SM_Capabilities (22) informs the MM if this SM is capable of supporting SM_PRM_Control (6) • A 0b indicates that the SM does not support this sub-function. • A 1b indicates that the SM does support this sub-function
CR(7) MM_Capabilities(23) MM_PRM_Permission(7) SM_PRM_Control (7) SM_Capabilities (23)	No	MM to SM Diagnostic Wrap - this function is not available to be controlled by the protect mode architecture MM_Capabilities (23) is set to 0 and is reserved MM_PRM_Permission(7) is set to 0 and is reserved SM_PRM_Control (7) s set to 0 and is reserved SM_Capabilities (23) s set to 0 and is reserved
ECR(0:1) MM_Capabilities(24:25) MM_PRM_Permission(8:9) SM_PRM_Control (8:9) SM_Capabilities (24:25)	No	Extended Diagnostic Control - this function is not available to be controlled by the protect mode architecture MM_Capabilities (24:25) is set to 00b and is reserved MM_PRM_Permission(8:9) is set to 0 and is reserved SM_PRM_Control (8:9) is set to 0 and is reserved SM_Capabilities (23:24) is set to 0 and is reserved
ECR(2) MM_Capabilities(26) MM_PRM_Permission(10) SM_PRM_Control (10) SM_PRM_Capabilities (26)	Yes	MM_Capabilities(26)informs SM if MM is capable of supporting MM_PRM_Permission (10) • A 0b indicates that the MM does not support this sub-function. • A 1b indicates that the MM does support this sub-function.
		MM_PRM_Permission (10) informs the SM of the current chassis policy which allows the MM to control IP Acquisition. • A 0b indicates that chassis policy is that the SM shall use ECR(2) to change the IP settings of the SM control point. • A 1b indicates that chassis policy is that the SM may ignore the ECR(2) value.
		SM_PRM_Control (10) informs MM of the current SM protect mode setting for IP Acquisition under control of ECR(2) • A 0b indicates that the SM shall allow the MM to use the IP Acquisition method to change the IP settings of the SM control point when ECR(2) transitions from 0→1. • A 1b indicates that the SM shall not allow the MM to use the IP Acquisition method to change the IP settings of the SM control point when ECR(2) transitions from 0→1. Notes: • When SM_PRM_Control (10) =1b, the MM shall not set the IP address of the SM control point. Therefore, no management traffic will flow from the MM's external Management Network to the SM. Theerfore no management traffic will be targeted to the SM control point and all management traffic destined to the SM control point must come through either the SM internal blade ports or the SM external ports. • When SM_PRM_Control (10) =1b, SM must never prevent MM initiated traffic destined to the internal blade ports or blade initiated traffic destined to the MM internal port.
		SM_Capabilities (26) informs the MM if this SM is capable of supporting IP Acquisition protect mode. • A 0b indicates that the SM does not support this sub-function. • A 1b indicates that the SM does support this sub-function
ECR(3:7) MM_Capabilities(27:31)	No	Reserved fields for future expansion – these functions are not available to be controlled by the protect mode architecture.

MM_PRM_Permission(11:15) SM_PRM_Control (11:15) SM_Capabilities (27:31)		MM_Capabilities (27:31) is set to all 0's and are reserved MM_PRM_Permission(11:15) is set to 0 and is reserved SM_PRM_Control (11:15) is set to 0 and is reserved SM_Capabilities (27:31) is set to 0 and is reserved

Table 13-2 - PRM Control

13.1.5 PRM FW Level Incompatibilities

There are cases that the firmware and associated capabilities on the MM and the SM will not be at the same level of support. Additionally situations can occur when the firmware is updated after a feature has been enabled and can have residual affects due to the update to some other versions of the firmware. The updated version of the firmware may not include mechanisms to clean-up fields that by definition cannot be managed when firmware is updated. Below is the condition(s) that may occur when both the MM and SM are not at a firmware level that supports PRM.

Note: *Beginning with VPD version 0x0104 when a SM's firmware is updated there is a requirement on the SM that the VPD.SM capabilities field is set to properly indicate what the capabilities of the SM are with respect to the current version of firmware that is active on the SM. For example, if the SM firmware is upgraded and does not support a certain capability then as per VPD base specification a given SM capability bit must be set to zero.*

MM Firmware	SM Firmware	Behavior
No PRM Support	No PRM Support	PRM not supported
No PRM Support	PRM Supported and Enabled	MM will attempt to control the SM behavior and configuration. • In this case the MM is not aware if SM is ignoring control bit changes and therefore the dependency is on the SM to notify the administrator (see below). The SM will ignore all PRM functions that are enabled. The SM must signal via alerts/logs so the network administrator is aware of this condition.
PRM Supported	No PRM Support	In general MM reports no SM PRM Support. • The MM sill rely on the SM's VPD to determine both the VPD version level is less then 0x0104 or the SM code level 2 version build date information is prior to 12/2006.
PRM supported	PRM Supported	PRM supported
Notes: • The SM shall always go through initialization after the SM FW has been changed by transitioning SR(6) 0 to 1 • A SM that that reports PRM capabilities will also set the code level 2 version build date field to 12/1/06 or later. • A mismatch in PRM capabilities or settings between the MM and SM should never signal a FRU replacement.		

Table 13-3 Firmware Level Incompatibilities

The MM must have the ability to detect if the SM has the capability to support PRM. To allow the MM to detect that PRM VPD.SM_PRM_Control() field is no longer supported the SM shall perform at least one of the following:

a. Set the VPD format and VPD version to indicate a format less than 0x0104.
b. Set the code level 2 firmware date prior to 12/2006.
c. Reset the VPD.SM_Capabilities PRM bits to zero.

13.1.6 Loss of Management Interface

In PRM mode the MM can cede control of sub-functions such as the SM IP address and reset to factory defaults. When the MM has ceded control, the normal MM recovery of an incorrect configuration at the SM will no longer be available. It is a vendor responsibility to have a defined recovery procedure in place.

13.2 Switch Stacking and STM

Stacking is a network function and provides aggregation of bandwidth and management of members of the stack. This is a SM feature for customers that need network redundancy, availability and management simplicity. When a SM is participating as part of a stack of SMs one of the stack members is determined to be the 'master' of the stack while the other members are termed the 'member'(s) of the stack. Typically depending on the SM's stack implementation either:

a. All stack members may have synchronized copies of the saved and running configuration files of the switch stack. This is to insure that if the master fails the configuration in effect will automatically be used by the newly elected master.
b. An administrator may perform a SM configuration process which will designate the master and members of the stack.

Typically interconnect links will be used between SMs to allow for a SM to participate in a stack of switches. These links may attach to SMs in the same chassis, to SMs in another chassis or to an external switch. The links may be an external cable or some internal wiring utilizing the chassis midplane between SMs. Various topologies are possible to support a particular SM's implementation of switch stacking but in general this may be either a 'Ring' topology or a 'Star' topology. The topology used is outside the scope of this architecture.

When a SM is participating as a member of the stack (may be a master or a member) the SM needs to function with the same behavior as provided by a SM in PRM. This is required to insure the stack operates correctly since the master of the stack is in control of configuration and stack management. That is, the MM will not be able to control the set of sub-functions that are provided by PRM and described in the preceding sections such as external port enablement, IP configuration changes, external switch management and reset to defaults. PRM behavior is required since a MM having control of the PRM functions may cause problems for normal stack operations. Therefore when a SM is participating as a member of a stack the chassis administrator will lose direct control of the SM's PRM sub-functions.

The above brings the notion of two different protect mode behaviors. The first is 'Static Protect Mode' or static PRM which is defined by the current PRM architecture. PRM architecture requires the MM must first grant permission for the SM to enter into PRM behavior then the SM will be allowed to enable PRM control of various chassis functions and then possibly making this a non-volatile setting on the SM. The second is 'Dynamic Protect Mode'; this mode is used when PRM is not enabled at the SM but requires PRM behavior and therefore does not require the MM to grant PRM permission to the SM. The latter is covered by STM behavior.

When a SM enters into STM the settings of the sub-function bits in VPD.SM_PRM_Control will indicate which sub-function can be controlled from the MM.

The SM is responsible to enforce and provide alerts to the network administrator when a SM fails to operate correctly with the other members of the stack. Dependencies such as the same vendors SMs are interconnected, having the correct firmware and/or hardware levels on all the stack members to insure correct stack operations are all completely enforced by the SM and not the responsibility of the MM.

The SM can only enter STM if both the SM and the MM support STM as indicated in the VPD capability fields. When the MM indicates to the SM that MM is not capable of supporting stacking then the SM must not enter into a stack and therefore stacking must be disabled. The SM must alert the network administrator of this condition.

13.2.1 STM Behavior

The following additional fields will be used for the SM to indicate to the MM that it is participating as a member of a stack of SMs.

a. One bit in the VPD.MM_Capabilities field that indicates if the MM firmware supports SM stacking
b. One bit in the VPD.SM_Capabilities field that indicates if the SM firmware supports SM stacking
c. Two VPD. SM_STM_Status bits: One bit that indicates if the SM is currently participating as a member of a stack of switches (with master / member role described below). The second bit that indicate if the SM is ‘master’ or ‘member’ of the stack.

The SM’s signaling mechanism to the MM for the change of a stack membership (participating to not participating as a member) will be done via the VPD.SM_STM_Status bits in VPD in conjunction with a transition of SR(6) (POST Complete) form zero to one. At any time the SM changes stack membership an SR(6) transition is required and the VPD.SM_STM_Status bits must be set appropriately.

In all cases when the SM enters into stack the MM will alert the chassis administrator that the SM is participating in a stack and the PRM behavior is in affect.

When a SM is participating as a stack member there are 2 choices:

- In the case that a SM is not enabled for PRM the MM will not have set the VPD.MM_PRM_Permission bits. The network administrator will not be given a choice to be allowed to enter into PRM.
- In the case that a SM is enabled for PRM the MM will have set the VPD.MM_PRM_Permission bits. The network administrator will given a choice to be allowed to enter into PRM.

The MM should be able to determine at any given time if the SM is in STM, participating as part of a stack and whether it is master or member of a stack. Other stacking information such as member IDs, priority, connected stack links is beyond the scope of this architecture but is a required function on the SM as part of SM’s stack management network user interface support.

When a SM is participating as a member of a stack then depending on the setting of the IP Address Acquisition PRM control bit the MM may or may not have control of the IP address configuration of the SM.

a. If the MM does not have control then the MM will continue to provide the ‘Current IP Address’ configuration to the administrator but the IP address configuration control will be completely

managed by the stack. Therefore the 'Current IP Address' configuration VPD fields (block 1) should be updated by the SM in order to provide accurate information to the administrator.

b. If the MM continues to control the current IP address configuration then the MM will provide for configuration of the SM's IP address (utilizing the IP change protocol sequence, described in section x.y.z) and provide the current IP address configuration to the administrator.

In either case the SM and not the MM is responsible to ensure that both the chassis/network administrator understand the IP configuration values that are to be used for both the master and member(s) of the stack.

When the MM indicates to the SM that MM is not capable of supporting stacking (MM capabilities in VPD) then the SM must not enter into a stack and therefore stacking must be disabled. The SM must alert the network administrator of this condition. **Note:** If the MM had initially indicated to the SM that the firmware supported SM stacking and then the MM firmware is updated and does not support stacking, then on the next restart of the SM the SM must alert the network administrator of this condition.

In all cases when the SM enters into a stack the MM will alert the chassis administrator that the SM is participating in a stack and the PRM behavior is in affect. In addition the network administrator should also be alerted or via other mechanisms that a SM is participating in a stack.

13.2.1.1 Overall High Level Flow for SM entering into a Stack

Figure 13-2 is a high level flow of a SM that begins participation as a member of a stack.

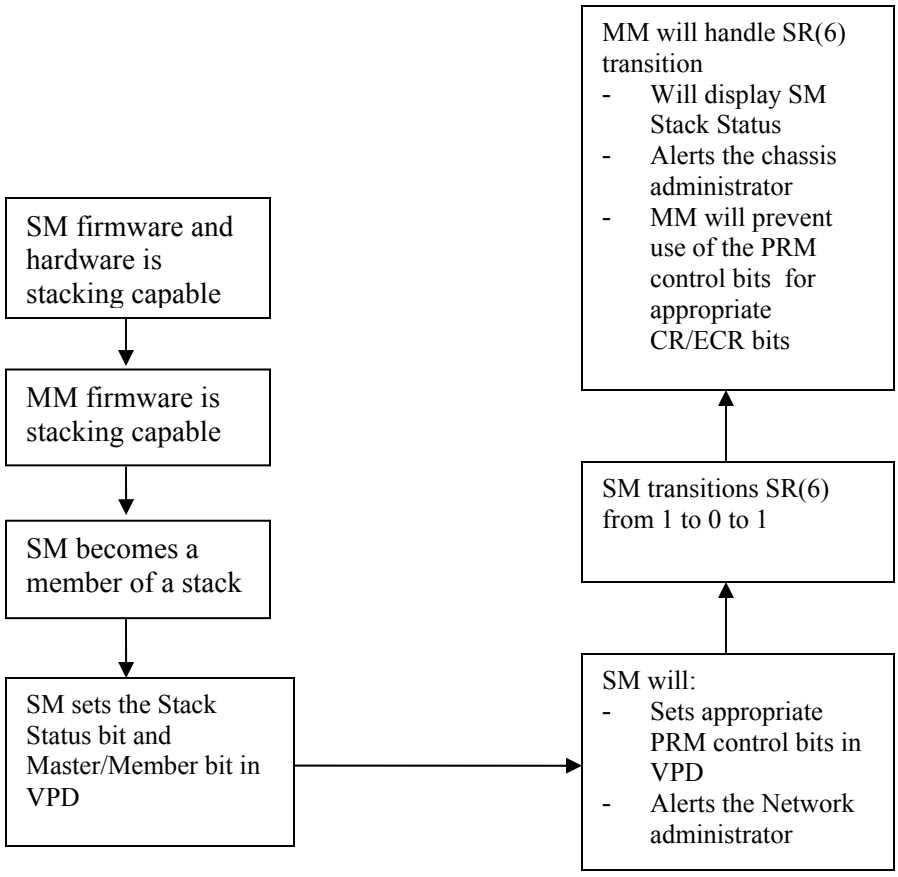

Figure 13-2 - Entering into STM

Figure 13-3 is a high level flow of a SM that is not participating as a member of a stack.

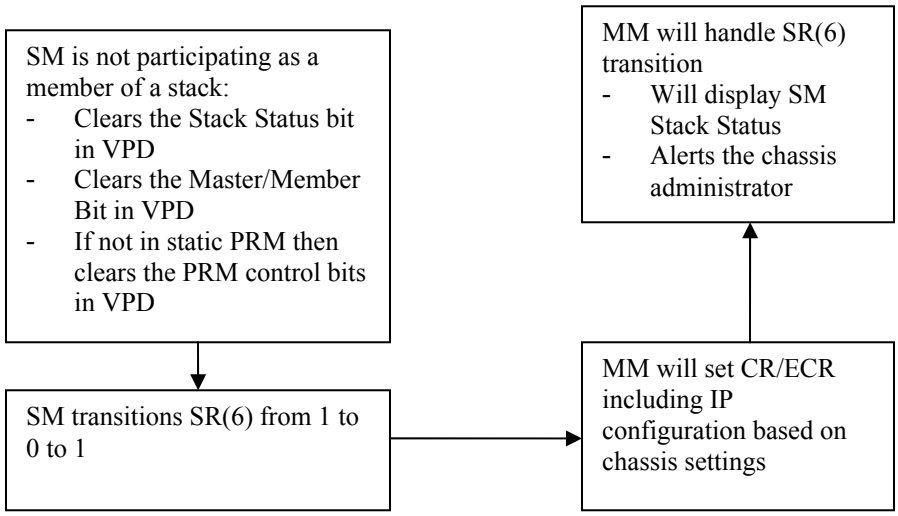

Figure 13-3 - Exiting STM

13.2.2 Dynamic PRM versus Static PRM Detection

The recognition of various cases to determine the MM and SM behavior with respect to static PRM and dynamic PRM are provided below.

1. When a SM begins participation in a stack and the MM is disabled for PRM and the SM is disabled for PRM, the SM will signal this via SR(6) transition. The MM will determine that this is a dynamic PRM case by using the following VPD fields:
    a. Reading the VPD.SM_PRM_Permission bit(s) being zero and therefore permission has not been granted.
    b. Reading the VPD.SM_PRM_Control bit(s) being one indicating the SM is in PRM.
    c. Reading the VPD. SM_Stack_Status bit is one and VPD.Stack_Master_Member_Status is set to indicate master or member role and also that the SM is part of a stack.

Note: The chassis and network administrator must be alerted that the SM is participating in a stack

2. When a SM begins participation in a stack and the MM is disabled for PRM and the SM is enabled for PRM, the SM will signal via SR(6) transition. The MM will determine that this is a static PRM case by using the following VPD fields:
    a. Reading the VPD.SM_PRM_Permission bit(s) being one and therefore permission had previously been granted for PRM.
    b. Reading the VPD.SM_PRM_Control bit(s) being one indicating the SM is in PRM..
    c. Reading the VPD. SM_Stack_Status bit is one and VPD.Stack_Master_Member_Status is set to indicate master or member role and also that the SM is part of a stack.

As specified in the PRM architecture the MM will alert the chassis administrator of the PRM mismatch at the MM and SM. In addition the chassis and network administrator will be alerted that the SM is participating in a stack.

3. When a SM begins participation in a stack and the MM is enabled for PRM and the SM is disabled for PRM, the SM will signal this via SR(6) transition. The MM will handle this and enable static PRM at the SM as follows:
    a. Writing the VPD.SM_PRM_Permission bit(s) to one therefore permission is granted to enter into PRM.
    b. Reading the VPD.SM_PRM_Control bit(s) being zero indicating the SM is not in PRM.
    c. Reading the VPD. SM_Stack_Status bit is one and VPD.Stack_Master_Member_Status is set to indicate master or member role and also that the SM is part of a stack.

As specified in the PRM architecture the MM will alert the chassis administrator that the SM is enabled for PRM and is also part of a stack. In addition, the chassis and network administrator will be alerted that the SM is participating in a stack. (Note: As per PRM architecture, the next restart of the SM will allow for the network administrator to enable static PRM at the SM.)

4. When a SM begins participation in a stack and the MM is enabled for PRM and the SM is enabled for PRM, the SM will signal via SR(6) transition. The MM will handle this as a normal PRM behavior as follows:
    a. Reading the VPD.SM_PRM_Permission bit(s) being one and therefore permission for PRM had previously been granted
    b. Reading the VPD.SM_PRM_Control bit(s) being one.
    c. Reading the VPD. SM_Stack_Status bit is one and VPD.Stack_Master_Member_Status is set to indicate master or member role and also that the SM is part of a stack.

The chassis and network administrator will be alerted that the SM is participating in a stack.

In regards to SM stacking and PRM enablement, the chassis administrator during initial chassis configuration will decide if the setting for PRM for a SM (or vendor group of SMs) should be enabled or disabled. This decision will be based on if the network administrator wants to guarantee that the MM will not be allowed to control the set of PRM functions for a SM capable of stacking independent of whether or not it is participating as a member of the stack. If the network administrator wants control at all times then PRM should be enabled. If the network administrator is comfortable with allowing the SM to only be in a dynamic PRM when the SM is participating as a member of the stack then PRM could be disabled. The optimum setting to insure there is not a conflict between the chassis administrator and the network administrator will be to enable PRM at the SM.

13.2.3 Loss of SM Management

When a SM enters into the stack it may or may be in static PRM or dynamic PRM. If in static PRM, then the external ports and external switch management will have already been enabled. The potential side effects of this are described in 13.1.6. If the SM enters into dynamic PRM, the SM is responsible for insuring that network administrator is not locked out from management of the stack and therefore must enable both external ports and external switch management.

As with PRM, the MM may lose the ability to configure and manage the IP configuration of the SM. If this is the case then all configurations must be accomplished via the SM external ports (or internal blade ports).

13.2.4 VPD Field Descriptions:

Summary of the additional VPD definitions for SM stacking support:

a. One bit in the MM_Capabilities field that indicates if the MM firmware supports SM stacking
b. One bit in the SM_Capabilities field that indicates if the SM firmware supports SM stacking
c. One bit in the 'SM_STM_Status' field that indicates if the SM is currently participating as a member of a stack of switches (with master / member role below).
d. One bit in the 'SM_STM_Status' field that indicate if the SM is 'master' (1) or 'member' (0) of the stack.

Note: The information in these tables is for reference purposes for the reader. For the most up to date information, refer to the 'BladeServer Base Specification for VPD'.

VPD Field Name	VPD blockX:offset	Implementation	Reason
SM_Capabilities	block1:0x02A0 (bit 32)	This bit set to 1 by the SM will indicate to the MM that the SM has the capability to support participation in a stack of SM's This bit set to 0 by the SM will indicate to the MM that SM does not have the the capability to support participation in a stack of SM's	When the SM is at the correct VPD version level (1) and the correct firmware level version (2) this field will determine what GM functions the SM will support
MM_Capabilities	Block2:0x02B0 (bit 1)	This bit set to 1 by the MM will indicate to the SM the MM has the capability to support stacking of SM's. This bit set to 0 by the MM will indicate to the SM that the MM does not support the capability of stacking of the SM's	When the SM that has the capability to support stacking detects that the MM does not have the capability to support stacking then SM must not allow the SM to participate as a member of a stack of switches. Information on the SM UI's should be provided to the network administrator to be made aware of this condition.
SM_STM_Status	Block1:0x02C2 (bit 0)	This bit set to 1 indicates to the MM that the switch is currently participating as a member of a stack of switches. Note: this can only happen after the MM has sets to 1 the MM Capability bit that indicates the MM supports stacking (see above). Bit 0 - This bit set to 0 indicates to the MM that the switch is currently is not participating as a member of a stack of switches.	When this bit is set to 1 then the SM must also indicate if it is 'master' of the stack or a 'member' of the stack. When bit 0 is set to 0 then bit 1 must also be set to 0.
	(bit 1)	This bit must always be set to either 0 or 1 whenever SM_STM_Status bit is set to 1 and indicates if the SM is a 'master' of the stack (1) or member of a stack (0).	

Table 13-4 VPD Field Descriptions

13.2.5 FW Level Incompatibilities

There are cases that the firmware and associated capabilities on the MM and the SM will not be at the same level of support. Additionally situations can occur when the firmware is updated after a feature has been enabled and can have residual affects due to the update to some other versions of the firmware. The updated version of the firmware may not include mechanisms to clean-up fields that by definition cannot be managed when firmware is updated. Below is the condition(s) that may occur when both the MM and SM are not at a firmware level that supports SM Stacking.

Note: *Beginning with VPD version 0x0104 when a SM's firmware is updated there is a requirement on the SM that the VPD.SM_Capabilities field is set to properly indicate what the capabilities of the SM with respect to the version of firmware that is active on the SM. For example, if the SM firmware is upgraded and does not support a certain capability then as per VPD base specification a given SM capability bit must be set to zero.*

MM Firmware	SM Firmware	Behavior
No Stacking Support	No Stacking Support	Stacking is not supported
No Stacking Support	Stacking Supported but SM not yet a member of the stack	SM is not allowed to enter into a stack. MM will control the SM behavior and configuration. The capabilities mismatch must be reported to the network administrator via an alert.
No Stacking Support	Stacking Supported and SM is currently a member of the stack	MM will attempt to control the SM behavior and configuration. • In this case the MM is not aware if SM is ignoring control bit changes and therefore the dependency is on the SM to notify the network administrator (see below). The SM must signal via alerts/logs so the network administrator is aware of this condition. [On next restart of the SM and the SM detects that the MM is not capable of stacking support. The SM must detect this condition and sends an alert to the network administrator]
Stacking Supported	No Stacking Support	SM does will not enter into stack
Stacking Supported	Stacking Supported	Stacking is supported and SM can enter into stack

Notes:
- The SM shall always go through initialization after the SM FW has been changed by transitioning SR(6) 0 to 1
- The SM shall always transition SR(6) 0 to 1 when entering or leaving the stack.
- A mismatch in stacking capabilities should never signal a FRU replacement.

Table 13-5 Firmware Level Incompatibilities

13.2.6 Switch Stacking and Post Timeout Extensions

A Switch Module that supports stacking may require additional time to complete a POST sequence. Currently the Base Specification for Switch Modules has specific timeouts for various POST diagnostic levels that are enforced by the Management Module. The Management module uses these architected times when a SM transitions from a power off state to a power on state to determine when a Switch Module POST has failed to complete in the specified timeout period. Since a SM by its nature provides the network connections to other internal and external components increasing of POST times can have adverse affects on chassis functions such as:

- Network connectivity after a SM is powered on
- When a blade PXE boots or network boots
- Blade acquiring a DHCP assigned address
- Chassis initialization after a AC cycle and restoring network connectivity

In order to allow for increased POST times new architecture is being added to allow for a SM to indicate to the Management Module a possible time extension is needed.

The SM must initialize three fields in the VPD that indicate the additional time needed for the three levels of diagnostics executed during POST. These are static fields must be initialized to the correct amount of additional time prior to the SM ever being powered on. This allows the Management Module to set the correct timeout period when the MM changes the CR(0) from zero to one. The following VPD fields have been added to support this new architecture.

VPD Field Name	VPD blockX:offset	Implementation	Reason
VPD_Version	block0:0x0002	VPD version must be >= 0x0104	Used to determine if the SM is at the correct VPD version to support PRM. If this is true then the SM capability field will be valid.
SM Capabilities	block1:0x02A0 Bit(33)	Post Timeout Extension Fields Supported o 0b=Not supported o 1b=Supported	Indicates if the SM supports Post Timeout extensions and the extension fields are valid.
POST Timeout Extension Fields	block1:0x02D8-DF	POST Timeout Extension's – Three 8 bit fields which represents the additional time added to the architected POST timeouts as specified in the Base Specification for Switch Modules. The SM is required to complete a given POST sequence after the MM signals a power on to the SM. If this time is exceeded the MM will report a POST failure. The resolution is in 1 second.. (See POST timeout extension architecture in the SM base specification) Bytes Bits (0:1) (8-15)– Standard Diagnostic Extension Time (2:3) (8-15)– Extended Diagnostic Extension Time (4:5) (8-15)– Full Diagnostic Extension Time (6:7) - Reserved Valid values are between 1 and 256 seconds (4.3 minutes).	Added for STM support to allow for increasing the POST time for various levels of diagnostics

If the Management Module detects from the SM VPD that the SM supports the 'POST Timeout Extension' capability then the MM will use the time value that is contained in the 'Post Timeout

Extension Fields' in VPD. This time value will be added to the architected Management Module Timeout Values for the various POST Diagnostic Levels as described in the Base Specification for Switch Modules. If the SM exceeds this combined time then the Management Module will generate a failure event.

Implementation Notes:

1. SM's should be designed to meet the architected POST times as specified in the Base Specifications for Switch Modules in the section on 'Management Module POST Timeout Values'. [Architecture Note: Adding the capability to extend these POST times accommodates designs that require a longer time for POST, but does not allow a implementation to simply structure their POST firmware such that the architected 'Management Module POST Timeout Values' will normally be exceeded. Therefore before exceeding the architected time limits an exception must be granted for the product design.]
2. The SM should use these fields in a way to ensure that only the smallest possible time extension is required, since longer POST times may cause the user of the chassis and MM to believe that POST may be hung or will not complete.
3. The SM implementation should not simply add a fixed time for all levels of POST diagnostics but should determine for each level of POST diagnostics if a time extension is required or not.
4. It would be expected that most SM will not require use of the POST time extension and set the 'Post Timeout Extension Fields Supported' capability bit to zero and set the 'POST Timeout Extension' fields to zero.
5. The maximum amount of extension time is limited to 4.3 minutes.

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