FPGA Attached Persistent Memory

Accelerating Applications Cost-effectively through Coherency to meet Fast & *Predictable* Data needs

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Introduction: Towards the Fast & Predictable Data

Then: Traditional and Big Data
- NAND Flash, SSD Controller, SSD, AFA Storage Systems
- DRAM: DDRx, HBMx, LPDDRx, GDDRx

Plus...

Now: Fast Data towards Predictable Data
- Persistent Memory, FPGA (Acceleration /Computation), Coherent & non-Coherent attached Memory & Storage product solutions
Critical Inflection Point based on Unpredictability & Complexity

- Traditional Data, Big Data, and Fast & Predictable Data
- New emergence of applications, use cases, and workloads (Enterprise/Cloud WLs vs AIML WLs)
- Deterministic transactions
- Compute, Storage, vs Memory-centric
- Storage vs Memory Semantics
- Heterogeneous Architecture (CPU, GPU, FPGA, ASIC)
- Interconnects (PCIe, CXL, CCIX, OpenCAPI)
- Volatile Memory (DDR, HBM, GDDR, LPDDR, SRAM)
- NAND Flash/Storage (3D NAND, SLC/MLC/TLC/QLC, Low Latency NAND)
- Persistent Memory (Optane, PCM, MRAM, ReRAM, FRAM, etc)
- Form Factors: Components, SiP, DIMM, SSD, Embedded, EDSFF
Addressing the Needs of Fast and Predictable Data

- Ever Increasing new types of Workloads
- Classification/ Recognition -> Prediction/ Decision
- Small, Random, Read
- Memory semantics
- Acceleration of Workloads (FPGA)
- Memory Hierarchy
- New types of Memory (Persistent Memory)
- Cache Coherency (Coherent Interconnect) / Standalone PCIe Interconnect

Not just about individual ingredients but **Product as Solution** to address Fast Data Needs
Benefits of FPGA; Addressing the needs for Complex Workloads

**MARKETS DEMANDING CUSTOMIZATION**

**EDGE**
Real-Time Actionable Intelligence

**NETWORK**
High-Bandwidth Aggregation and Processing

**DATA CENTER**
Managing, Organizing, and Processing the Explosion of Data

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**Flexibility**
FPGA functionality can change upon every power-up of the device

**Acceleration**
TTM & Acceleration (Compression, Dedup, Classification, Encryption, etc)

**Integration**
on-die processors, transceiver I/O’s, RAM blocks, DSP engines, and Different Memory hierarchies

**TCO**
Benefits on NRE, Design cycles, Manufacturing cycles, etc
Memory Hierarchy for FPGA; Addressing Different Usage Needs

FPGA Memory & Storage Hierarchy Building Blocks

- **On-Chip Memory**
  - Highest BW and Power Efficiency

- **In-Package Memory**
  - High Bandwidth, Density

- **On-Board**
  - Flexibility, Density, Speed, Persistency

**Building Blocks**
- 2D, 3D NAND Flash (Storage Block)
- DDRx
- QDR, RLDRAM
- HBMx
- eSRAM
- M20K
- MLAB
FPGA + Persistent Memory (PMEM) for Fast & Predictable Data needs

<table>
<thead>
<tr>
<th>Latency &amp; BW Benefits</th>
<th>FPGA+ PMEM</th>
<th>Values</th>
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<tr>
<td>Media</td>
<td>Persistent Memory (i.e. Optane)</td>
<td>Memory access with persistency</td>
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<td>Memory I/O</td>
<td>DDR I/O</td>
<td>Higher I/O pin speed</td>
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<td>I/F</td>
<td>PCIe, Coherent I/F (i.e. CXL or others)</td>
<td>Coherent attached</td>
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<td>Capacity</td>
<td>FlexScale (small to large capacities)</td>
<td>Capacity Scaling</td>
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<tr>
<td>FF</td>
<td>AIC + DDR DIMM slot, On-board</td>
<td>FF Flexibility</td>
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<tr>
<td>Latency</td>
<td>Low</td>
<td>Transaction commit</td>
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<tr>
<td>BW</td>
<td>High</td>
<td>Performance</td>
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With FPGA Acceleration!
Addressing Fast and Big Data needs through Accelerated Coherent Memory Expansion

<table>
<thead>
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<th>Coherent Memory Expansion</th>
<th>Accelerated (AFU) + Coherent Memory Expansion</th>
<th>Persistent Memory over Fabric</th>
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<td><strong>Larger Workloads</strong></td>
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<td>4TB+ capacity support per Device</td>
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<td><strong>TCO Reduction</strong></td>
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<td>Consolidation of different Memory and Storage tiers</td>
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<td><strong>Performance for large data sets</strong></td>
<td>Memory transaction vs Block access/transaction</td>
<td>Accelerate big data workloads</td>
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<tr>
<td>Enable Coherent memory expansion and leverage FPGA Memory Tiers</td>
<td>Enable in-line encryption, compression, analytics or other AFUs</td>
<td>Scalable, Shared Memory</td>
</tr>
<tr>
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<td>FPGA’s Memory locality access over Fabric, scalable memory pool</td>
</tr>
</tbody>
</table>
Coherent FPGA + PMEM Enables Variety of Use Cases

Different Coherent Topologies

Accelerated Coherent Memory Expansion
In-line acceleration to/from PM as coherent memory

Coherent Memory Hierarchy Expansion
FPGA as memory controller for multiple memory tiers, enabling both capacity and BW/latency.

Persistent Memory over Fabric

Host Server

Switch
Data Acceleration through minimal data movement & Memory semantics

1. Minimize Data Movement from Storage to Memory through maximizing DRAM footprint - best performance for high SLA workloads
2. Dramatically increase over memory footprint and reduce Storage footprint
3. Smart caching Option to HBM for high bandwidth
4. Acceleration Functions – compression, encryption, query acceleration, others
Intelligence Edge Metadata DB

- Big Meta DB in SSD
- Long DB loading time to DRAM
- IO BW busy

- Persistent Memory on FPGA to reduce DB loading time
- FPGA acceleration for pattern search and matching
- Improved BW and Latency
FPGA + Persistent Memory

- Unique Competitive Solution to address Big, Fast and Predictable Data needs
- Workload offload to FPGA for Acceleration
- Memory Semantics
- Low Memory latency access at high BW throughput
- Leverage on different Memory Hierarchy
- Deterministic high transaction per second
- Coherent and non-coherent Persistent Memory options (through Coherent Interconnect or PCIe)
- Cost effective & Flexible capacity and performance scale-out model
Thank you

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&
Intel Keynote on August 7th @ 11AM