STT-MRAM – A High Performance Complement to Flash Memory

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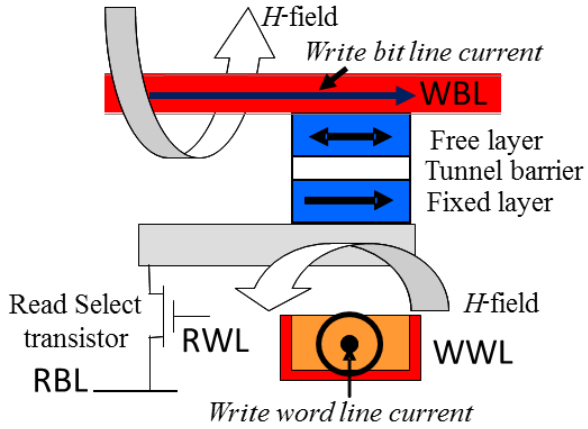
Flash Memory Summit

Overview

- STT-MRAM Technology Background
- STT-MRAM Technology Specifications
- STT-MRAM Use Cases
- Silicon Data

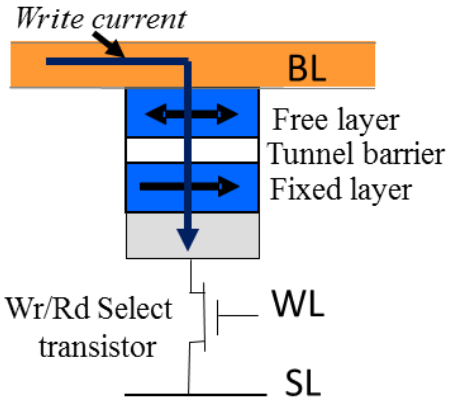
STT-MRAM Technology Background

MRAM Technology Evolution



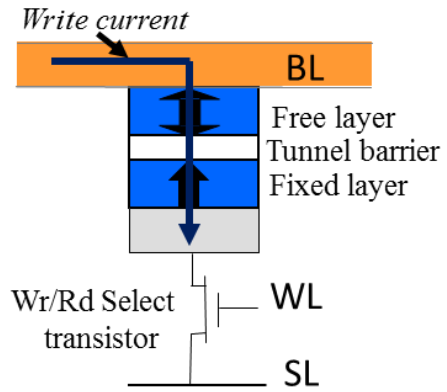
Toggle MRAM

- Production since 2006
- 256kb – 16Mb
- 35ns Parallel (SRAM), SPI, QSPI
- Commercial, Industrial, Automotive



STT-MRAM (iMTJ)

- Production 2015
- 64Mb ST-DDR3, 90nm node
- Commercial

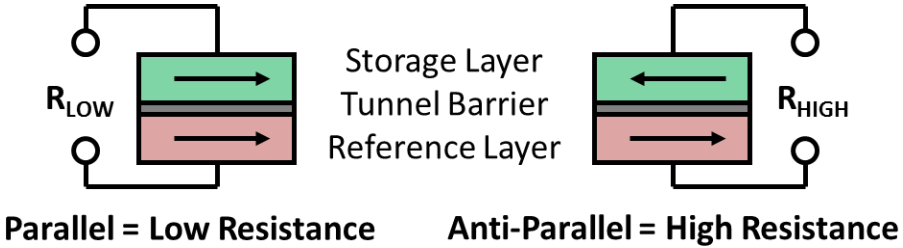


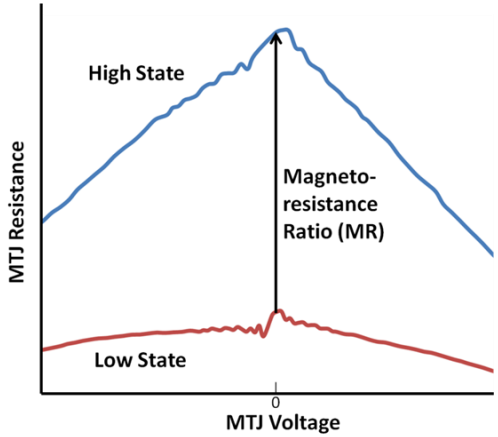
STT-MRAM (pMTJ)

- 256Mb ST-DDR3, 40nm node, Prod. 2017
- 1Gb ST-DDR4, 28nm node, Prod. 2019
- Commercial

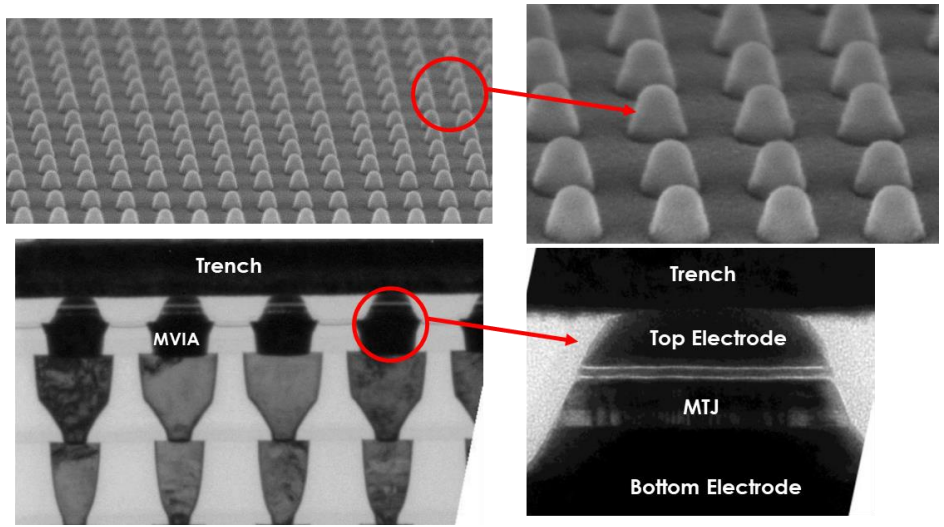
MRAM States

- **Magnetoresistance Effect**
  - Parallel = Low
  - Anti-Parallel = High
  - MR = (Rhigh/Rlow-1)*100%
  - RA = Rlow * Area
- **Aluminum Oxide (Toggle)**
  - MR ~40% at 25C
  - Higher RA material
- **Magnesium Oxide (STT-MRAM)**
  - MR >120% at 25C
  - Lower RA material



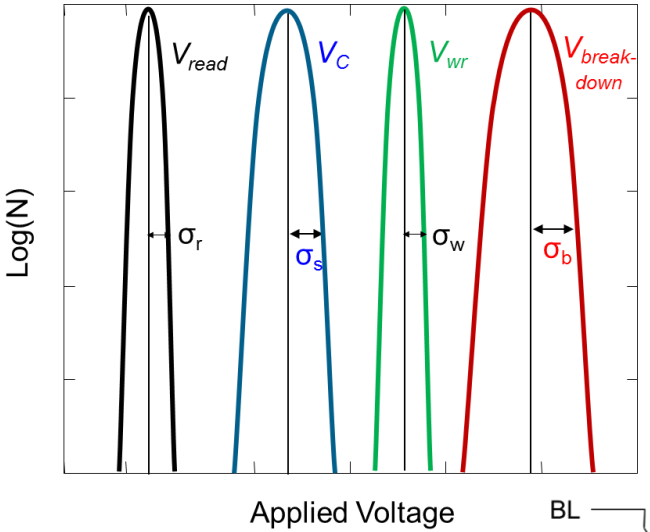


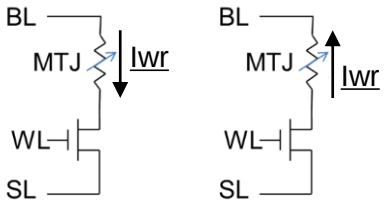
STT-MRAM Integration



- **Magnetic Tunnel Junction (MTJ) integrated between metal layers**
  - No changes to transistor integration
  - Fast development on advanced nodes
- **Simple 1T-1MTJ structure**
  - One transistor select device
  - Cell area constraints similar to DRAM
  - MTJ connected directly to Bitline

STT-MRAM Operation





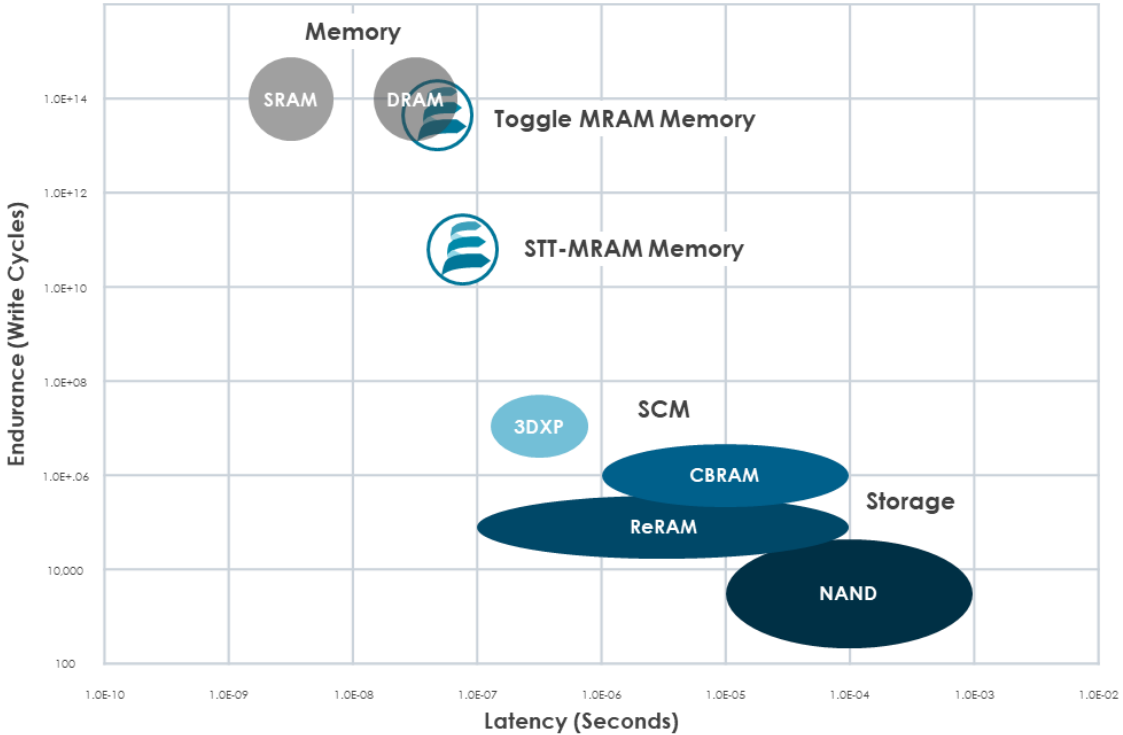
High->Low

Low->High

- **Read Operation**
  - Low voltage to avoid disturb
  - Detect High or Low resistance state
  - Low power
- **Write Operation**
  - Current direction determines state
  - Some overdrive required for low BER
  - Too much overdrive impacts endurance

STT-MRAM Technology Specifications

Memory Performance with Persistence



MRAM COMBINES PERFORMANCE OF MEMORY WITH PERSISTENCE OF STORAGE

- **Non-Volatile:** Maintains data without power or refresh
- **Fast:** Read/write similar to DRAM
- **Endurance:** Handles memory workloads

256Mb ST-DDR3 and 1Gb ST-DDR4

EVERSPIN TECHNOLOGIES

EMD3D256M08BS1
EMD3D256M16BS1

FEATURES

256Mb ST-DDR3 Spin-transfer Torque MRAM

- Non-volatile 256Mb (32Mb x 8, 16Mb x 16) DDR3

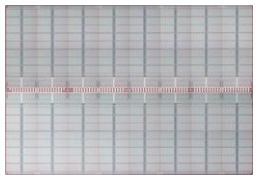
EVERSPIN TECHNOLOGIES

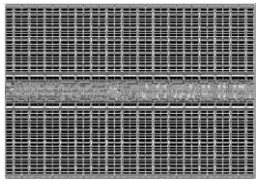
EMD4E001GAS1

FEATURES 1Gb Non-Volatile ST-DDR4 Spin-transfer Torque MRAM

- 128Mb x8, 64Mb x16 Organization
- Supports most DDR4 features
- Page size of 1024 bits for x8, 2048 bits for x16
- VDD = VDDQ = 1.2v
- VPP = 2.5V
- Operating Temperature of 0˚C to 85 ˚C
- 667MHz clock frequency (fCK)
- On-Device Termination
- Multipurpose register READ and WRITE capability
- Per-Device addressability (PDA)
- Connectivity Test
- On-Chip DLL aligns DQ, DQS, DQS transition with CK transition
- Burst lengths of 8 addresses
- All addresses and control inputs are latched on rising edge of the clock

	256Mb ST-DDR3	1Gb ST-DDR4
VDD / VPP	1.5V	1.2V / 2.5V
Data Retention	**3 months / 70C**	**3 months / 70C**
Endurance	**1e10 cycles**	**1e10 cycles**
Uniform Lifetime Writes per Chip	**320 PBW** 3.8 years continuous	**1280 PBW** 15.2 years continuous
Peak Bandwidth per x16 Chip	**2.67GB/s**	**2.67GB/s**



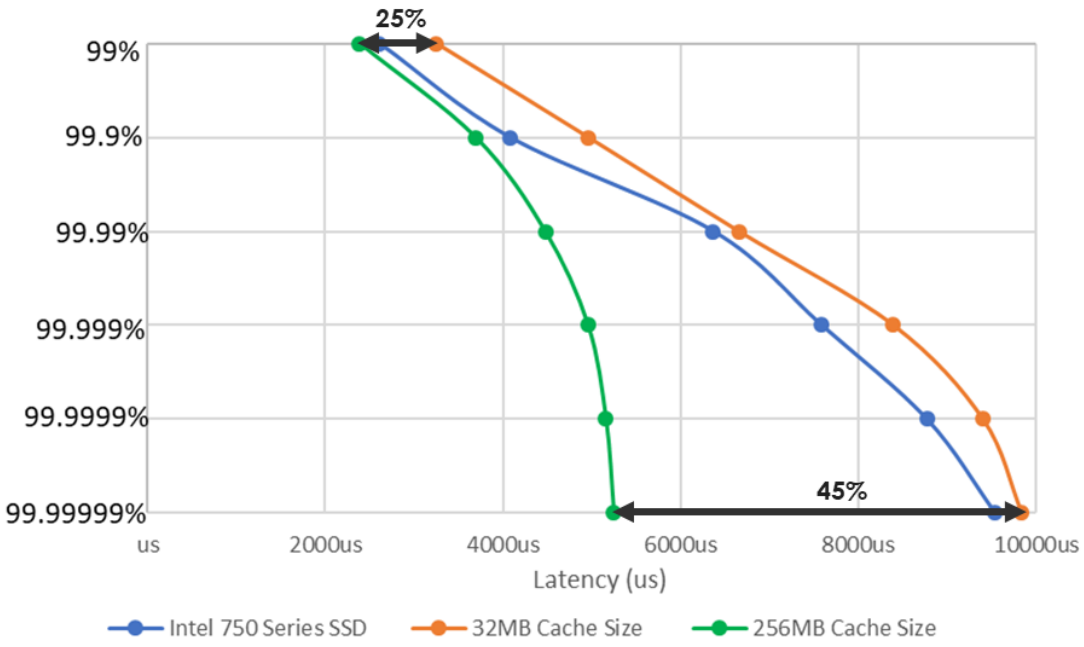


STT-MRAM Use Cases

Enterprise Storage

Larger Buffer Improves QOS	Enable Higher Number of Streams	Simplified Architecture Eliminates Power Fail Hardening	More Physical Space For Storage Capacity	No Capacitor Liability	Optimized Interleave For Sequential Performance

SSD QoS Improvement



QOS IMPROVEMENT

- 25% - 45% latency improvement
- Latency improvement is architecture dependent

Flash Memory Summit

Storage Accelerator

Optimized Log Management	9x Improvement In Overall Storage Performance*	No Special Drivers Standard NVMe	No Stored Charge Liability

T. Andre
Flash Memory Summit 2019
Santa Clara, CA

EVERSPIN TECHNOLOGIES

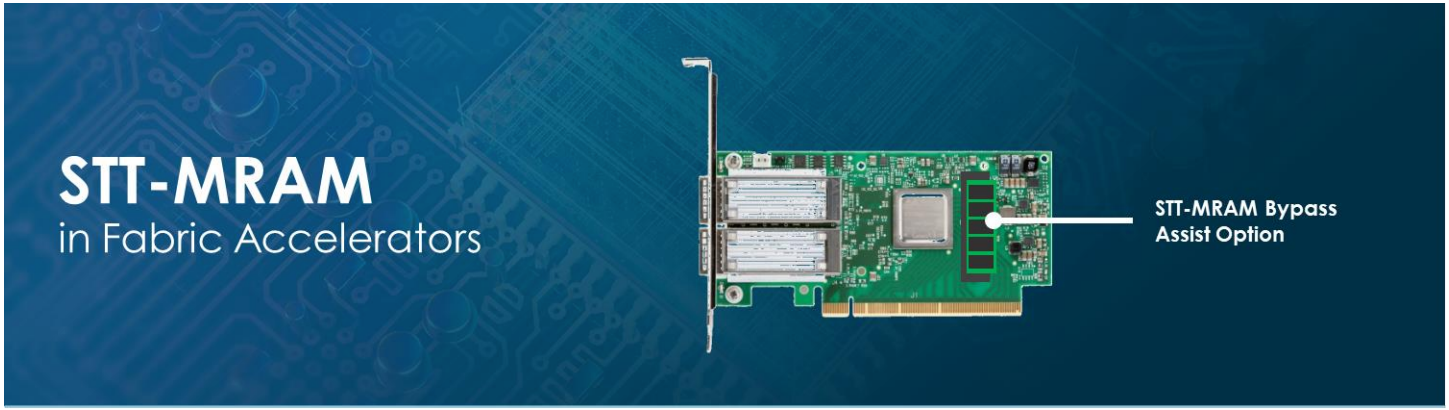
1GB STT-MRAM Storage Accelerator

Category	Parameter	Specification
	Available Capacity	1GB
	Persistent Memory Modules	256Mb Perpendicular STT-MRAM
Performance	Sequential Read/Write	Up to 6,000 MB/sec
	Random 4KB Read	Up to ~230MB/sec
	Random 4KB Write or Sustained 4KB Write	Up to 1,500,000 IOPS
	Random 70/30 Read/Write	Up to 1,460,000 IOPS
	Average Latency Read/Write (QD1)	6 µsec (read), 7 µsec (write)
	Worst Case Latency Read/Write (QD8)	10 µsec (read), 11 µsec (write)
Endurance	Drive Writes per Day	Unlimited uniform access
	Data Retention	Power on - infinite; Power off - 3 months at 50°C

Category	Parameter	Specification
Interface	Host Interface	PCIe Gen3 x8 (8GT/s), Non-volatile Memory Express (NVMe)
	Access Modes	Block mode (NVMe)
	PCIe Card Form Factor	Half Height, Half Length (HHHL)
Environment	Power Consumption 70/30 Read/Write	<25W
	Operating Temperature	0 to 55°C ambient with suggested airflow
	Non-operating Temperature	-40°C to +70°C
OS	Linux, Windows	
Management	Self Monitoring Analysis and Reporting Technology (SMART) commands	

https://www.smartm.com/salesLiterature/dram/nvNITRO_Accelerator_overview.pdf

Fabric Accelerator



Higher Performance With Bypass Assist

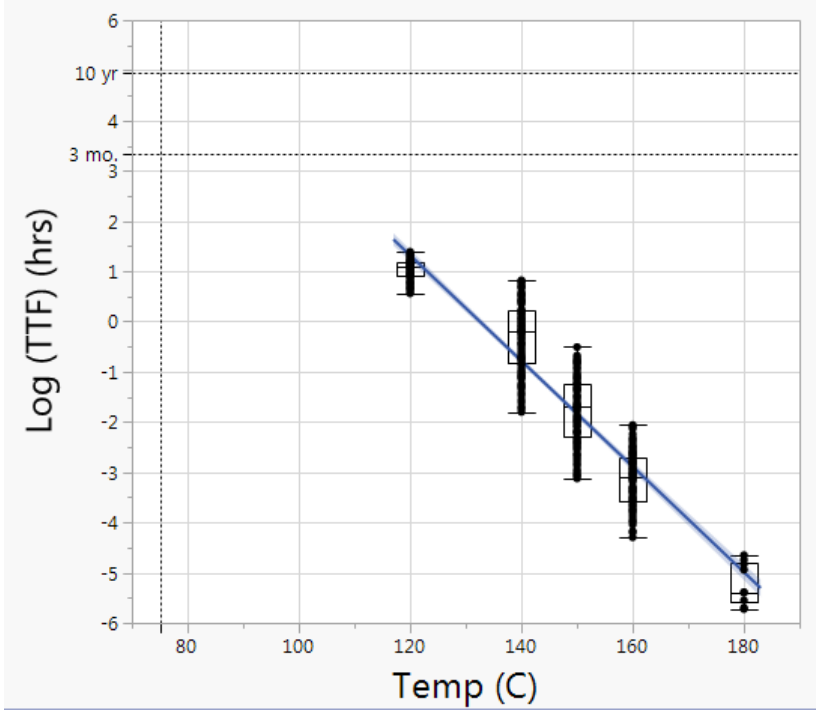
- Acts as power loss protected write burst data buffer on the fabric/network controller card for offload engines
- Providing at point persistent write data completion
- Eliminates the multi-microseconds latency path before data can be committed to a persistent device

Provide bigger working persistent memory region

Enables product differentiation

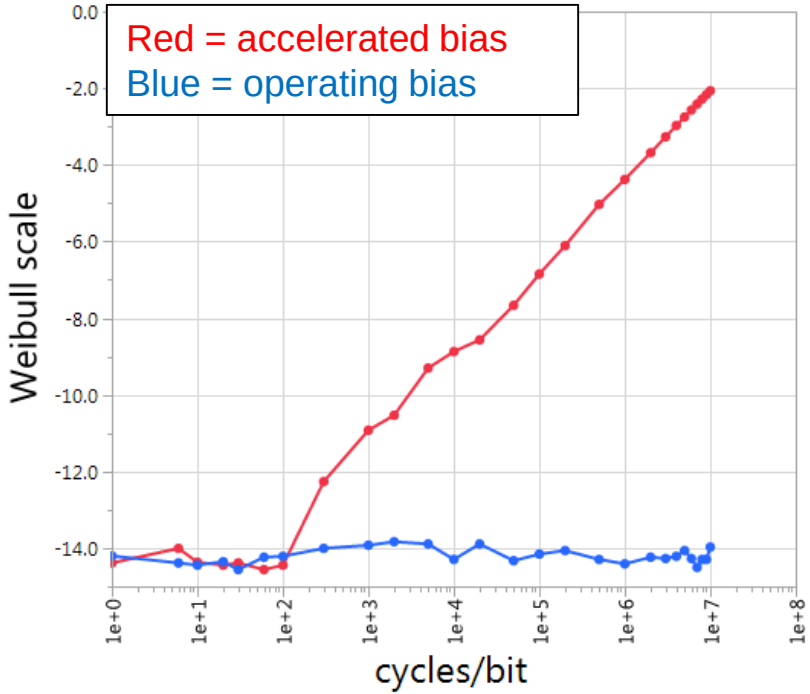
Silicon Data

Data Retention



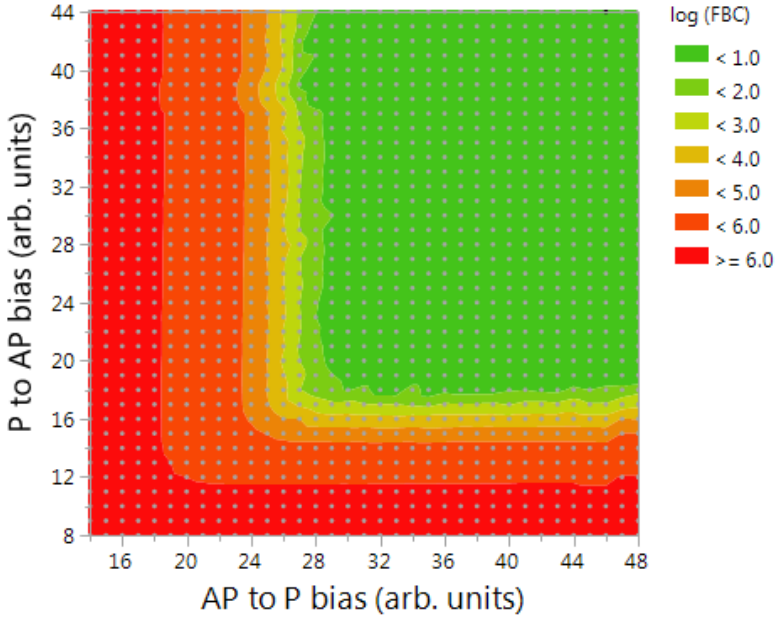
- **1Gb Data Retention**
  - Accelerated Testing at Elevated Temperatures
  - Demonstrates 10yr at 85C

Endurance



- **1Gb Endurance**
  - Accelerated Testing at elevated voltages
  - Well behaved TDDB Weibull distribution
  - Testing validated 1E10 cycles through every page

Write Operation



- **1Gb Write Operation**
  - Normal switching distributions
  - Wide operating range

Summary

Summary

- **1Gb STT-MRAM is here!**
  - Built on 13 years of MRAM production experience
- **STT-MRAM delivers 2.67GB/s write and read performance per chip**
  - ST-DDR4 interface with JEDEC DDR4 compatible footprint
- **STT-MRAM delivers over 1 Exabyte lifetime writes per chip**
  - Supports a lifetime of write data buffering with low chip count
- **STT-MRAM delivers highly reliable solutions**
  - Demonstrated reliability and persistence without capacitors or batteries
  - Large persistent memory capacity improves QoS