Compute Express Link (CXL) and Persistent Memory: Enabling scalability

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Flash Memory Summit

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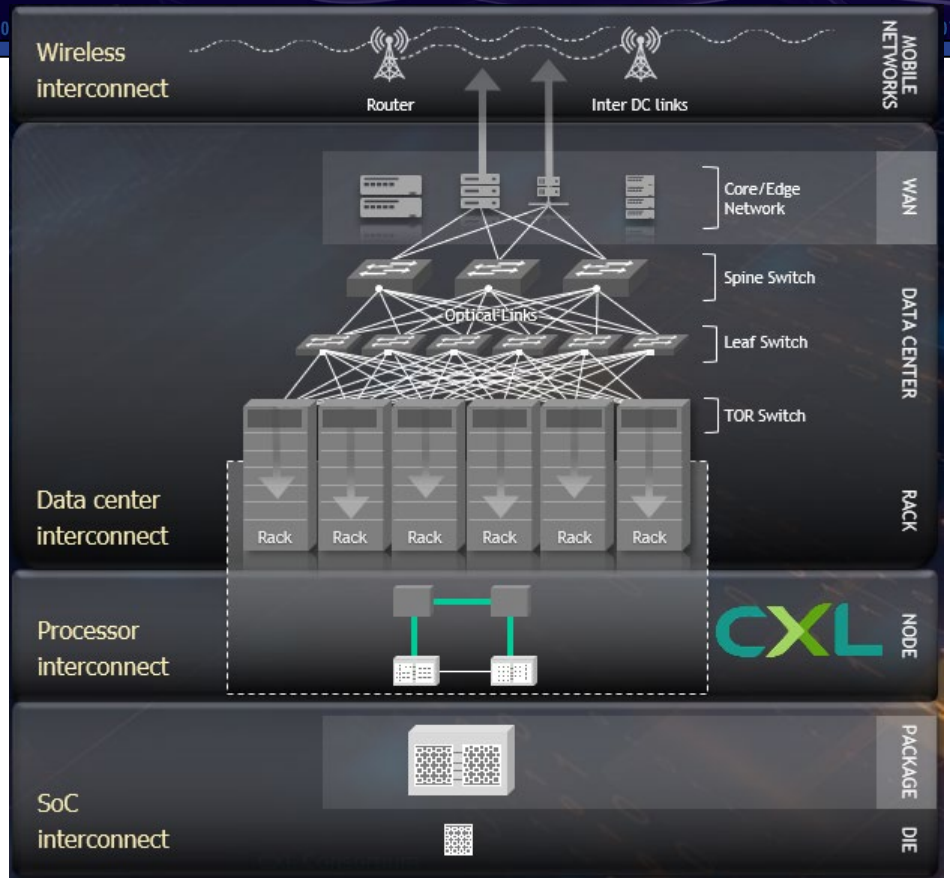
Introducing Compute Express Link (CXL)

Processor Interconnect:

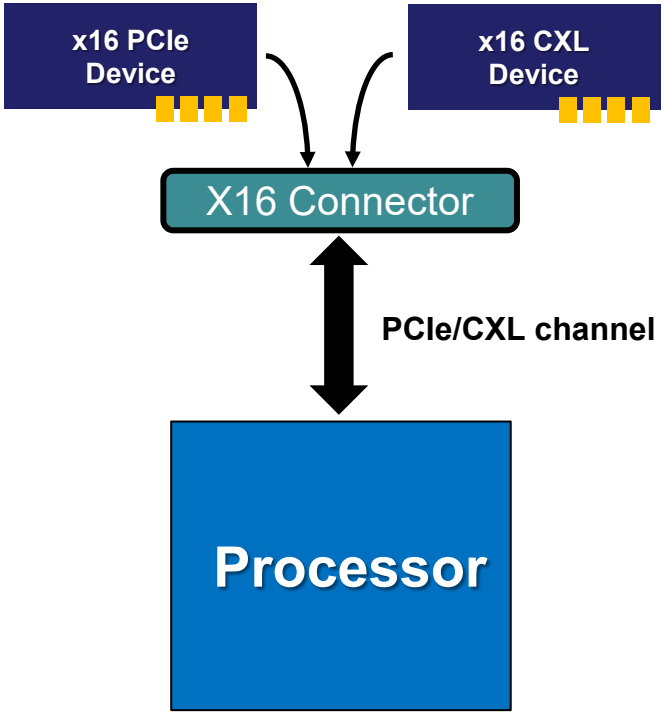
- Open industry standard
- High-bandwidth, low-latency
- Coherent interface
- Leverages PCI Express®
- Targets high-performance computational workloads
  - Artificial Intelligence
  - Machine Learning
  - HPC
- Targets Memory-centric architectures



A new class of interconnect for device connectivity

What is CXL?

- Alternate protocol that runs across the standard PCIe physical layer
- Uses a flexible CPU port that can auto-negotiate to: PCIe or CXL
- First generation CXL aligns to 32 Gbps PCIe 5.0
- CXL usages expected to be key driver for an aggressive timeline to PCIe 6.0

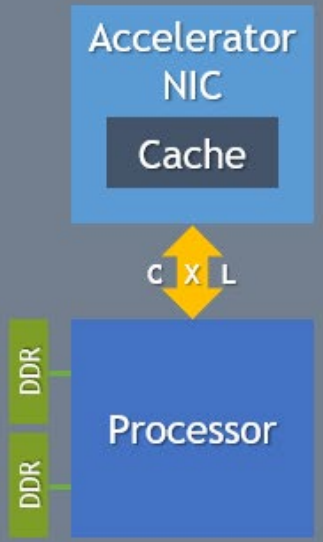


Representative CXL Use Cases

Caching Devices / Accelerators

Usages:
- PGAS NIC
- NIC atomics

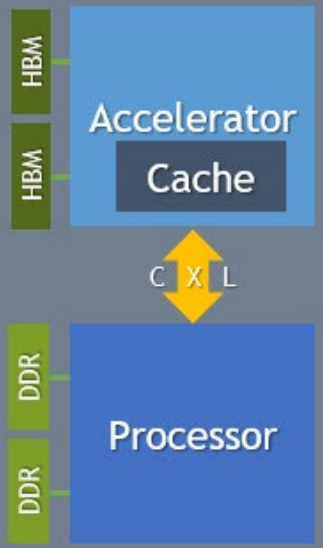
Protocols:
- CXL.io
- CXL.cache



Accelerators with Memory

Usages:
- GPU
- Dense Computation

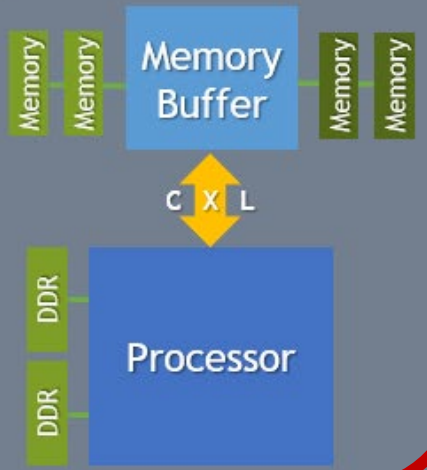
Protocols:
- CXL.io
- CXL.cache
- CXL.memory



Memory Buffers

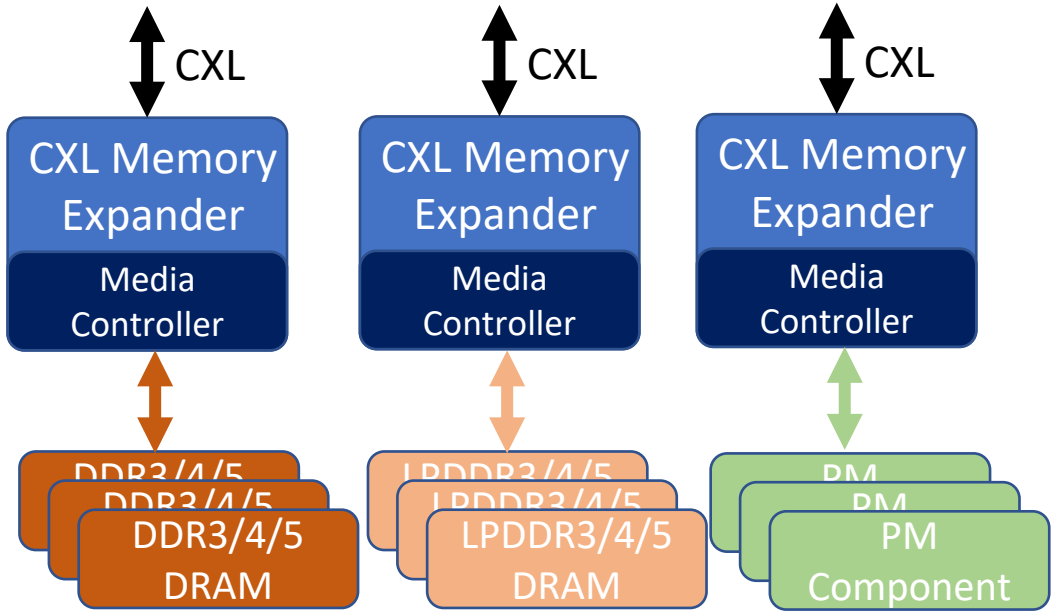
Usages:
- Memory BW expansion
- Memory capacity expansion
- Storage Class Memory

Protocols:
- CXL.io
- CXL.mem



CXL: A Common Memory Interface

- CXL provides a common, standard interface for many types of memory
- Media independence: could be used to connect DDR3/4/5, LPDDR3/4/5, Persistent memory, etc
- Enables flexibility for different media characteristics (persistence, latency, BW, endurance, etc)



Heterogeneous Memory Attach - DIMMs vs CXL

- DIMMs are not suitable for Heterogeneous Memory types

- CXL solves the problem
  - Enables a slow memory tier to be completely isolated from main tier
    - Minimal interference between CXL and direct attached DRAM DIMMs
  - Enables other memory types whose bandwidth is additive to existing platform memory bandwidth
    - E.g. DDR4 and DDR5 can coexist in the same platform
  - CXL capacity additive to platform memory capacity
    - With inevitable move towards 1 DIMM per DDR channel, CXL becomes a cost-effective path for capacity expansion

CXL: Addressing System Challenges

1. Power density
   - DIMM slots tend to be power limited to 15-18W (less in more dense platforms)
   - CXL enables:
     - Separation of DIMM slots and CXL Memory slots
     - Higher power CXL Memory devices (e.g. 25W+)

2. Memory channel count scaling
   - Parallel DDR* interfaces require 200+ pins
   - CXL enables:
     - Less pins per package = more channels or smaller packages
     - Lower mother board PCB layer counts

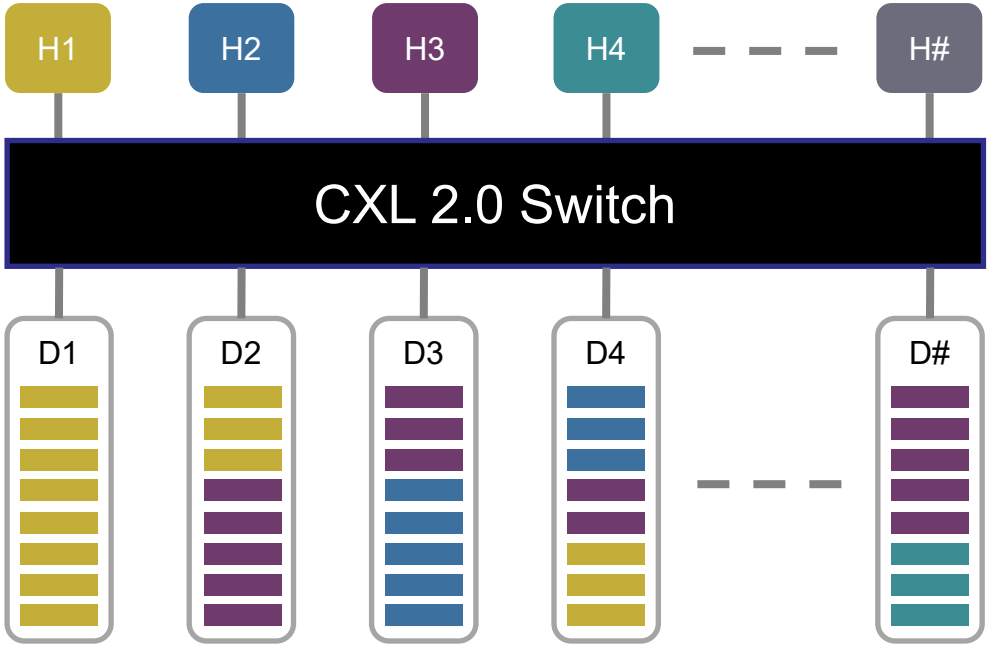
3. Form factor flexibility

What's new in CXL 2.0?

- Pooled memory
- Standardized Management Interface
- Global Persistent Flush

CXL 2.0 Memory Pooling

Memory Pooling with Multiple Logical Devices

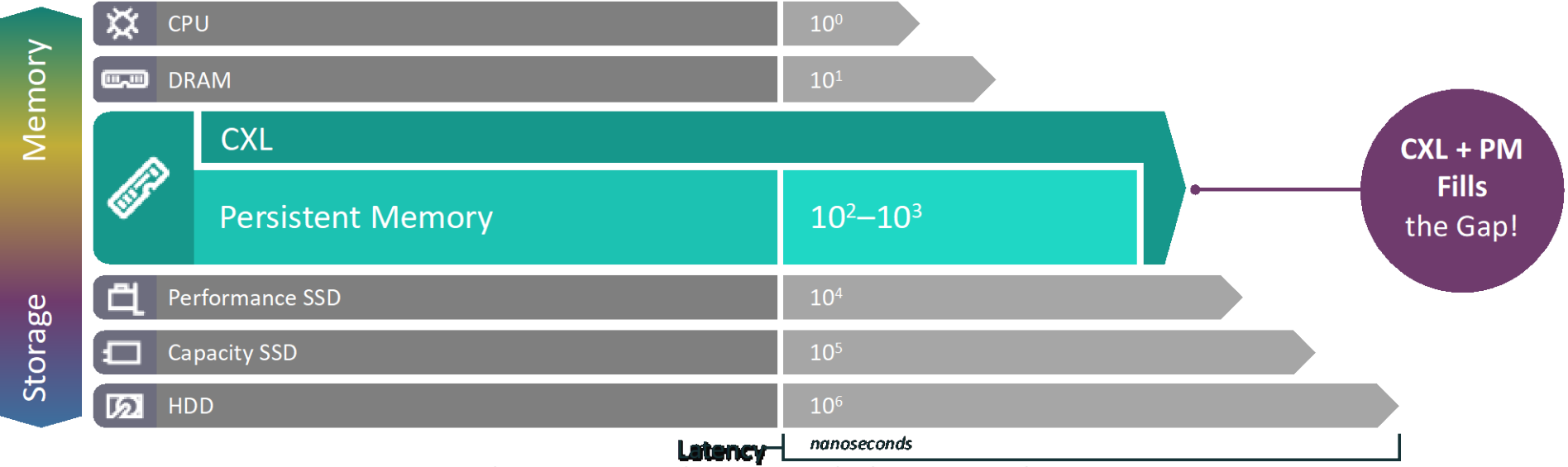


Persistent Memory Benefits of CXL 2.0

Moves Persistent Memory from Controller to CXL

Enables standardized Management of the Memory and Interface

Supports a Wider Variety of Form Factors



Summary

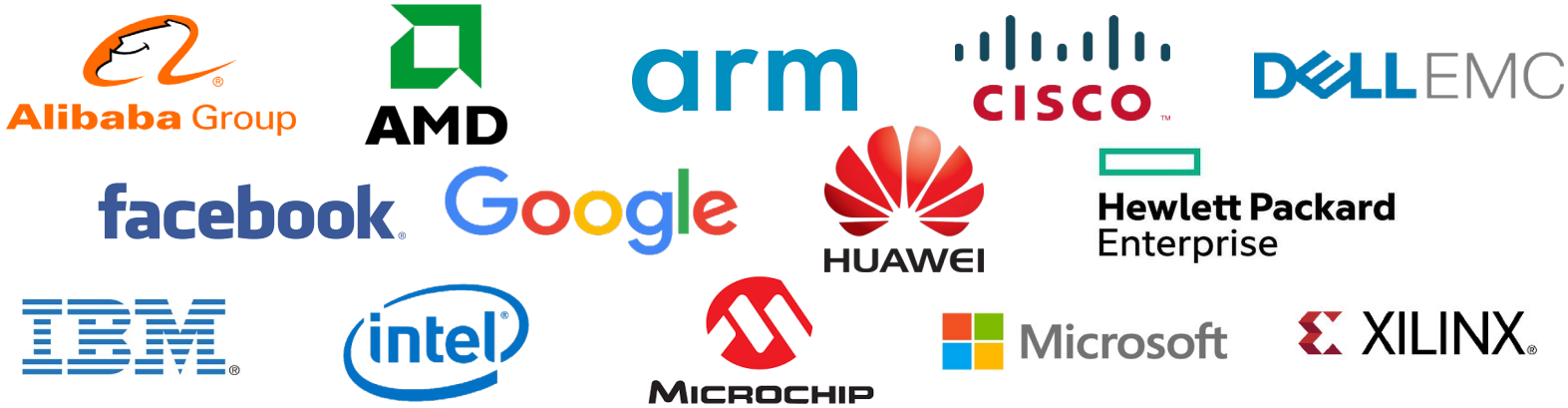
CXL enables a standardized, scalable persistent memory solution:

- Bandwidth and capacity
- Form factor flexibility
- System design flexibility: Power, Thermal, Complexity, Cost
- Electrical, protocol, and switching interface
- Management interface

CXL Consortium Overview

- CXL Consortium boasts 130+ member companies to date and still growing

- CXL Consortium Work Groups:
  - 5 Technical (Protocol, PHY, Software & Systems, Memory, Compliance) and Marketing
- CXL Board of Directors:



Call to Action

- CXL ecosystem in the industry continues to grow…
  - First anniversary of incorporation – second generation specification, working on third generation
  - Response to industry needs and challenges
- Fully backwards compatible with CXL 1.1
- Compliance & Interop program
- Call to action
  - Join CXL Consortium
  - Follow us on Twitter and LinkedIn for more updates!

Thank You!

Flash Memory Summit

Everything You Need To Know
For Success