









Cameron Brett, KIOXIA, Moderator Panelists:



Jonmichael Hands, Chia Network; Don Jeanette, TRENDFOCUS; Trent Johnson, IBM; Paul Kaler, HPE; Bill Lynn, AMD



Thursday, August 10, 8:30 am Ballroom B

Learn more - www.snia.org/fms



Santa Clara Convention Center

August 8-10, 2023

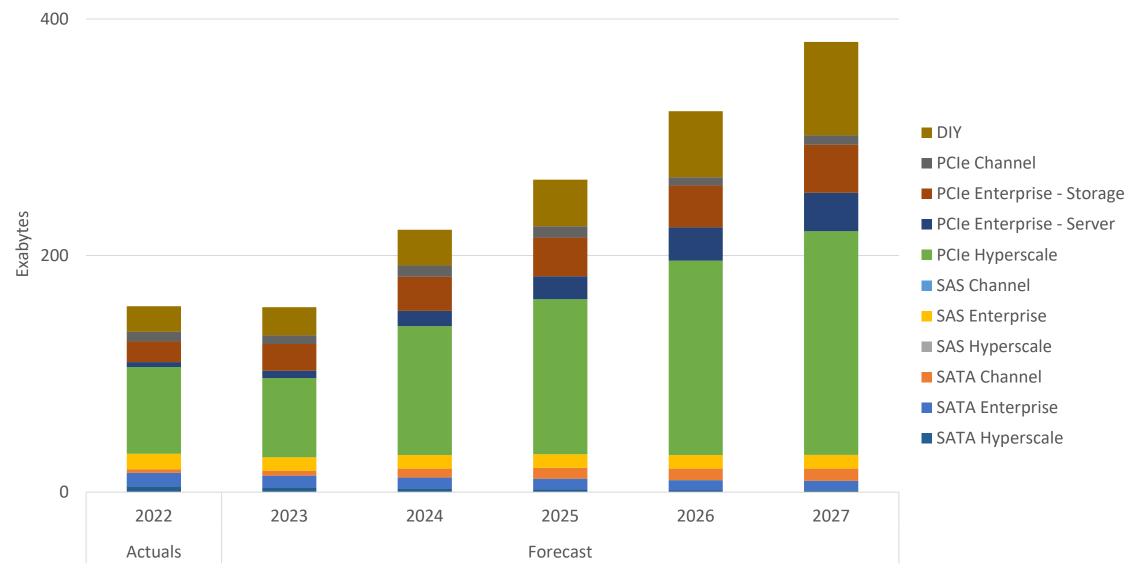
FlashMemorySummit.com

ALL ABOUT MEMORY & STORAGE

Don Jeanette

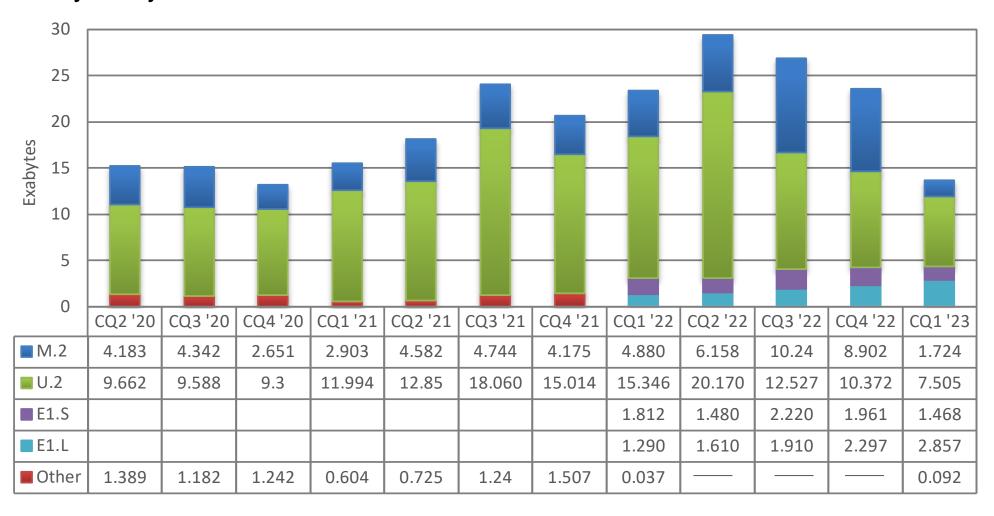
Trend Focus

eSSD Forecast: Exabytes by End Market

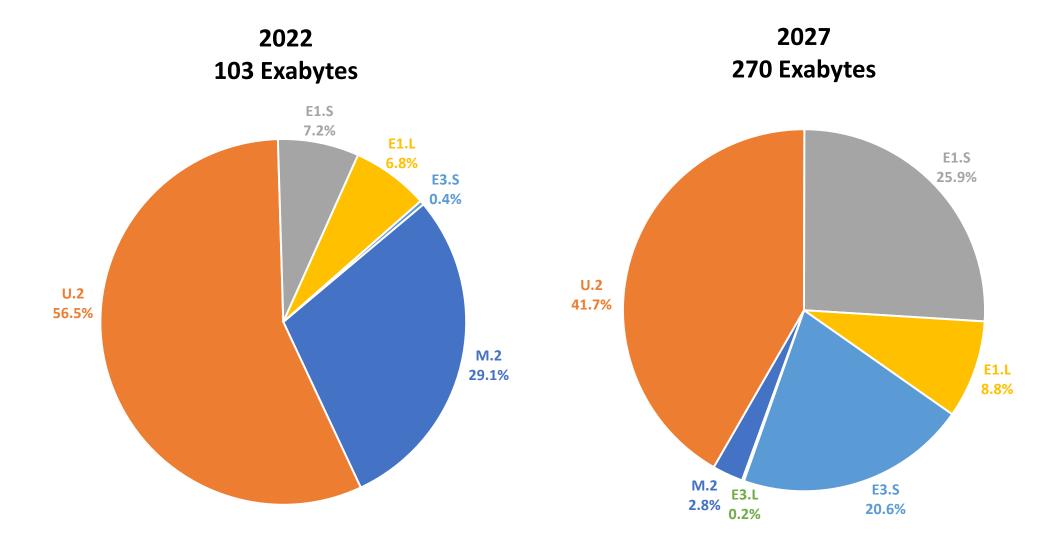


Historical Enterprise PCIe SSD

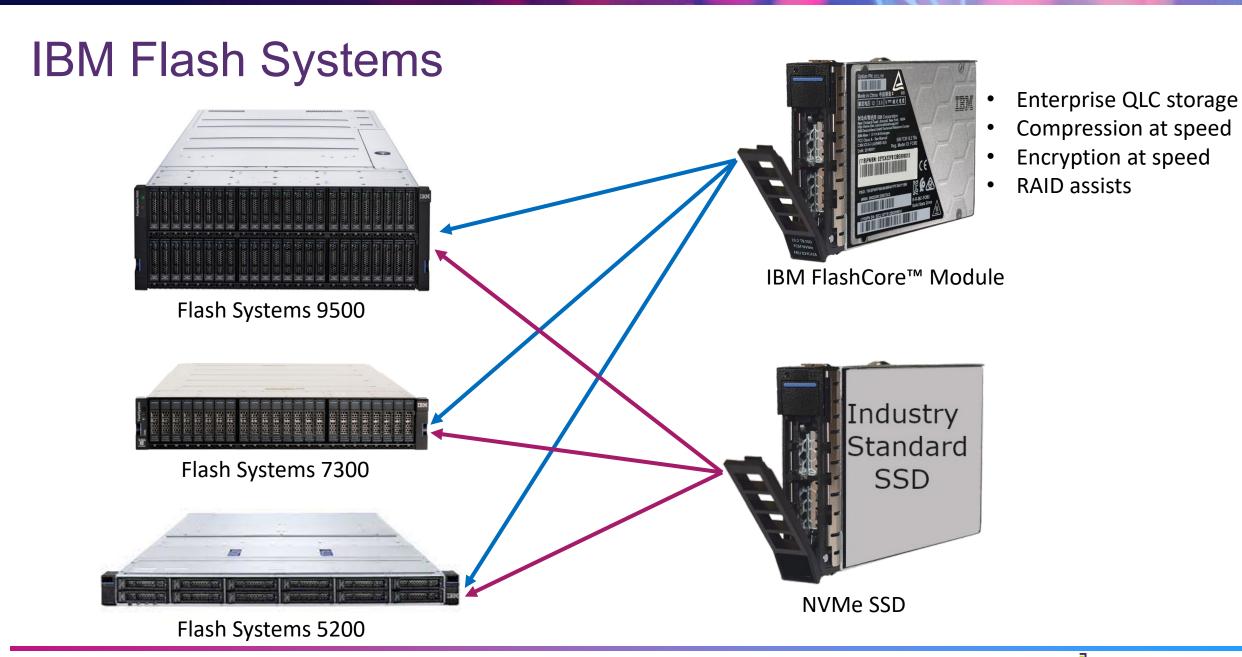
Exabytes By Form-Factor



PCIe Exabytes by Form Factor



Trent Johnson



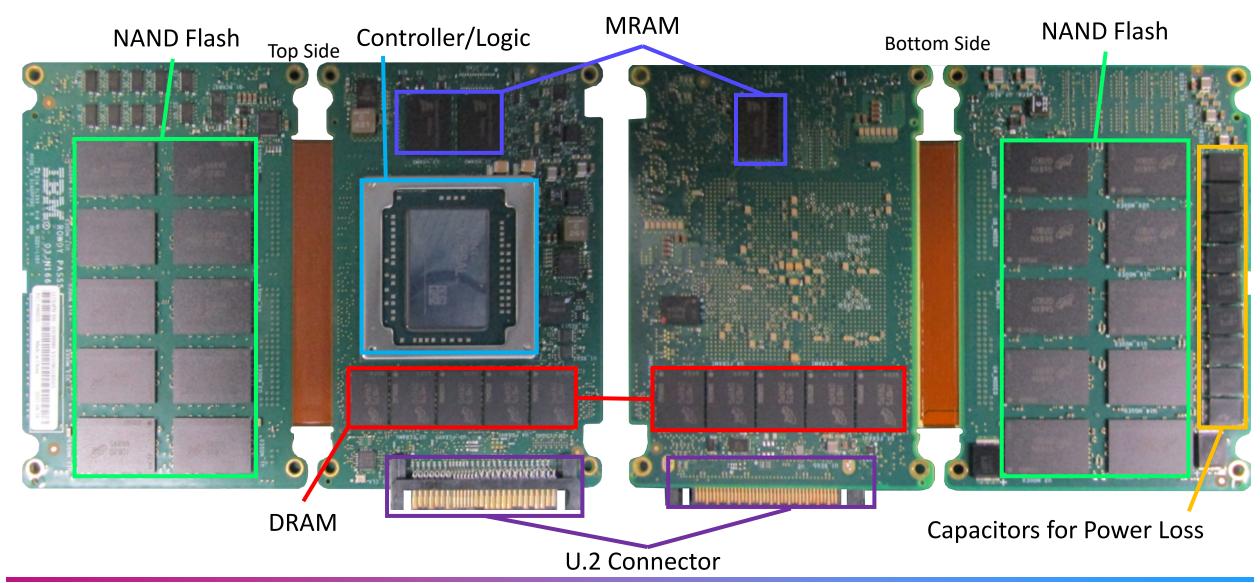


Benefits of EDSFF for IBM Flash Systems

- Greater drive power envelope allows for more flexible design
- More efficient use of space allows greater enclosure density
- Fewer lane connections enabled by PCle 5
- Increased switch bandwidth enabled by PCIe 5
- Simpler connector
- Slots are useful for more than just SSDs
- Increased adoption of E3 is driving volumes from U.2 to E3



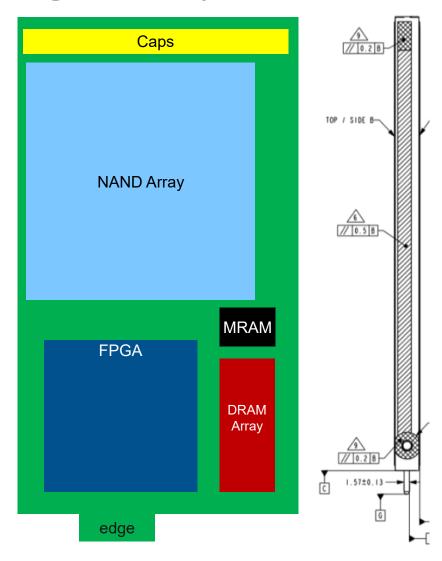
The Layout of Today's IBM FlashCore™ Module



FlashCore™ Module E3.L Floor Planning Concept







Paul Kaler

Hewlett Packard Enterprise

HPE 1U ProLiant Server EDSFF E3.S Adoption

HPE ProLiant DL320 Gen11 1U, 1P



HPE ProLiant DL360 Gen11 1U, 2P



Up to 8 EDSFF E3.S or 4 E3.S 2T NVMe PCle Gen5 SSDs

Up to 20 EDSFF E3.S or 10 E3.S 2T NVMe PCle Gen5 SSDs

Software Defined Compute, Data Collection and Management, Cold Storage workloads requiring a cost optimized, compact form factor

Compute-dense solution for high-performance workloads such as VDI, EDA, CAD, or virtualization workloads that require increased compute density with built-in security and flexibility

HPE 1U ProLiant Server EDSFF E3.S Adoption

HPE ProLiant DL325 Gen11 1U, 1P



HPE ProLiant DL365 Gen11 1U, 2P



Up to 20 EDSFF E3.S or 10 E3.S 2T NVMe PCle Gen5 SSDs

Up to 20 EDSFF E3.S or 10 E3.S 2T NVMe PCle Gen5 SSDs

Software Defined Compute, Data Collection and Management, CDN, VDI, and Cold Storage workloads requiring a cost optimized, high density, compact form factor

Compute-dense solution for high-performance workloads such as VDI, EDA, CAD, or virtualization workloads that require increased compute density with built-in security and flexibility

HPE 2U ProLiant Server EDSFF E3.S Adoption

HPE ProLiant DL380 Gen11 2U, 2P



HPE ProLiant DL380a Gen11 2U, 2P



Up to 36 EDSFF E3.S or 18 E3.S 2T NVMe PCle Gen5 SSDs

Performance, expandability, and scalability for diverse workloads and environments, e.g., Collaborative, CRM, SCM, ERM, Data & Analytics, Al, VDI, and Content Mgmt

Up to 8 EDSFF E3.S or 4 E3.S 2T NVMe PCle Gen5 SSDs

4DW GPUs in a 2U2P ProLiant DL design for emerging Al workloads, e.g., Al Training & Inference, MCAD, HPC, and Engineering Apps

HPE 2U ProLiant Server EDSFF E3.S Adoption

HPE ProLiant DL345 Gen11 2U, 1P



HPE ProLiant DL385 Gen11 2U, 2P



Up to 36 EDSFF E3.S or 18 E3.S 2T NVMe PCle Gen5 SSDs

Up to 36 EDSFF E3.S or 18 E3.S 2T NVMe PCle Gen5 SSDs

Data-intensive workloads such as software-defined storage, video transcoding, and virtualized apps

Compute and data storage demanding workloads requiring increased core count, and storage and I/O scalability, e.g., AI, ML, Big Data analytics

HPE Alletra 4000 Storage Server EDSFF E3.S Adoption

HPE Alletra 4110

1U, 2P all-NVMe data storage server



20 EDSFF E3.S NVMe PCle Gen5 SSDs

For the most **performance-demanding** data storage-centric workloads:

- Data stores for machine learning
- Distributed and NoSQL databases
- High-performance Software-Defined Storage (SDS)
- Data-heavy hyperconverged infrastructure (HCI)

HPE Alletra 4120

2U, 2P hybrid-NVMe data storage server



12 EDSFF E3.S NVMe PCle Gen5 SSDs (rear mount)

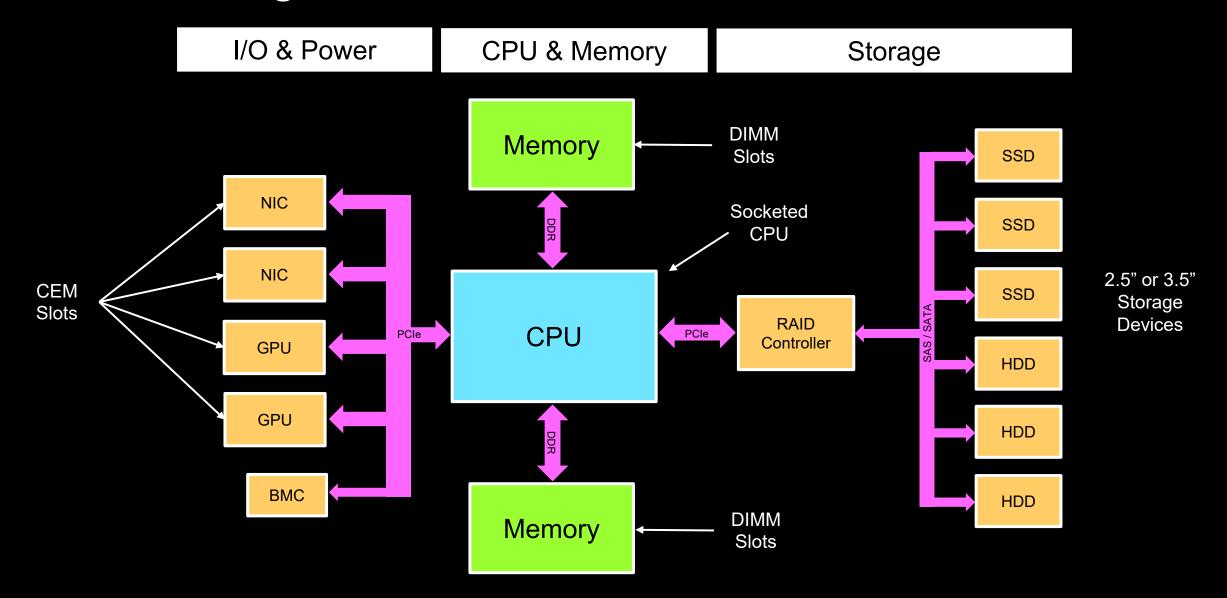
For the **broadest range of data** storage-centric workloads including:

- analytics data lakes
- general purpose Software-Defined Storage (SDS)
- converged data protection
- active archives
- and many more!

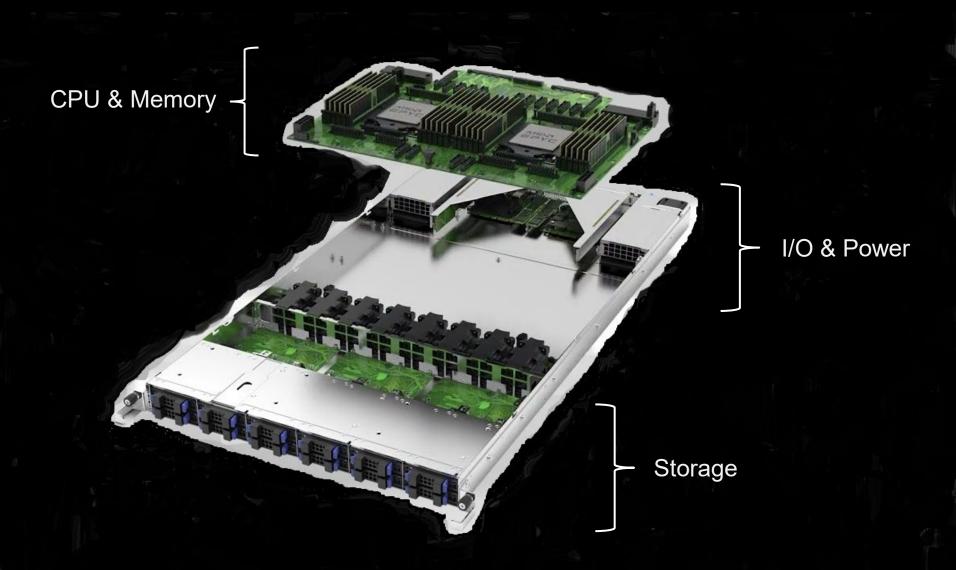


Bill Lynn AMD

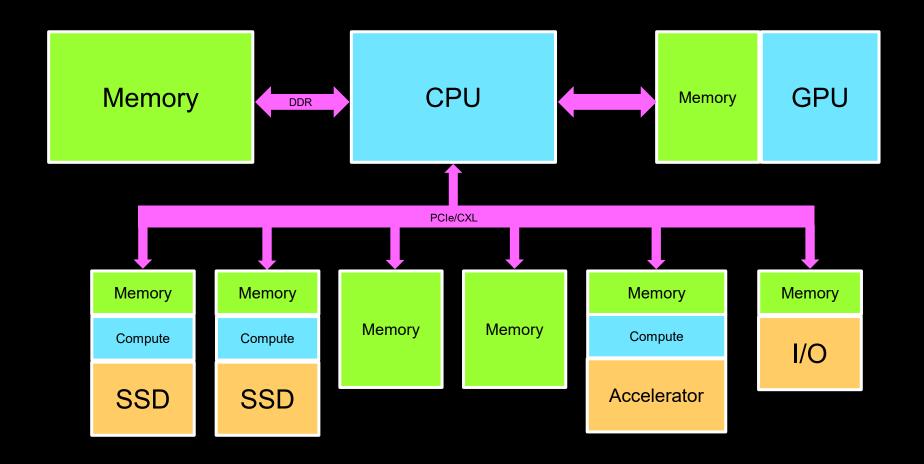
Traditional Single Socket Server Architecture



DC-MHS Implementation with full width HPM

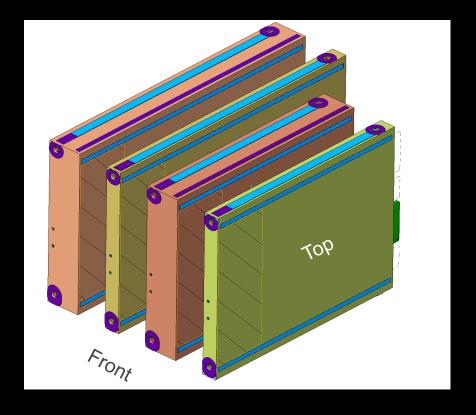


Memory is Everywhere



E3

- Family of four device form factors with a common width that vary in length and width.
- Primarily targeted as a replacement for 2.5" and 3.5" drive form factors.
- Based on the SFF-TA-1002 connector providing support for PCIe Gen 5 and Gen 6.
- Supports various PCIe link widths including x1, x2, x4, x8, and x16
- Expanded use cases include CXL memory, low end accelerators, and network adapters



Device Variation	Width	Length	Thickness	Power
E3.S	76mm	112.75mm	7.5mm	25W
E3.S 2T	76mm	112.75mm	16.8mm	40W
E3.L	76mm	142.2mm	7.5mm	40W
E3.L 2T	76mm	142.2mm	16.8mm	70W



Jonmichael Hands

Chia Networks

SSD EDSFF Ecosystem – Drive Vendors

















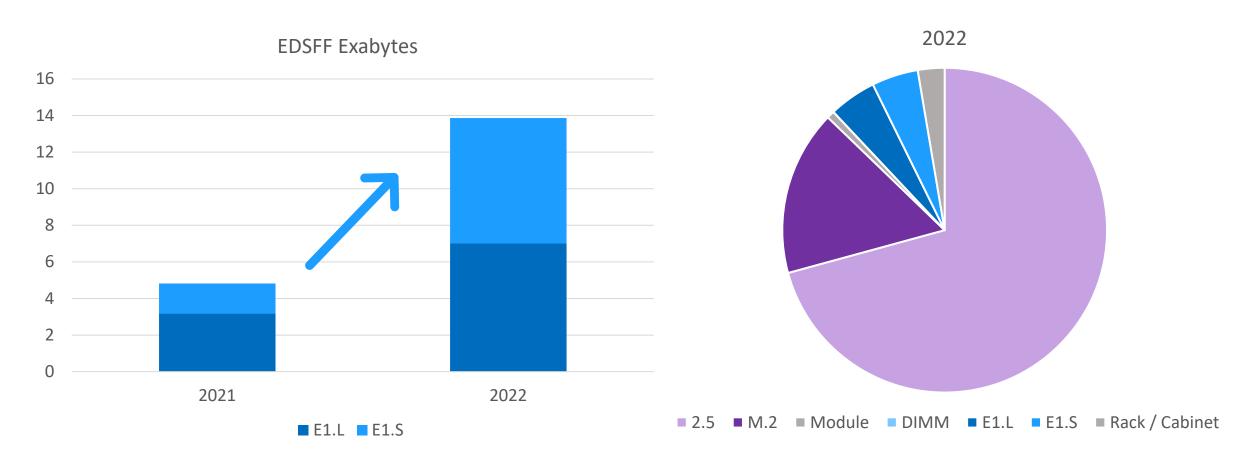








EDSFF Market Adoption



Source: IDC Worldwide Quarterly SSD Shipment Results, CY 4Q22 Doc #US49401423, February 2023

EDSFF Server and Storage SUPERMICE



SSG-221E-NE324R

ASG-1115S-NE316R



16x Hot-swap EDSFF E3.S (1T) NVMe slots, support E3.S (2T)





24x Hot-swap EDSFF short (E1.S) 9.5 or 15mm NVMe slots



SSG-121E-NE316R – Support E3.S 2T x8 (CXL) Devices



EDSFF Specification Update

- E3, SFF-TA-1008
 - 2.03: Support for 4C+ (OCP NIC), and 2x1C, added new use cases (CXL), label positioning, LED definition (power/activity & fault/identify)
 - 2.04: Clarify "sustained" max power
- SFF-TA-1009: 3.1.1
 - PCIe 6.0!!
 - USB 2.0 and NIC signals, LED stuff

8. PCIe Electrical Requirements

In general, EDSFF devices are expected to follow requirements as specified in both the *PCI Express Base Specification* and the *PCI Express Card Electromechanical Specification*. This chapter provides device requirements that deviate from the *PCI Express Card Electromechanical Specification*. For details on the connector electricals, please refer to *SFF-TA-1002 Card Edge multiliane protocol agnostic connector specification*.

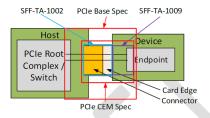


Figure 8-1. EDSFF Electrical Requirements Coverage

8.1 Signal Integrity Requirements

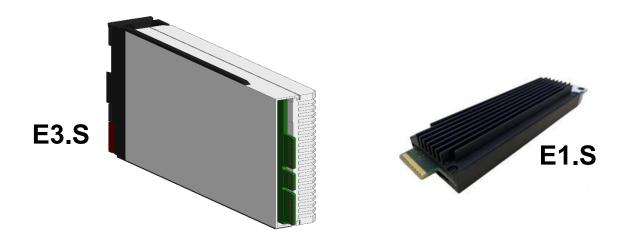
Table 8-1 summarizes the signal integrity requirements for the device. Additional explanation is provided in the subsequent sections. All measurements are referenced to an $85~\Omega$ differential impedance.

Line Rate	Insertion Loss (IL)	Return Loss (RL)	Power Sum Near End Crosstalk (PSNEXT) ¹	Power Sum Far End Crosstalk (PSFEXT) ¹
PCIe 4.0 (8 GHz NRZ16.0 GT/s)	-5.5 dB (f = 0 to 8 GHz)	≤ -10 dB (< 4 GHz) ≤ -7 dB (4 to 24 GHz)	≤ -40 dB (0 to 12 GHz)	≤ -40 dB (0 to 8 GHz) ≤ -48 + 1.0 * f dB (f = 8 to 12 GHz)
PCIe 5.0 (<u>32.0 GT/s</u> 16- GHz NRZ)	≥ -0.2 - 0.425 * f dB (f = 0 to 16 GHz) ≥ 5 - 0.75 * f dB (f = 16 to 24 GHz)		≤ -45 dB (0 to 16 GHz) ≤ -55 + 0.625 * f dB (f = 16 to 24 GHz)	≤ -36 dB (0 to 16 GHz) ≤ -44 + 0.5 * f dB (f = 16 to 24 GHz)
PCIe 6.0 (64.0 GT/s)	\geq -1.5 - 0.28125 * f dB (f = 0 to 16 GHz) \geq 6 - 0.75 * f dB (f = 16 to 24 GHz)	≤-15dB (< 1.25 GHz) ≤-10dB (1.25 to 24 GHz)	\leq -60 dB (0 to 16 GHz) \leq -70 + 0.625 * f dB (f = 16 to 24 GHz)	\leq -50 dB (0 to 16 GHz) \leq -60 + 0.625 * f dB (f = 16 to 24 GHz)

Table 8-1. Summary of Signal Integrity Requirements

CXL Memory Modules (CMMs) – new standard

- EDSFF form factors are also now leveraged for main memory expansion with CXL interface
- In fact, JEDEC has recently published the first CXL Memory Module Specification (CMM) with significant industry support: JESD317
- Standard CMM targets specified: E1.S x8, E3.S 2T x8, E3.S 1T



JEDEC STANDARD

Compute Express Link (CXLTM) Memory Module Reference Base Standard

JESD317

March 2023

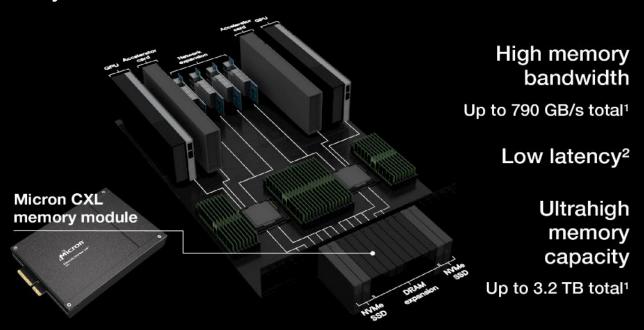
JEDEC SOLID STATE TECHNOLOGY ASSOCIATION





CXL Memory Modules

- Enable memory expansion physically removed from CPU or even outside of host system
- Can leverage the same EDSFF slots for CXL in system as used for PCIe-attached NVMe drives



¹ Memory capacity and bandwidth values based on AMD's next-generation SP5 high-end platform that offers 1P and 2P support, 12-channel DDR5 memory and 64 CXL V1.1+ lanes

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Emerging data center application workloads

Micron CXL memory expansion is ideal for data-intensive applications



High-performance computing



In-memory database



Business analytics



Virtualized platforms

Benefits of Micron CXL memory

Increase performance

Achieve up to 40% faster execution time³

Boost utilization

Balance memory bandwidth to CPU cores

Optimize allocation

Scale up memory without overprovisioning

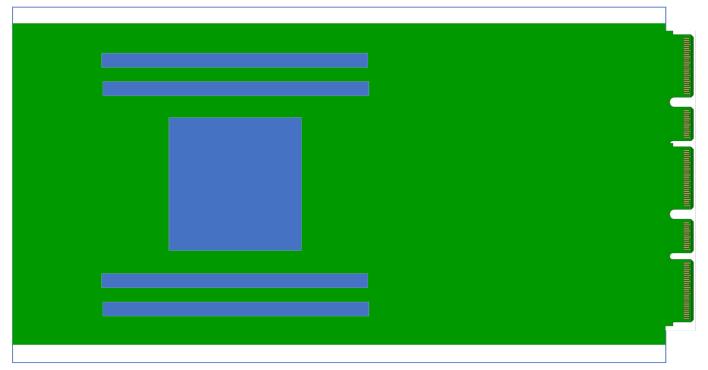


² Equivalent to single NUMA hop

³ Micron internal testing results based on CXL evaluation platform and emulation

EDSFF form factors and beyond

- The ecosystem for EDSFF has grown so significantly with E1 and E3 devices, further leverage is also being explored in industry.
- Most recent is work in SNIA SFF on new SFF-TA-1034 module: Pluggable Multi-purpose Module
- Could be leveraged for many different applications



- EDSFF-compatible connector
- Supports up to 32 lanes of PCIe/CXL
- High power support (400W+)

Targeting ~38-39mm height max and 16.8mm, fits in 1U rack space







Thank You!



Panelists and Discussion Topics

- General updates, use cases and product availability (65 minutes)
- Moderator Cameron T Brett
- Panelists
 - Don Jeanette, VP, Trend Focus
 - Jonmichael Hands, VP of Storage, Chia Networks
 - Trent Johnson, SSD Hardware Architect, IBM
 - Paul Kaler, Future Storage Architect, HPE
 - Bill Lynn, AMD
- ~8 mins per panelist (3-4 slides), with 25 mins of topic discussion
- Interactive with questions from audience

Narrative / Flow of Session / Slide Content (your own template)

- Cam welcomes and introduces the panelists
 - States the panelist will provide updates, insights and new product info
 - Interactive discussion, so questions can be asked during presentations
- Don provides the latest on SSD market data and growth of EDSFF
 - Comments on adoption and replacement of older technologies
- Trent Johnson why did IBM choose to develop EDSFF SSDs?
 - What is IBM's product and use case?
- Paul Kaler Newest platforms supporting EDSFF, E3 only?
 - Why the transition supporting PCIe 5.0 and beyond for EDSFF?
- Jonmichael SSD, spec and use case updates (from last webinar)
- Bill Lynn What is AMD doing with E3.S and CXL

Panel Discussion Topics

- Question 1 Geared to Don and market
 - How is the E3 and E1 adoption affecting
- Question 2 Geared to Paul and Trent on OEM applications
 - Why E3 for server and storage use cases? And why tie it to PCIe 5.0
- Question 3 Geared to JM on SSD trends
 - How is overall SSD adoption by vendors?
 - Cam can comment on KIOXIA SSDs
- Question 4 Geared to Bill/CXL
 - What makes E3.S a good fit for CXL and what other devices are a good fit?
- Question 5 What features/capabilities would you like to see come next for EDSFF?

Panel Discussion Topics

Add your own questions/topics you'd like me to ask