Enabling an Open Chiplet Ecosystem with UCIe

Richelle Ahlvers, *Intel, Vice-Chair and Executive Committee, SNIA*

Brian Rea, *Intel, Marketing Working Group Co-Chair, UCI Express*

SNIA COMPUTE, MEMORY, AND STORAGE SUMMIT

Solutions, Architectures, and Community

VIRTUAL EVENT, MAY 21-22, 2024

About the Presenters

Richelle Ahlvers

Storage Technology Enablement Architect, Intel

Richelle is a Storage Technology Enablement Architect at Intel, where she promotes and drives enablement of new technologies and standards strategies. Richelle has spent over 25 years in Enterprise R&D teams in a variety of technical roles, leading the architecture, design and development of storage array software, storage management software user experience projects including mobility, developing new storage industry categories including SAN management, storage grid and cloud, and storage technology portfolio solutions.

Richelle has been engaged with industry standards initiatives for many years and is actively engaged with many groups supporting manageability including SNIA, DMTF, NVMe, OFA and UCIe. She is Vice-Chair of the SNIA Board of Directors, Chair of the Storage Management Initiative, leads the SSM Technical Work Group developing the Swordfish Scalable Storage Management API, and has also served as the SNIA Technical Council Chair and been engaged across a breadth of technologies ranging from storage management, to solid state storage, to cloud, to green storage. She also serves on the DMTF Board of Directors as the VP of Finance and Treasurer and Chairs the Timberland SIG driving the NVMe-oF reference implementation.

About the Presenters

Brian Rea
Technology Initiative and Ecosystem Enablement Manager, Intel

Brian Rea is a senior technologist in the industry initiative and technology enabling team at Intel and is the Marketing Working Group Co-Chair for the UCIe Consortium. Brian has held engineering, marketing, and strategic planning roles bringing products with new technologies to market including USB, Gigabit Ethernet, PCIe, and CXL.

His passion is working with customers and partners to enable ecosystem innovations in silicon, hardware, and software.

Brian holds an MBA from the University of Washington and a BSEE from the University of Texas at Austin.

Agenda

What is UCIe™? And what are chiplets?

I’m a storage vendor. Why would I want to use chiplets?

I just use storage systems. How do chiplet-based systems help me?

What about other standards that I already use? Do they also work with UCIe-based systems?

UCIe Overview

SNIA COMPUTE, MEMORY, AND STORAGE SUMMIT
Solutions, Architectures, and Community
VIRTUAL EVENT, MAY 21-22, 2024

Chiplet Motivation

- Manufacturability
  - Create SOCs beyond reticle limit
  - Improve yields with smaller die
- Optimized process node for cost and functionality
  - Disaggregated dies across different nodes
  - Use new process node for advanced functionality
  - Targeted to best process: e.g. memory, logic, analog, co-packaged optics
- Faster Time to Market
  - Reuse proven chiplets
  - Create custom combinations, leveraging base product
- Interconnect benefit: Power Efficient, High Bandwidth, Low Latency

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."

- Gordon E. Moore
"Cramming more components onto integrated circuits," Electronics, Volume 38, Number 8, April 19, 1965

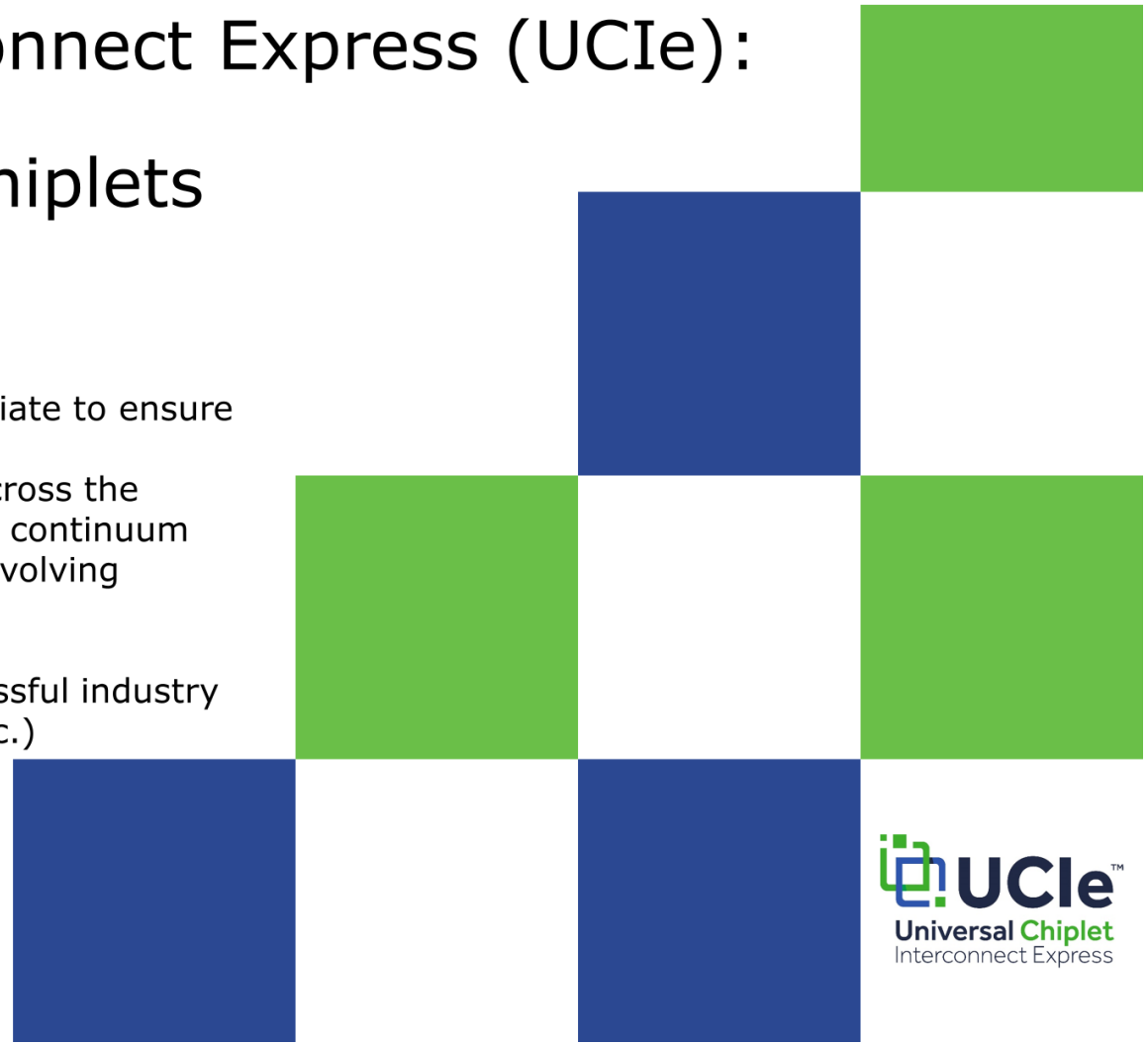
Universal Chiplet Interconnect Express (UCIe):

An Open Standard for Chiplets

<u>Guiding principles of UCIe</u>

1. Open Ecosystem with Plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)

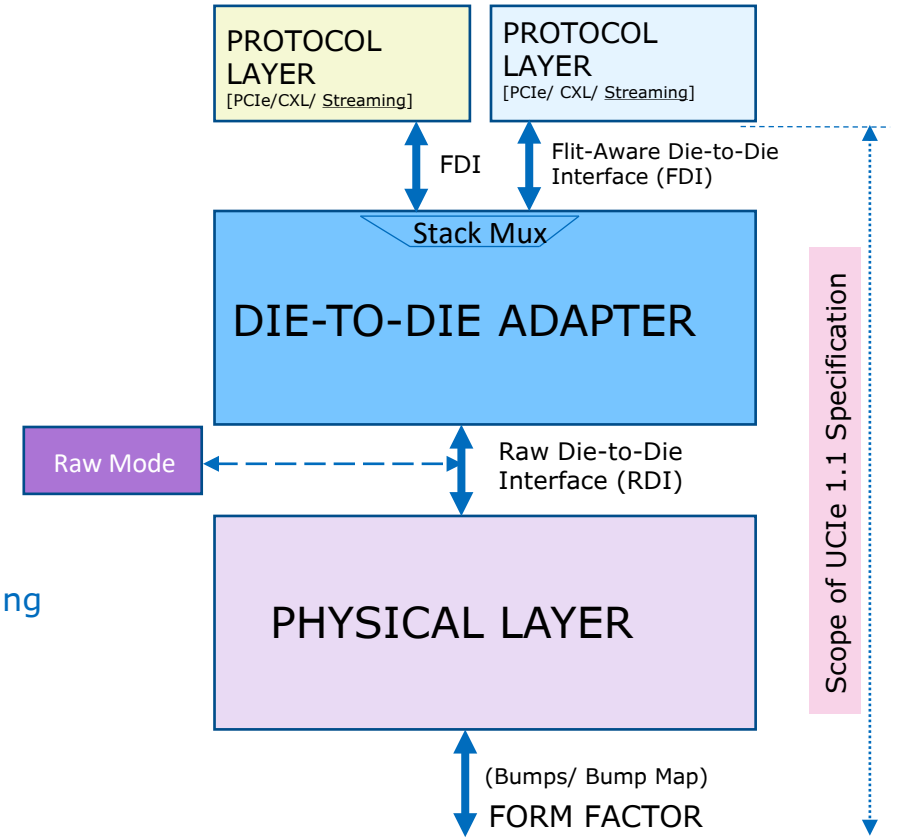


Founded March 2022, Now with over 130 Members

Leading IP, Tool, Chip Design, Foundry, OSAT, Services, and End Customer Companies

UCIe 1.1: Layered Approach with industry-leading KPIs

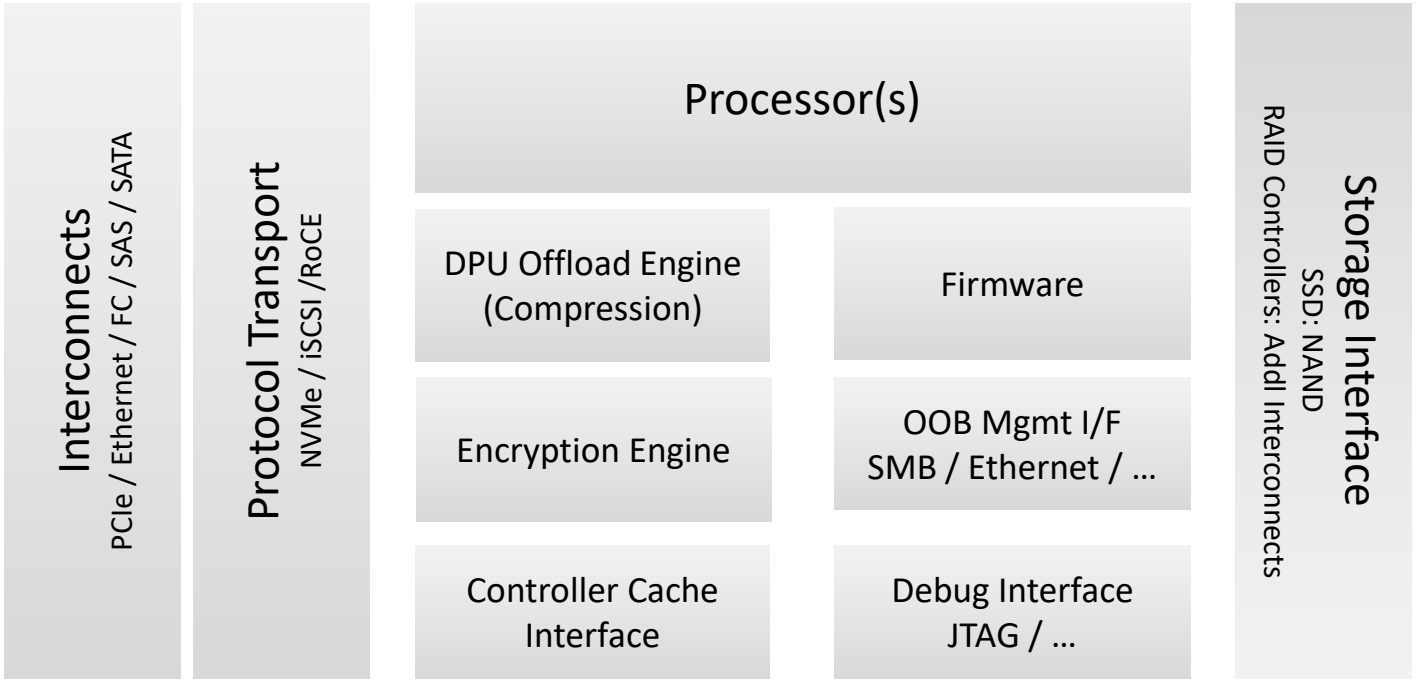
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:** Reliable delivery
  - Support for multiple protocols: bypassed in raw mode
- **Protocol:** CXL/PCIe and Streaming
  - **CXL™/PCIe® for volume attach and plug-and-play**
    - SoC construction issues are addressed w/ CXL/PCIe
    - CXL/PCIe addresses common use cases
      - I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
    - Protocol can be anything (e.g., AXI/CHI/SFI/CPI/ etc)
    - Streaming Protocols can use the D2D adapter (re-use CRC, Retry, etc.)
    - Streaming Protocols can multiplex with other protocols with on-demand interleaving
- **Well defined specification**: interoperability and future evolution
  - Configuration register for discovery and run-time
    - control and status reporting in each layer
    - transparent to existing drivers
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface



Applications to Storage

Storage systems have common building blocks.

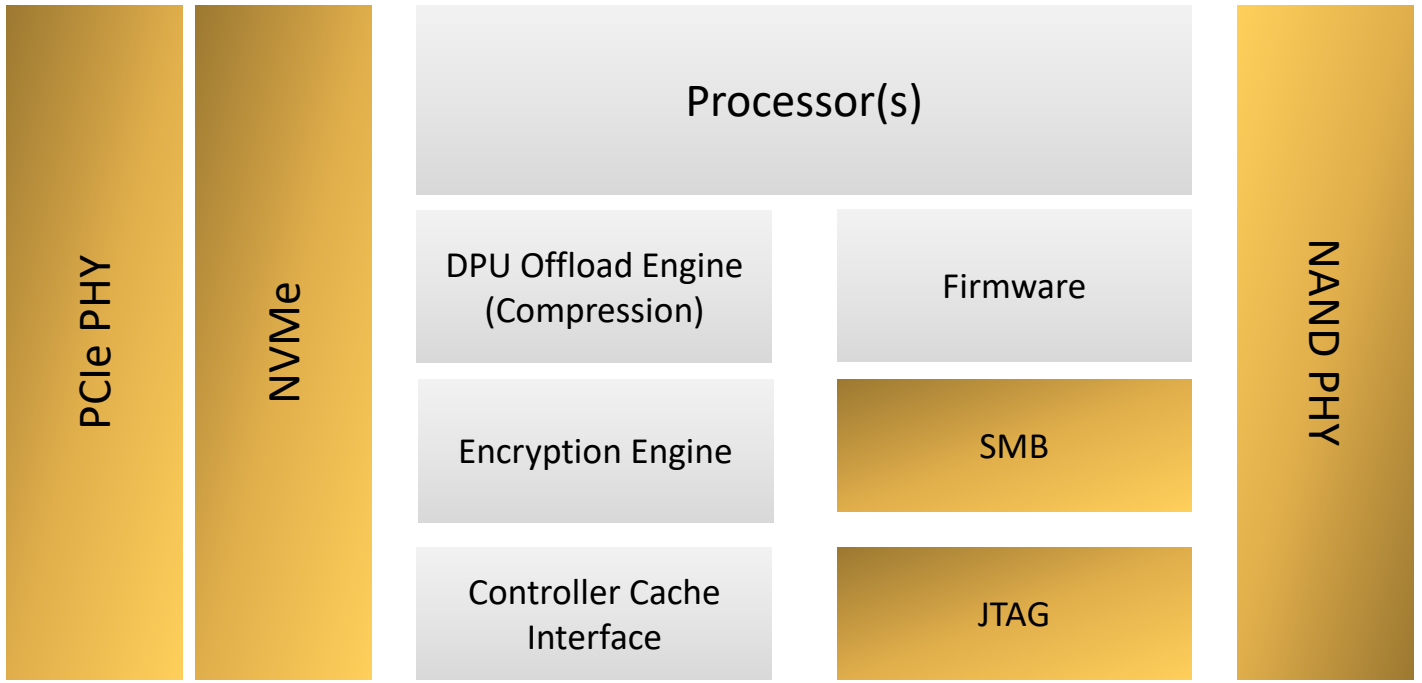
- There are common components used to build storage controllers.
- There are many of the same functions on SSD controllers and RAID controllers (albeit at different scale)
- Storage device systems already incorporate custom ASIC development into their designs



* Note: This does not represent any vendors actual architecture.

NVMe PCIe SSD:

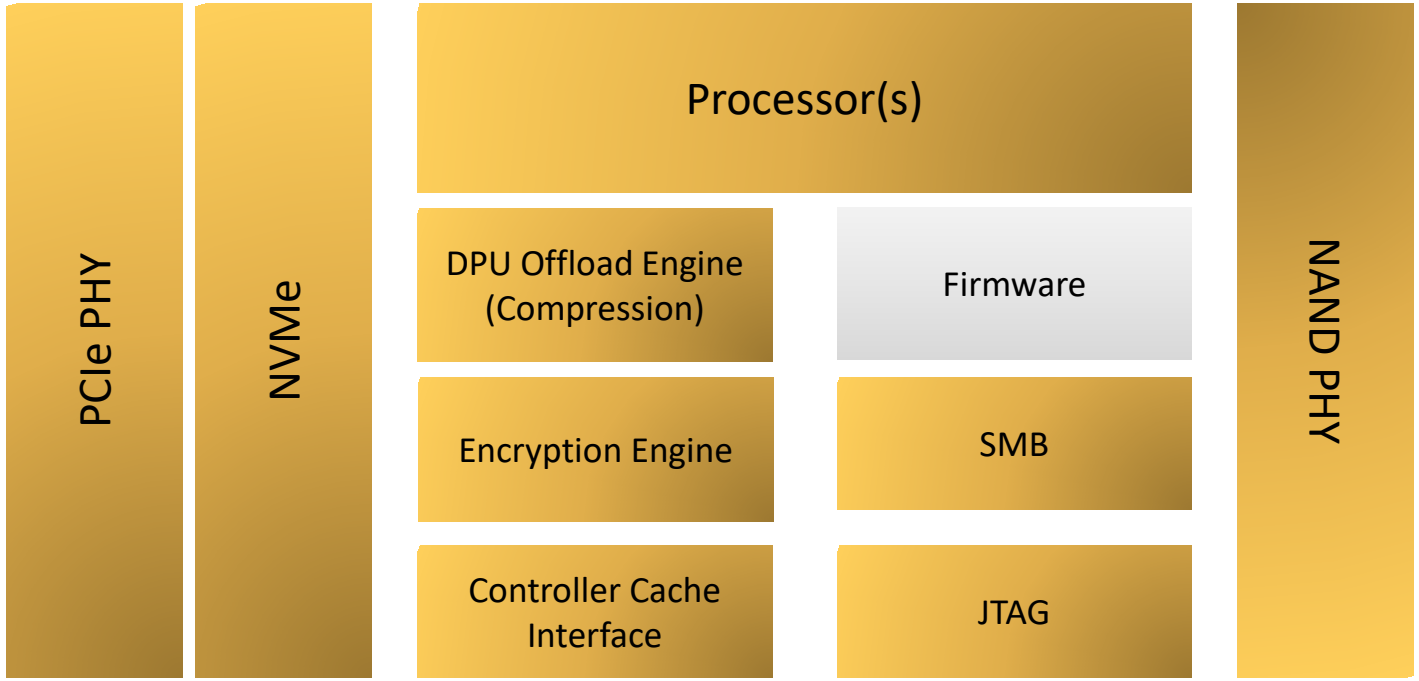
- Example representation for an NVMe SSD:
- This could be implemented in a chiplet-based ASIC SSD controller.



* Note: This does not represent any vendors actual architecture.

NVMe PCIe SSD: Potential Chiplets.

- Most of the functions depicted are candidates to be integrated from external sources
- This allows storage vendors to focus on their areas of true differentiation and value-add



* Note: This does not represent any vendors actual architecture.

Why are products built with standards-based chiplets valuable?

- Vendors focus on value-add and time to market
  - Pick the “off the shelf” components that have already been built and tested for peripheral functionality
- Built with standards already in use to accelerate adoption and integration:
  - Can be both built and integrated into systems using standards (e.g., PCIe and CXL)
  - Manage with MCTP-based protocols in-band: MCTP, PLDM, SPDM
  - Standards-based management out-of-band as part of UCIe
- Faster time to market, faster technology adoption times
- Good for vendors AND customers: fuels future innovation while leveraging the foundation of best in class, interoperable, common elements defined by open standards and a broad ecosystem

Please take a moment to rate this session.

Your feedback is important to us.