Breaking Through the Memory Wall with CXL®

SNIA COMPUTE, MEMORY, AND STORAGE SUMMIT

Solutions, Architectures, and Community

VIRTUAL EVENT, MAY 21-22, 2024

Presented by

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Product Manager,

CXL Smart Memory Controllers

Agenda

- Memory Wall
- Breaking through the Memory Wall
- Memory Bound Use Cases
- CXL for Modular Shared Infrastructure
- Ecosystem Enablement
- Calls to Action

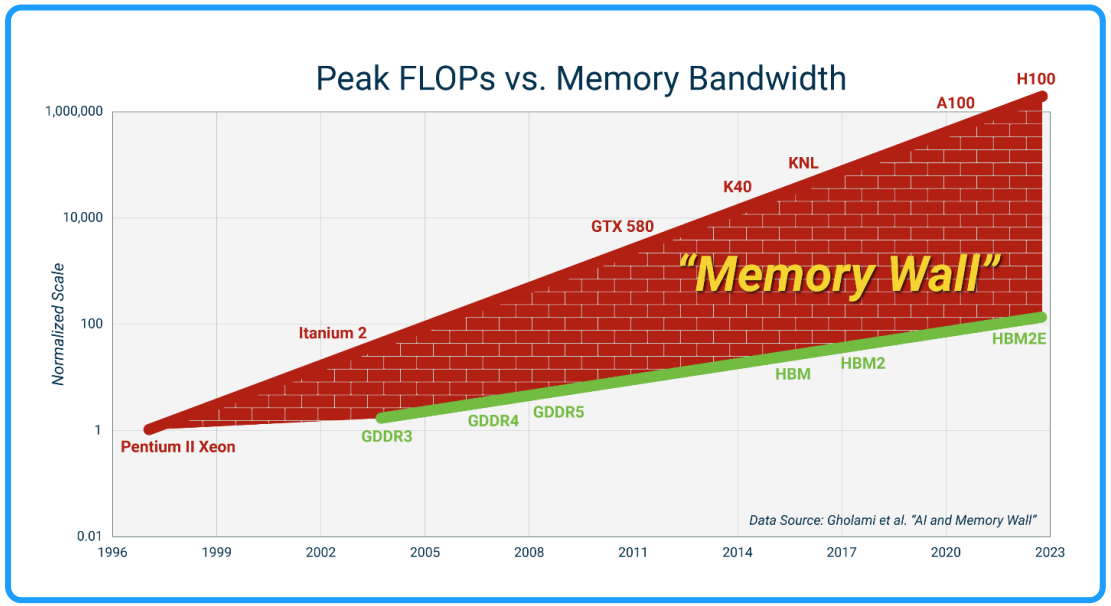
The Memory Wall

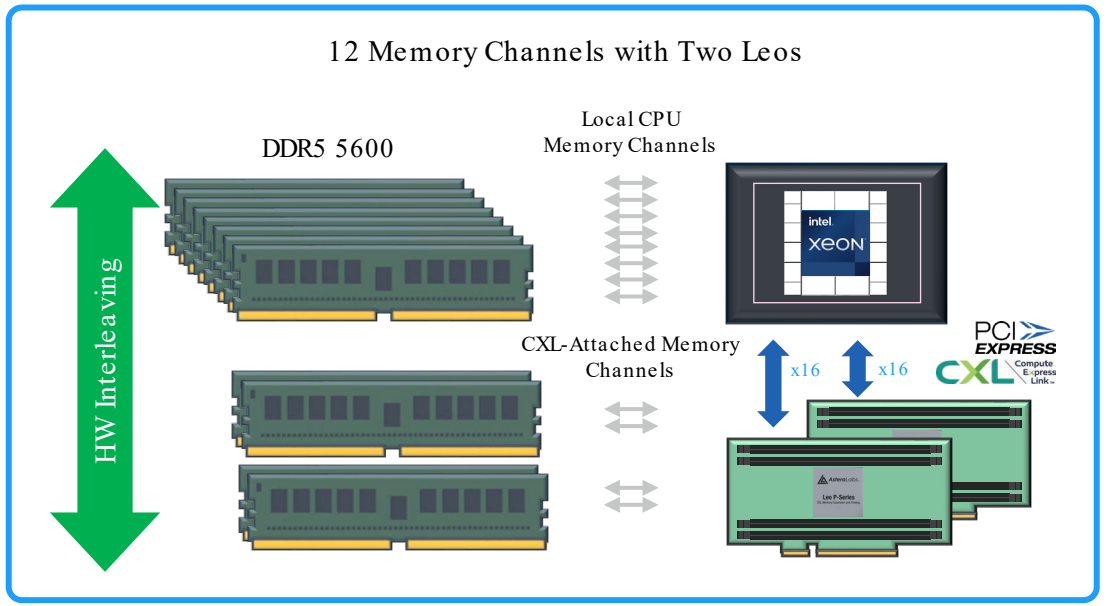
Challenges with Previous Attempts

1. Limited scalability of memory BW and capacity
2. Significant memory latency delta vs local memory
3. Proprietary system configuration and deployment
4. Complex software integration with popular apps

Breaking Through the Memory Wall with CXL

1. Increase server memory BW and capacity by 50%
2. Reduce latency by 25%
3. Standard DRAM for flexible supply chain and cost
4. Seamlessly expand memory for existing and new applications





Breaking Through the Memory Wall

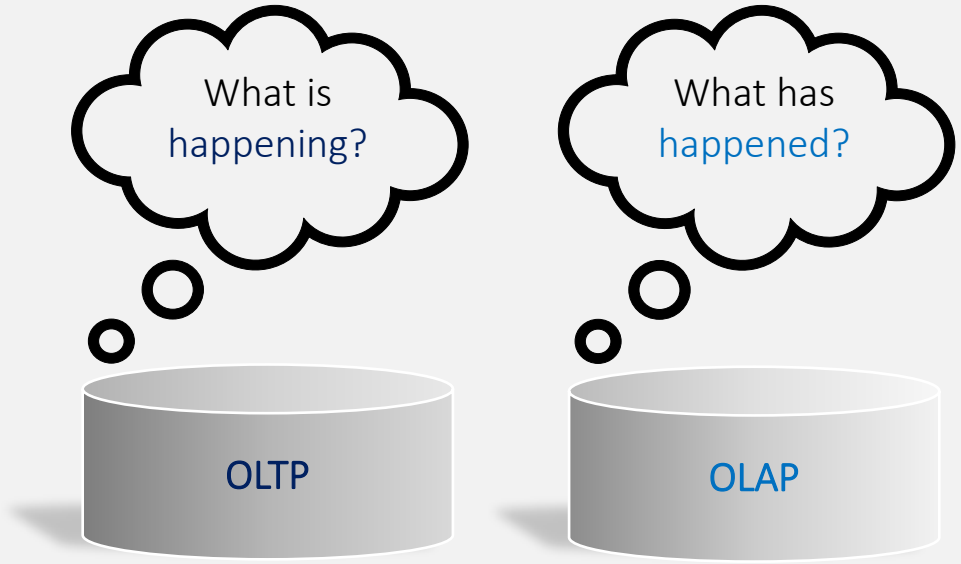
eCommerce & Business Intelligence

- **O**nline **T**ransaction **P**rocessing
- **O**nline **A**nalytics **P**rocessing

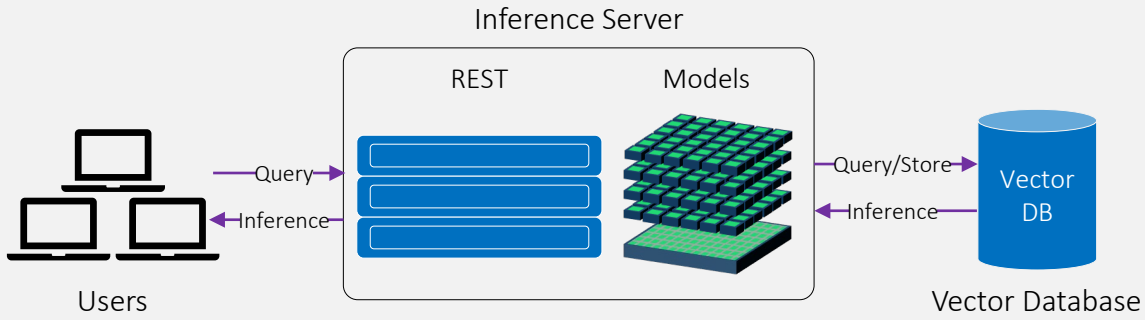
AI Inferencing

- Recommendation Engines
- Semantic Cache

Opportunity for CXL to Boost MySQL Database Performance

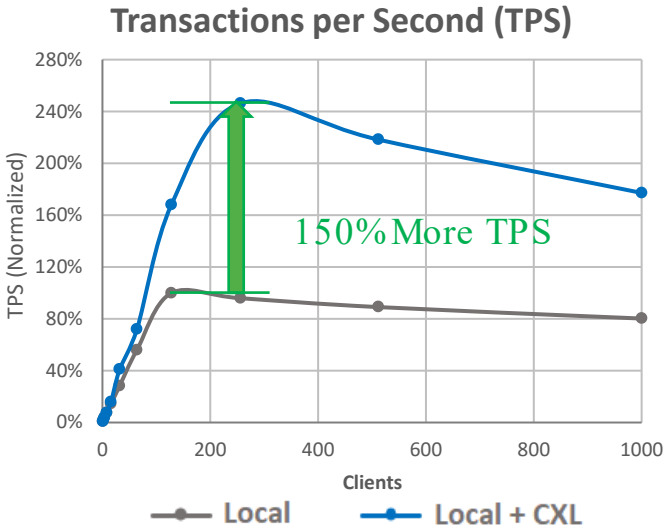


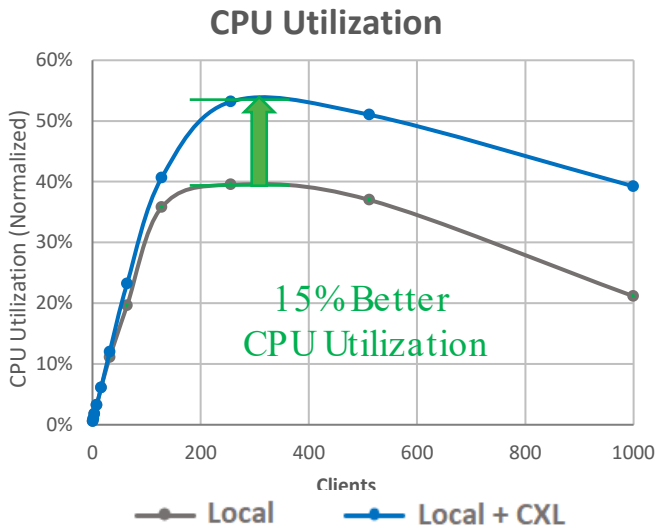
Opportunity for CXL to Boost Vector Database Performance



OLTP & OLAP Results

OLTP

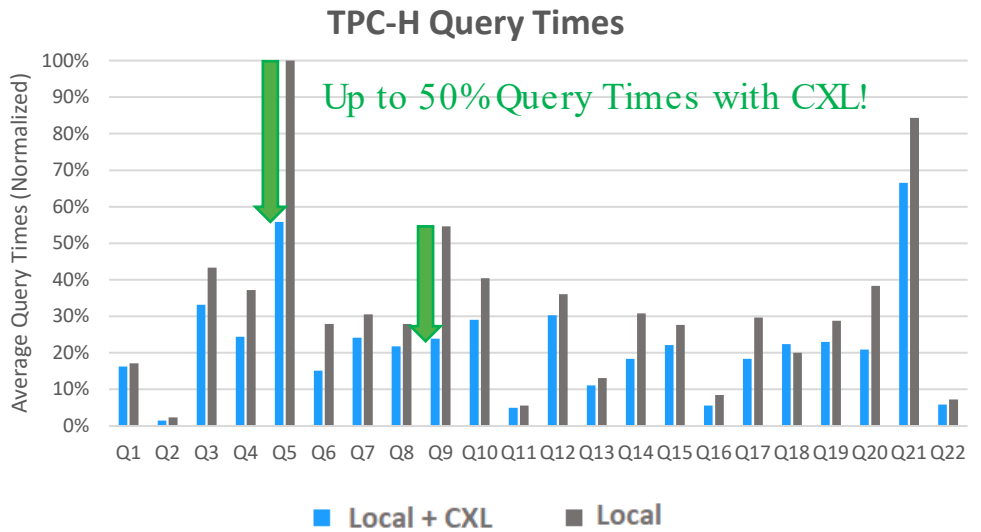




System Under Test Configuration	
CPU	4th Gen Intel® Xeon® Scalable Processor (Single-Socket)
Storage	2x NVMe PCIe 4.0 SSDs
Local	128GB (8x 16GB DDR5-4800)
Local+CXL	128GB (8x 16GB DDR5-4800) + 128GB (2x 64GB DDR5-5600)
CXL Mode	Memory Tiering (MemVerge Memory Machine)
Benchmark	Sysbench (*Percona Labs TPC-C Scripts*)

150% More TPS with 15% Better CPU Utilization

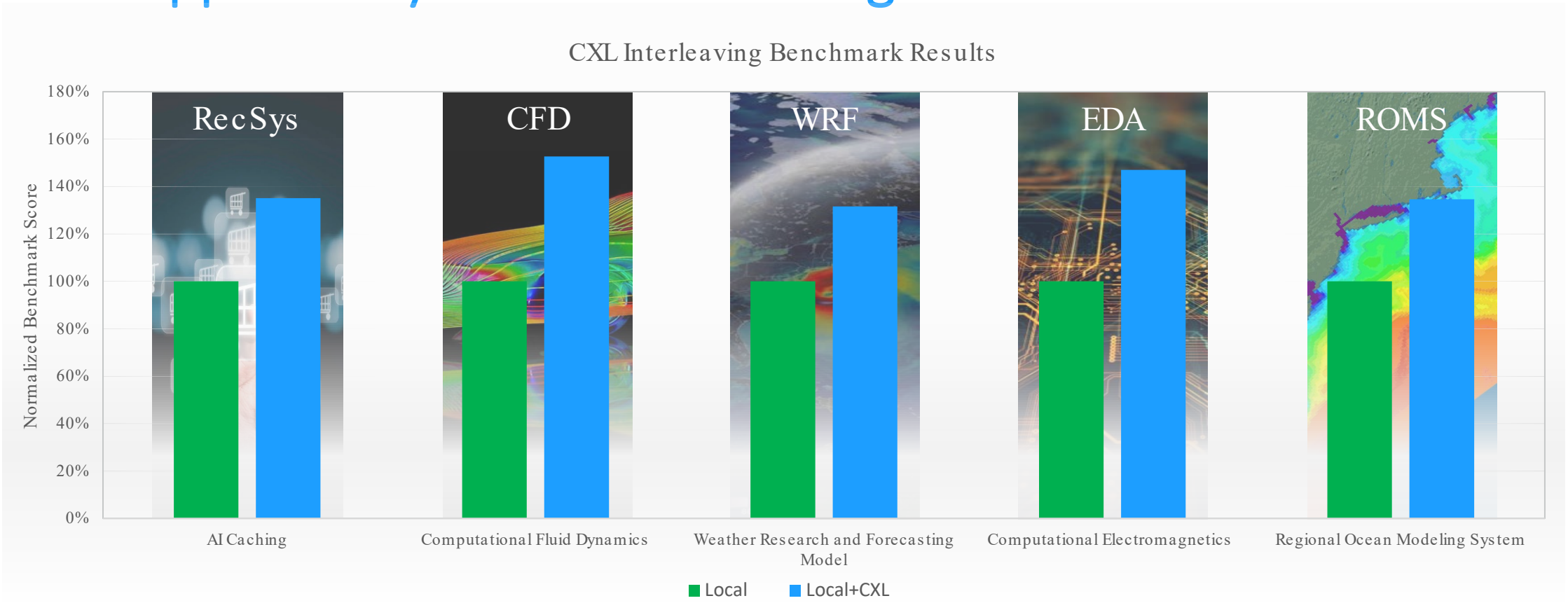
OLAP



System Under Test Configuration	
CPU	5th Gen Intel® Xeon® Scalable Processor (Single-Socket)
Storage	4x NVMe PCIe 4.0 SSDs
Local	512GB (8x 64GB DDR5-5600)
Local+CXL	512GB (8x 64GB DDR5-5600) + 256GB (4x 64GB DDR5-5600)
CXL Mode	12-Way Heterogenous Interleaving
Benchmark	TPC-H (1000 *scale factor*)

Cut Big Query Times in Half with CXL Memory

Broad Applicability of CXL Interleaving



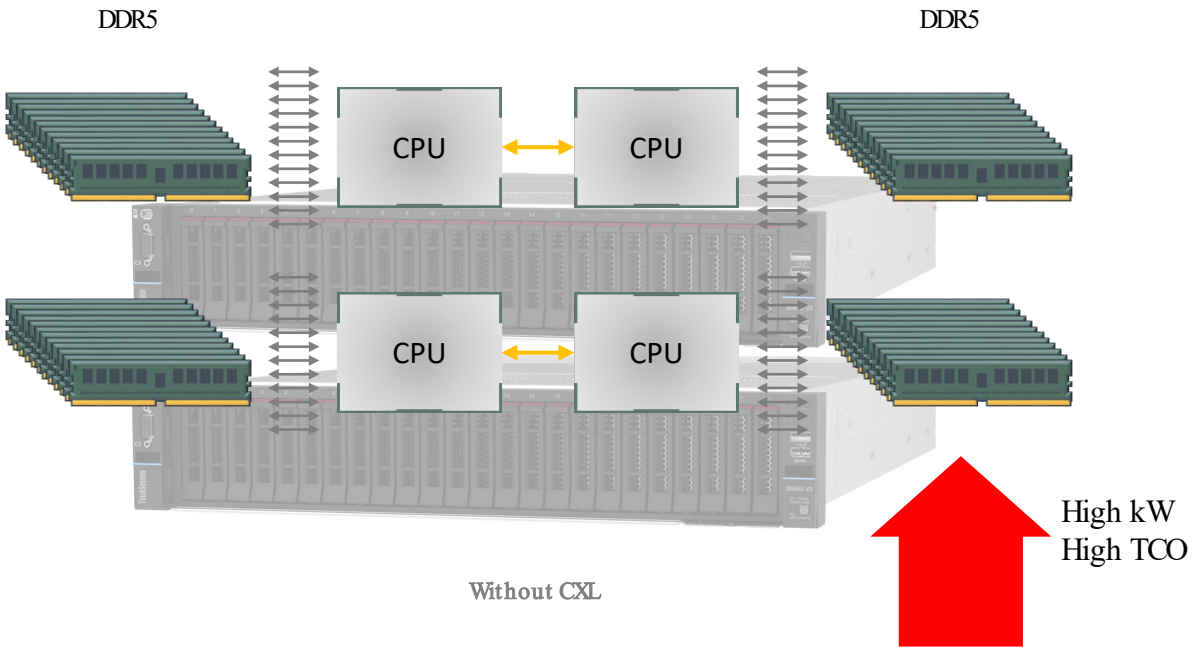
System Under Test Configuration	
CPU	Single 5th Gen Intel® Xeon® Scalable CPU
Storage	4x NVMe PCIe 4.0 SSDs
Local	512GB (8x 64GB DDR5-5600)
Local+CXL	512GB (8x 64GB DDR5-5600) + 256GB (2 Leos, 2x 64GB DDR5-5600 per Leo)
CXL Mode	12-Way Heterogenous Interleaving

CXL Interleaving Up to 50%+ Performance Improvement

Breaking the Memory Wall for Databases

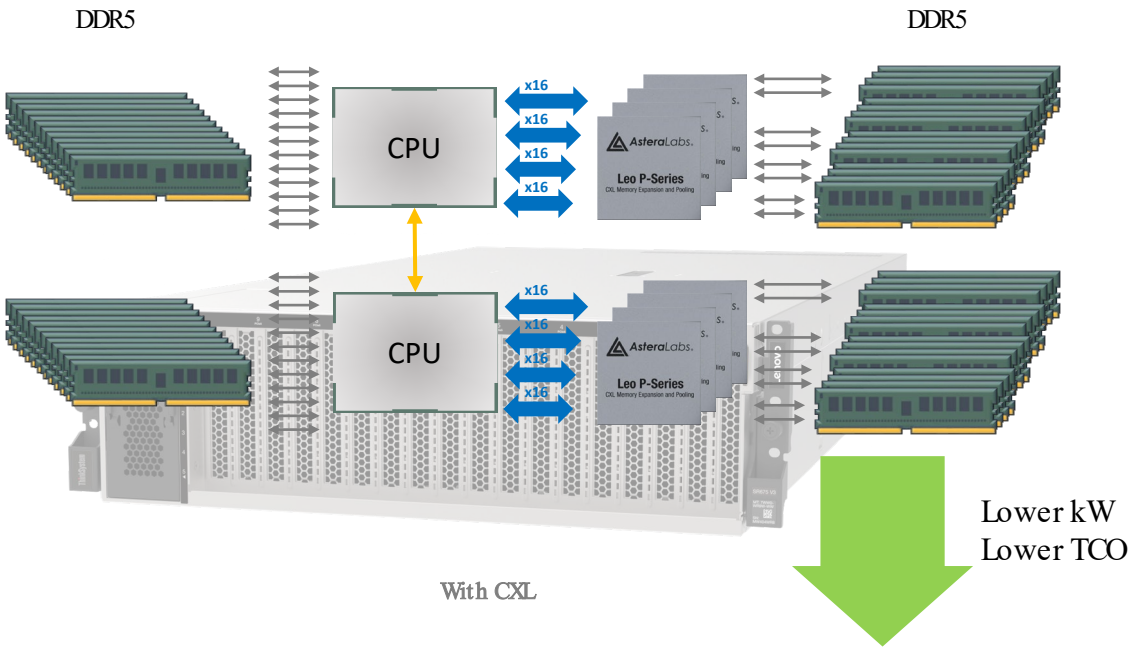
48 DIMMs with Two 2-Socket Systems

Popular Certified & Supported SAP HANA® Hardware



56 DIMMs with One 2-Socket System

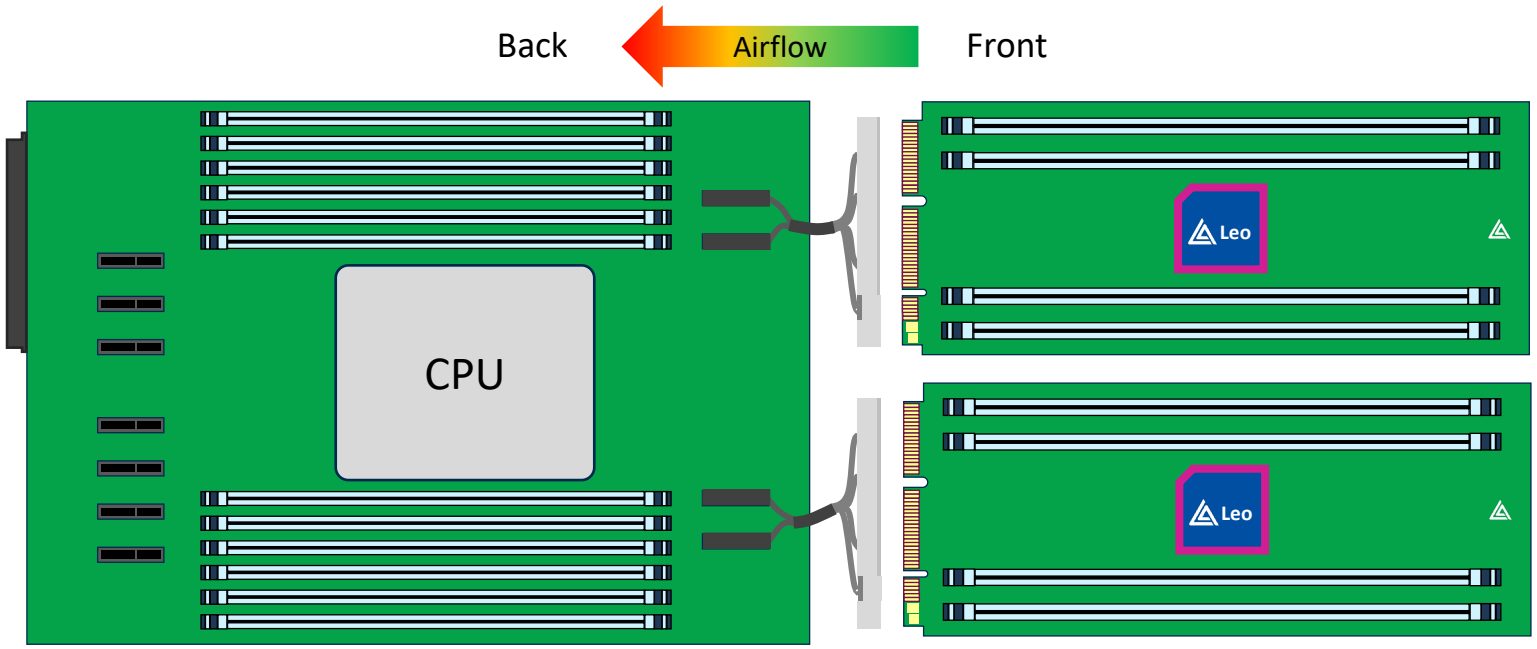
Optimized Hardware for In-Memory Databases



Interleaving across CXL-Attached Memory
2.33x memory capacity and **1.66x** memory bandwidth per socket with CXL
Lower TCO for memory-intensive application

CXL Memory Expansion for Hyperscalers

- 2 PCIe 5.0 x16 add-in cards for memory expansion per **M-DNO** (**D**e**N**sity **O**ptimized) HPM
- Each PCIe 5.0 x16 card with an MXIO cable connector



Target Use Case

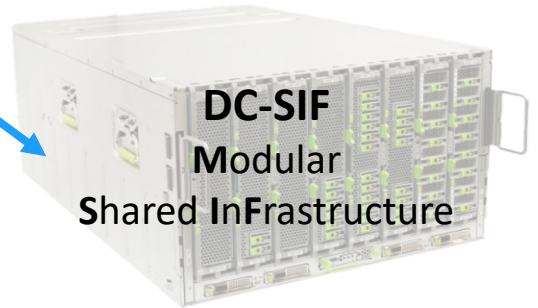
Mode: Low-latency memory expansion
Config: 2DPC SW-tiering or 1DPC HW interleaving
Apps: In-memory databases, semantic cache

Component Form Factor

Design: Coplanar add-in card
Connector: PCIe 5.0 x16 (SFF-TA-1033)
Memory: 2-4 DIMMs per card

System Form Factor

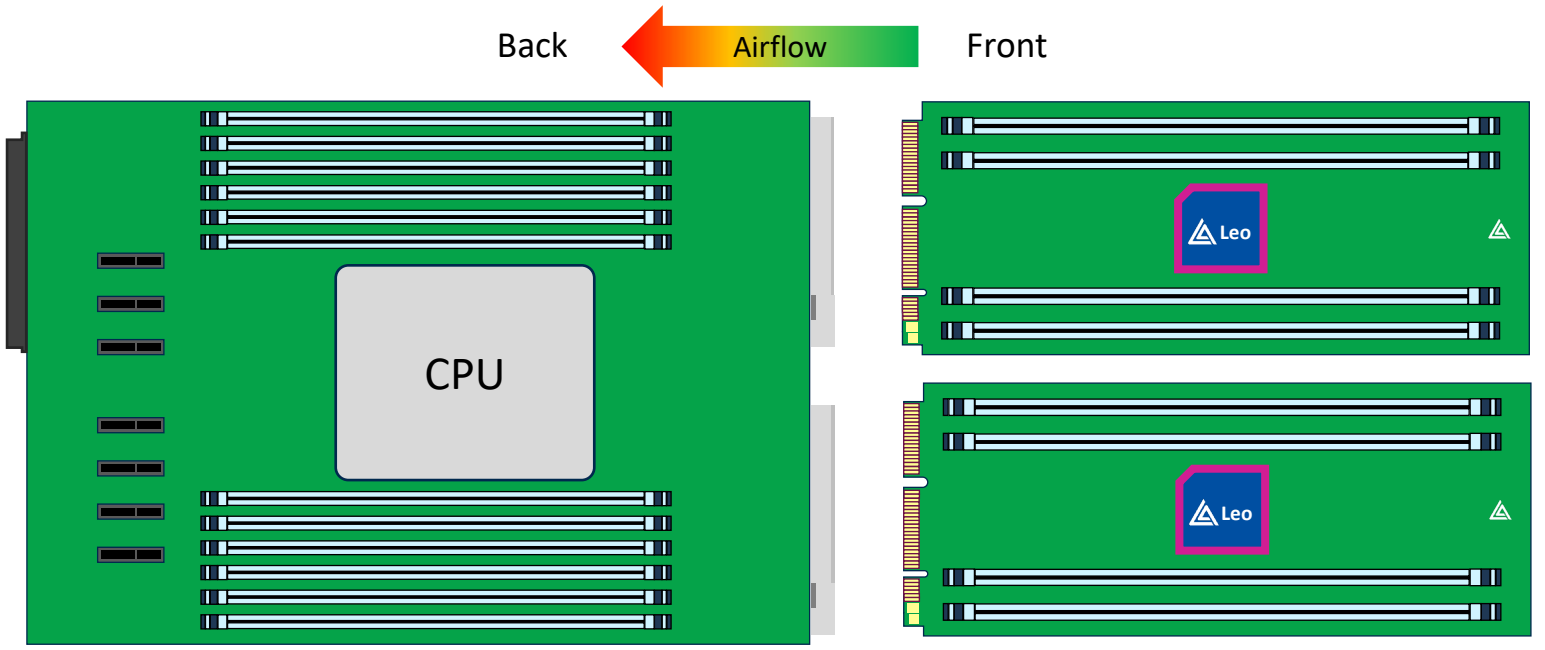
Platform: Modular Hardware System (DC-MHS)
Interface: 2x PCIe 5.0 x8 MCIO connectors
MB: Density Optimized HPM (M-DNO)



Coplanar High-Density Memory Expansion with Cold-Swap Support

CXL Memory Expansion for Hyperscalers

- 2 PCIe 5.0 x16 add-in cards for memory expansion per **M-DNO** (**D**e**N**sity **O**ptimized) HPM
- Each PCIe 5.0 x16 card with an edge connector



Target Use Case

Mode: Low-latency memory expansion
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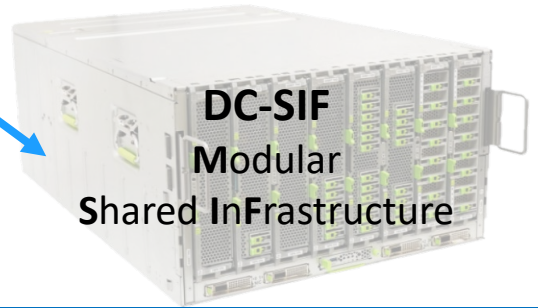
Apps: In-memory databases, semantic cache

Component Form Factor

Design: Coplanar add-in card
Connector: PCIe 5.0 x16 (SFF-TA-1033)
Memory: 2-4 DIMMs per card

System Form Factor

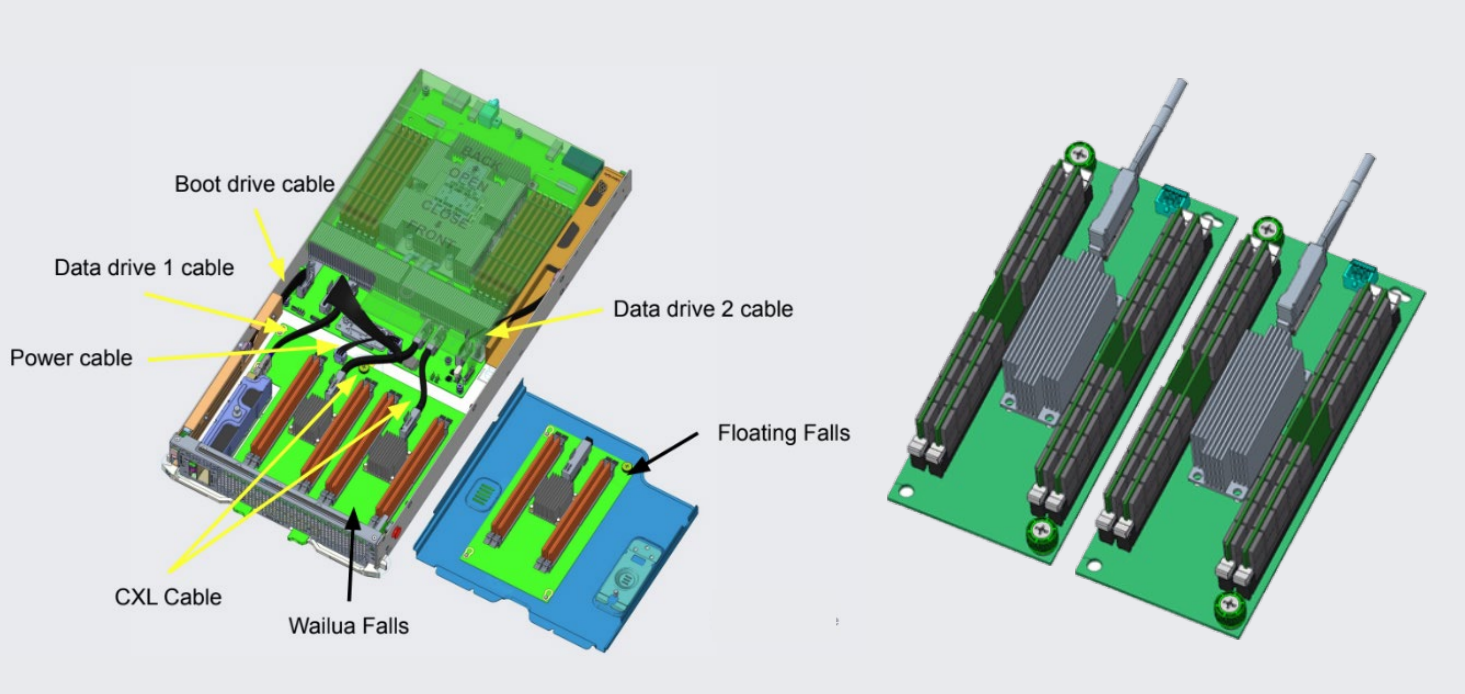
Platform: Modular Hardware System (DC-MHS)
Interface: 1x PCIe 5.0 x16 SFF-TA-1034
MB: Density Optimized HPM (M-DNO)



Coplanar High-Density Memory Expansion with Cold-Swap Support

CXL Memory Expansion for Hyperscalers

- 2 PCIe 5.0 x16 add-in cards for memory expansion per **M-DNO** (**D**e**N**sity **O**ptimized) HPM
- Each PCIe 5.0 x16 card with an MXIO cable connector



Component Form Factor

Design: Coplanar add-in card
Connector: 2x PCIe 5.0 x8 (SFF-TA-1016)
Memory: 2-4 DIMMs per board

Host Processor Module Form Factor

Interface: 2x PCIe 5.0 x8 (SFF-TA-1016)
Power: DC-MHS PIC Power (2x3, 72A + 6)
Mechanical: 175 x 74 x 35.10 mm (L x H x W)

System Form Factor

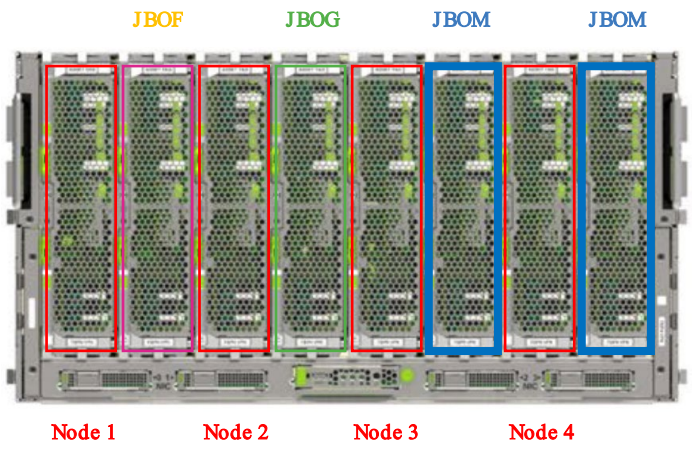
Platform: DC-MHS 7OU Chassis
Blades: 8 M-DNO HPM
Expansion: Up to 8 DIMMs per Blade

Coplanar High-Density Memory Expansion with Cold-Swap Support

Modular Shared Infrastructure (M-SIF)

OCP Alignment with DC-MHS:

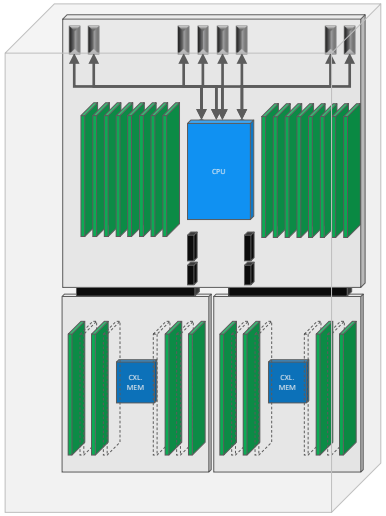
- Flexible CXL Expansion Options (M-DNO)
- Shared Elements with CXL Support (M-SIF)
- Standardized DIMM Support
- Memory Expansion for High-Density Systems
- High Power Connector (200W-600W)

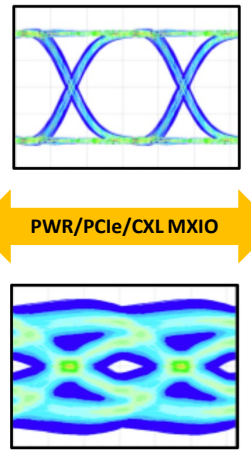


Challenges:

- Signal Integrity
- Link Bifurcation & Configuration
- Latency/Performance
- DIMM Interoperability

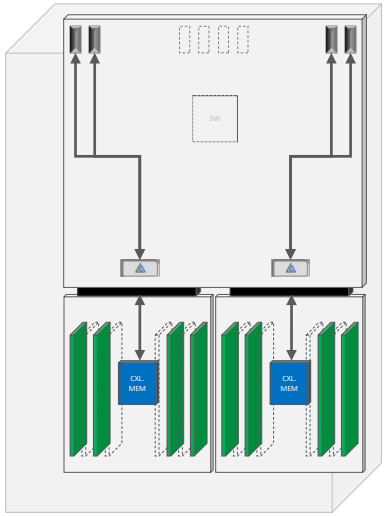
16-24 DIMMs per M-DNO





PWR/PCIe/CXL MXIO

8-16 DIMMs per M-SIF



Host Interface Board

PCIe/CXL Retimers

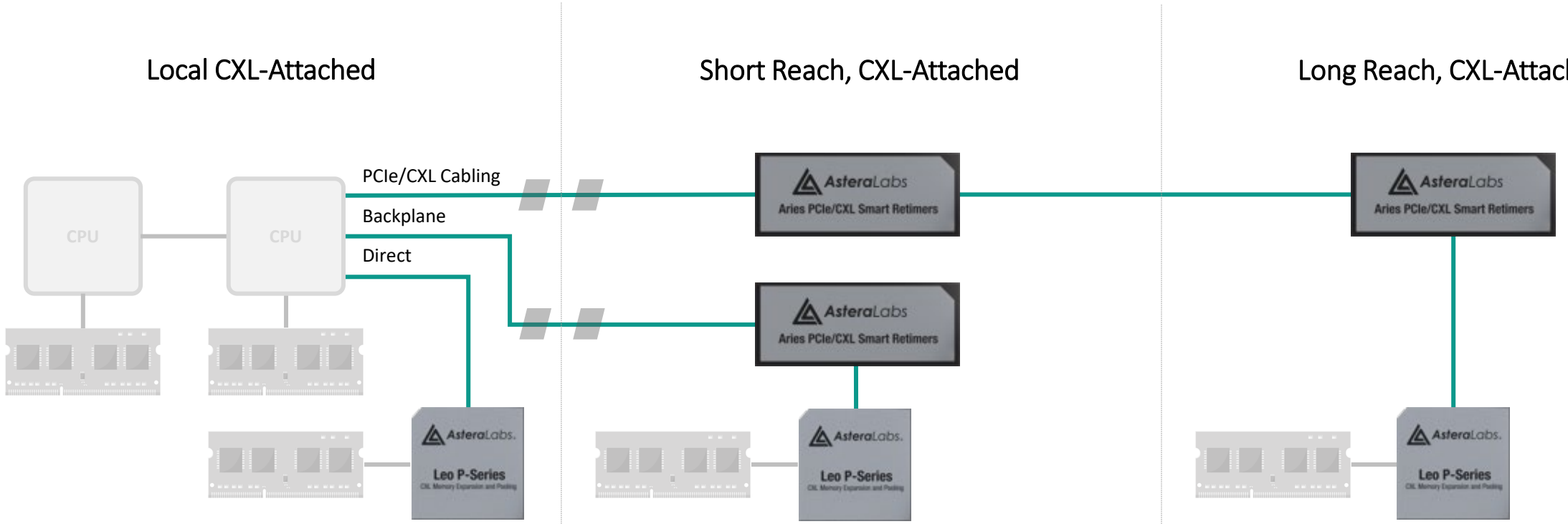
Add-in Cards

CXL Controllers

Core Element
Host Processor Module (HPM)

Shared Element
Disaggregated Resources

Enabling CXL Connectivity for M-SIF



1

- Use Case: Memory Expansion
- HPC and AI Inferencing
- MB / PCIe / MXIO Connectivity

2

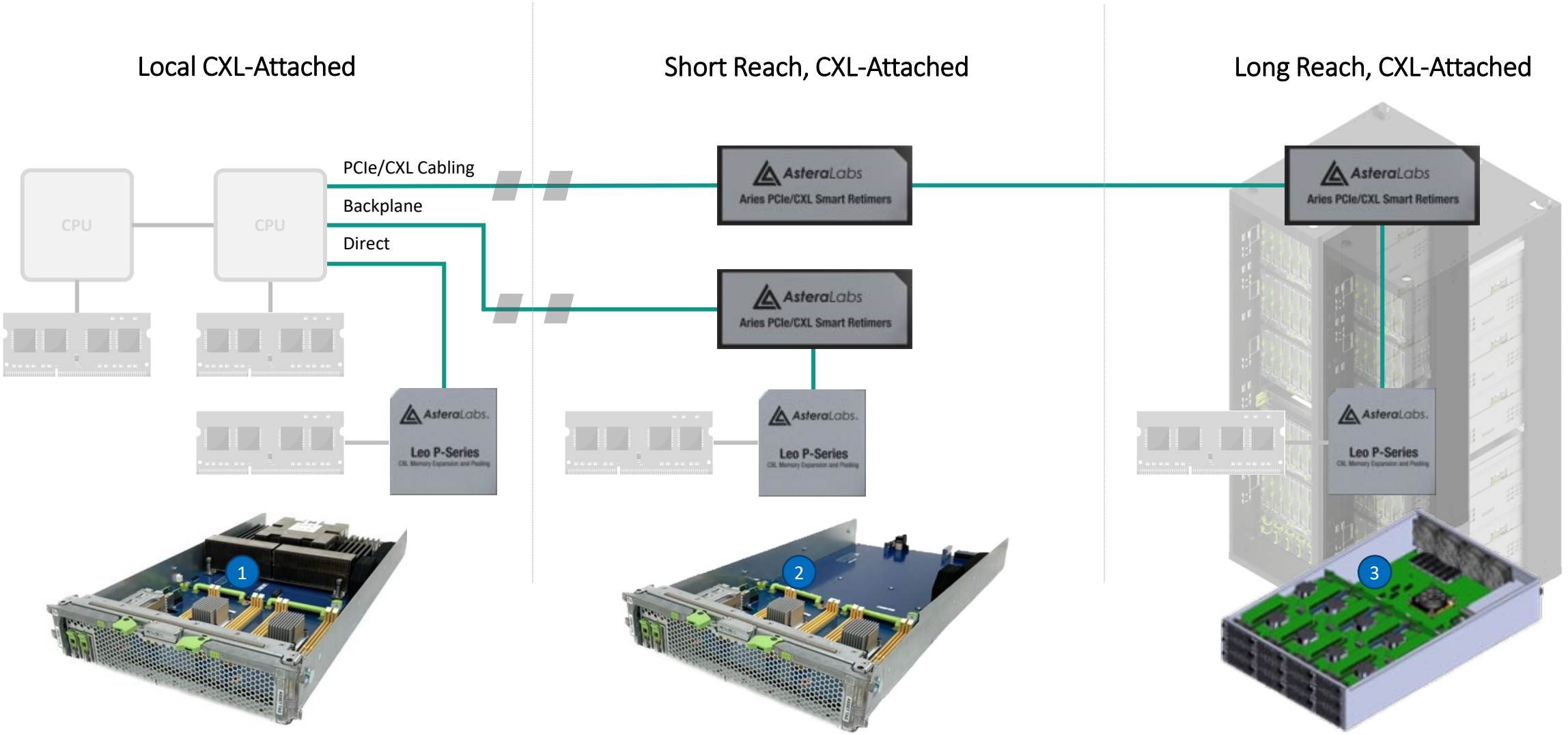
- Use Case: JBOM Enablement
- Enterprise In-Memory Database
- MXIO or Backplane Connectivity

3

- Use Case: Shared/Pooled Memory
- Recommendation and Semantic Search
- PCIe Cabling Connectivity

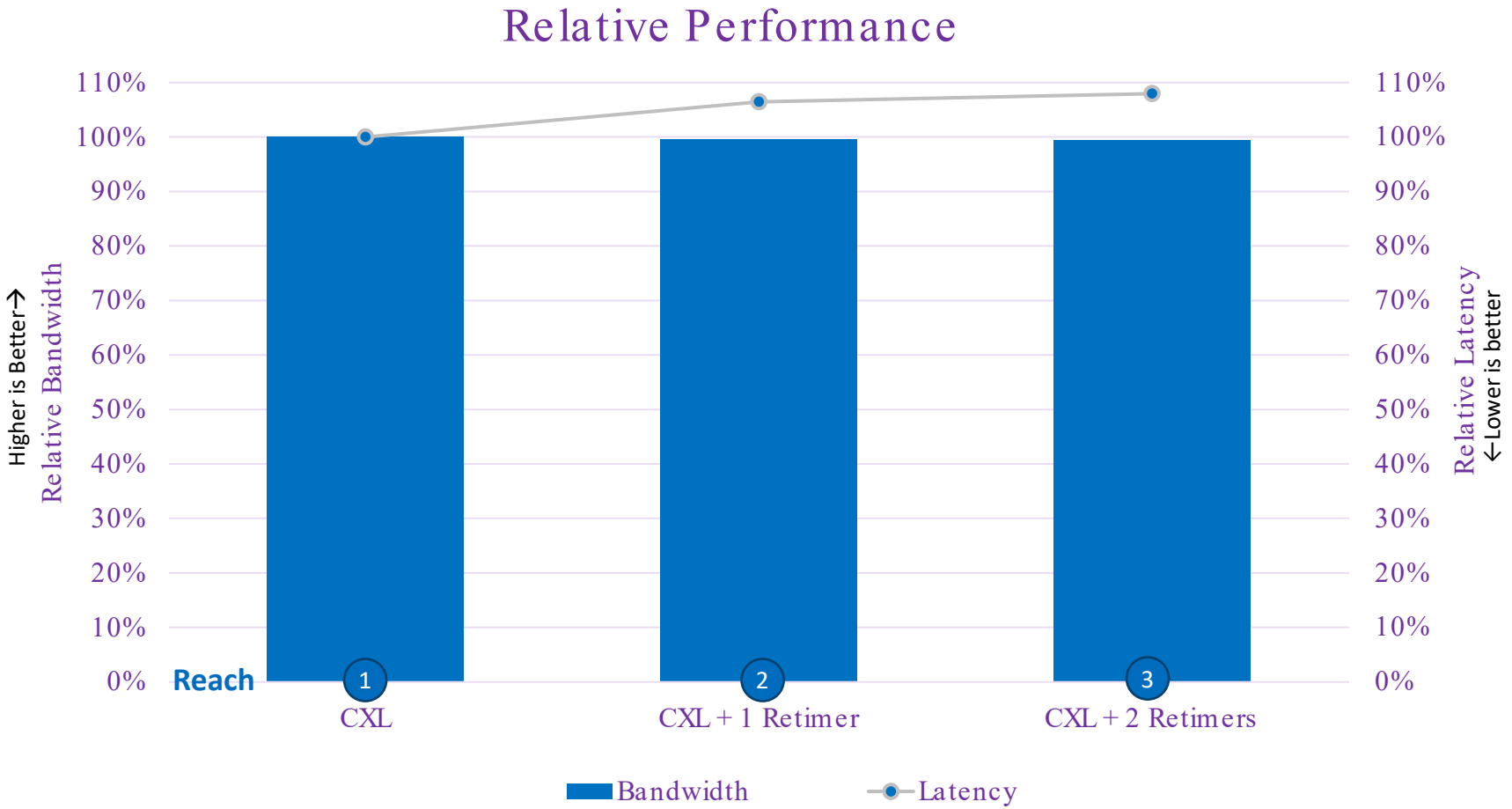
Unlocking More Capabilities

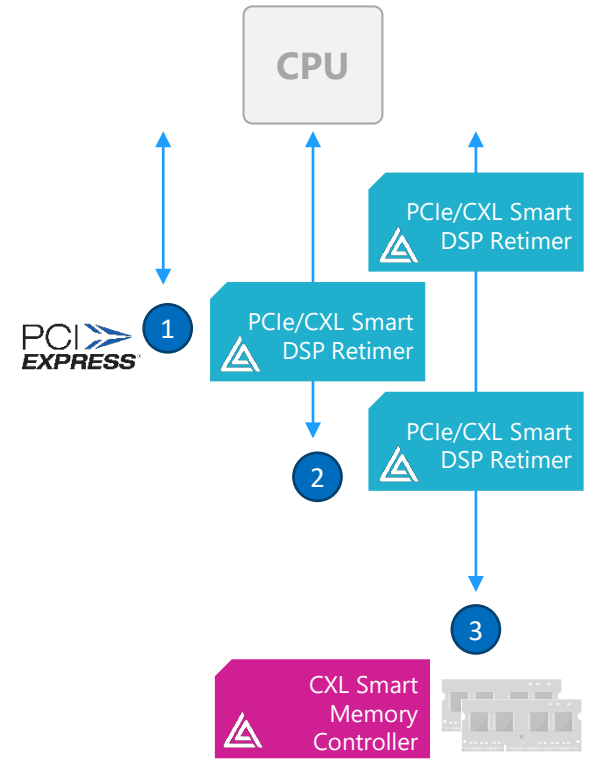
Enabling CXL Connectivity for M-SIF



Unlocking More Capabilities

Extending Reach for PCIe/CXL Memory

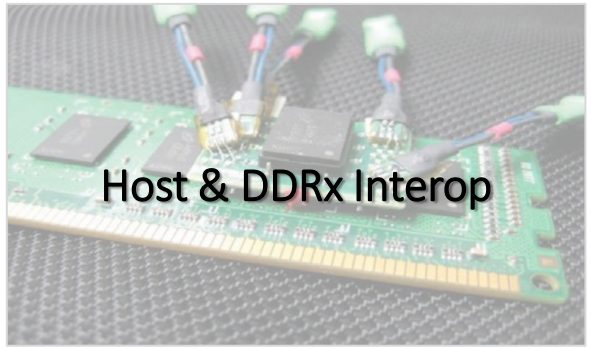


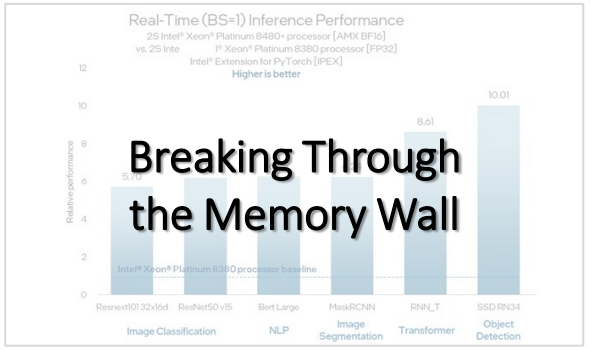


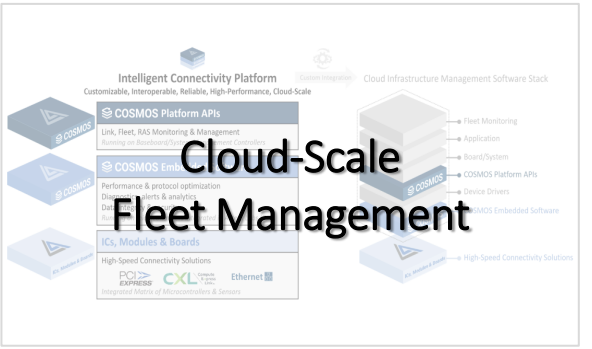
System Under Test Configuration	
CPU	5th Gen Intel® Xeon® Scalable CPU
CXL-Attached Memory	128GB (2x 64GB DDR5-5600)
OS	Linux Ubuntu 22.04
Benchmark	Intel MLC (Memory Latency Checker)

Optimizing High Performance & Latency Sensitive Applications through a Total Solution

Ecosystem Enablement



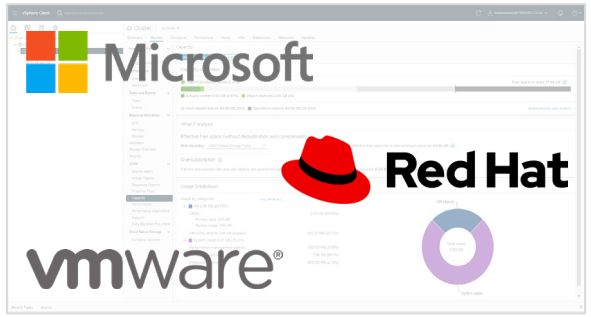


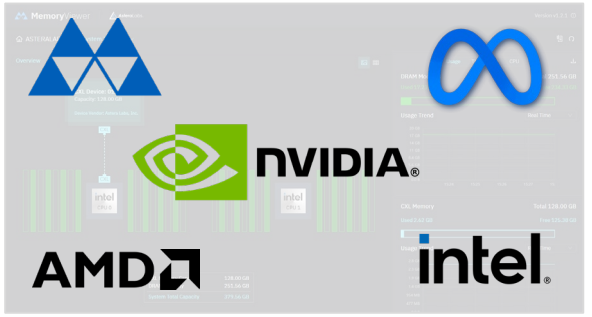


- CXL Discovery and Allocation
- DIMM Stability & Performance
- OS Development & Feature Testing

- CXL Resource Management
- High Performance HW Interleaving
- High-Capacity Memory Density Tiering

- COSMOS & DMTF Redfish® Support
- CXL 2.0 RAS & Telemetry
- SW Integration & Orchestration



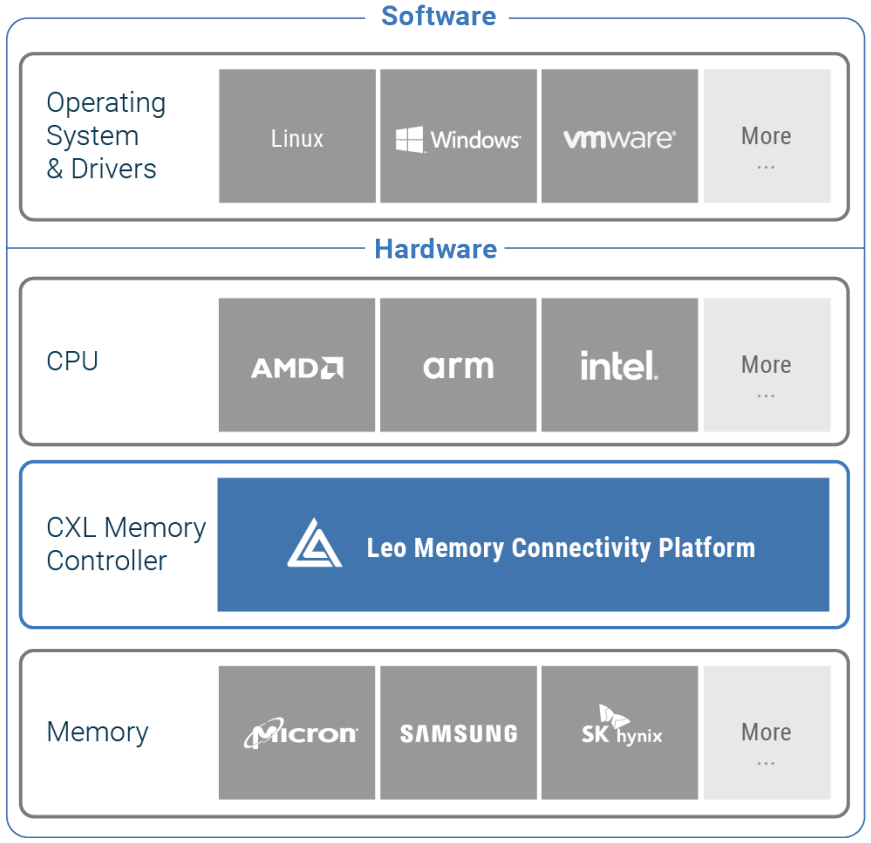


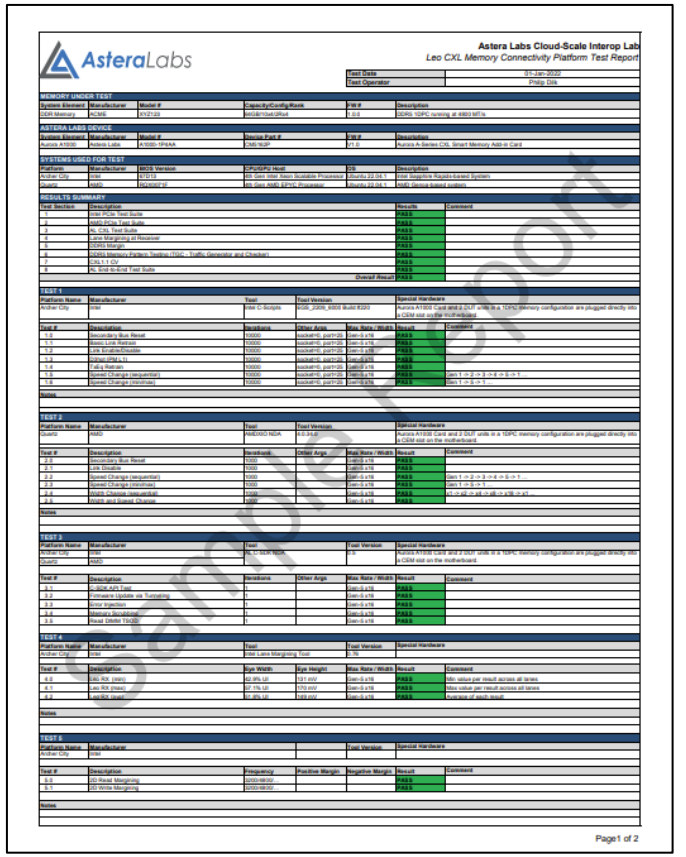
Cloud-Scale Interop Lab Sample Report for Leo

Example Tests

CLX Compliance Tests
- PCIe Electrical Testing
- Transaction Layer Testing
- Arbitrator and Multiplexer
- Power Management Tests

Reset and Initialization Tests
- System & Memory Tests
- DDR Tests
- Stress Tests
- Traffic Tests
- Security Tests
- RAS





Working Closely with DDR Vendors to Improve Performance & Stability

Calls to Action

Learn More

CXL Products and Specifications

- Leo CXL Memory Controller: Product Page
- OCP CXL Tiered Memory Expander: v1.0
- OCP DC-MHS/M-SIF Base Spec: v0.5

Get Engaged

CXL Management Collaboration

- OCP: CMM Proposal
- Linux: https://pmem.io/ndctl/collab

Ecosystem Alliance Contact:

- ahmed.medhioub@asteralabs.com

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