SNIA COMPUTE + MEMORY + STORAGE SUMMIT

Architectures, Solutions, and Community
VIRTUAL EVENT, APRIL 11-12, 2023

Watch Out! Memory's Changing!

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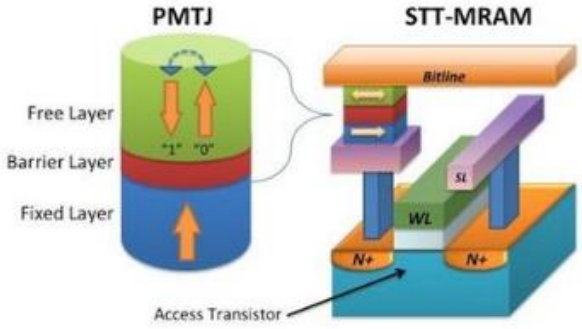
Outline

- Emerging memories are inevitable
- CXL will cause great change
- Chiplets will prevail

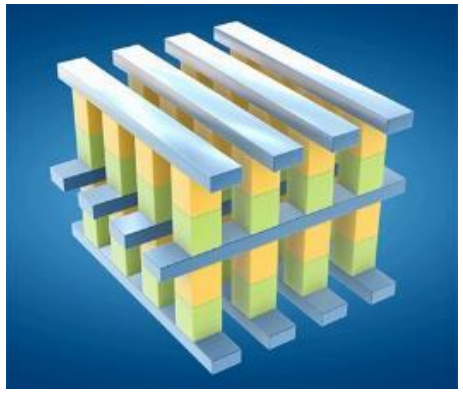
Emerging Memories

Candidates for DRAM/NAND Replacement

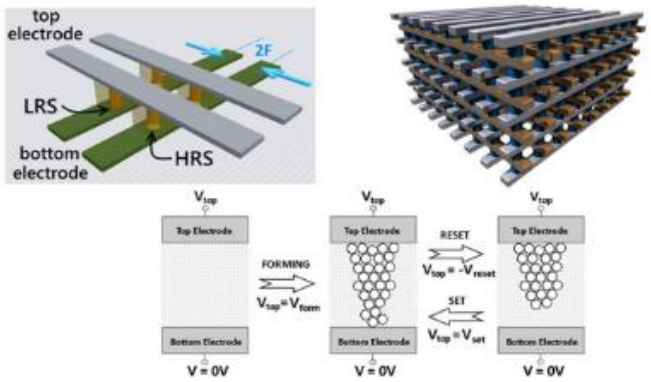
MRAM



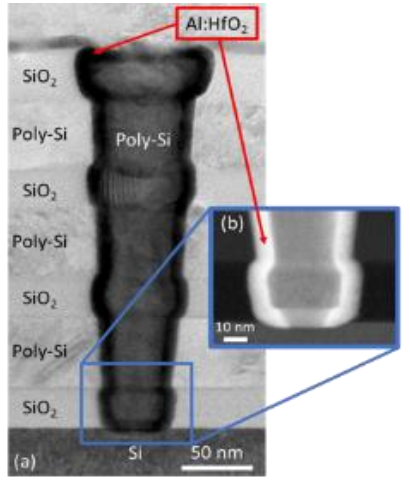
PCM



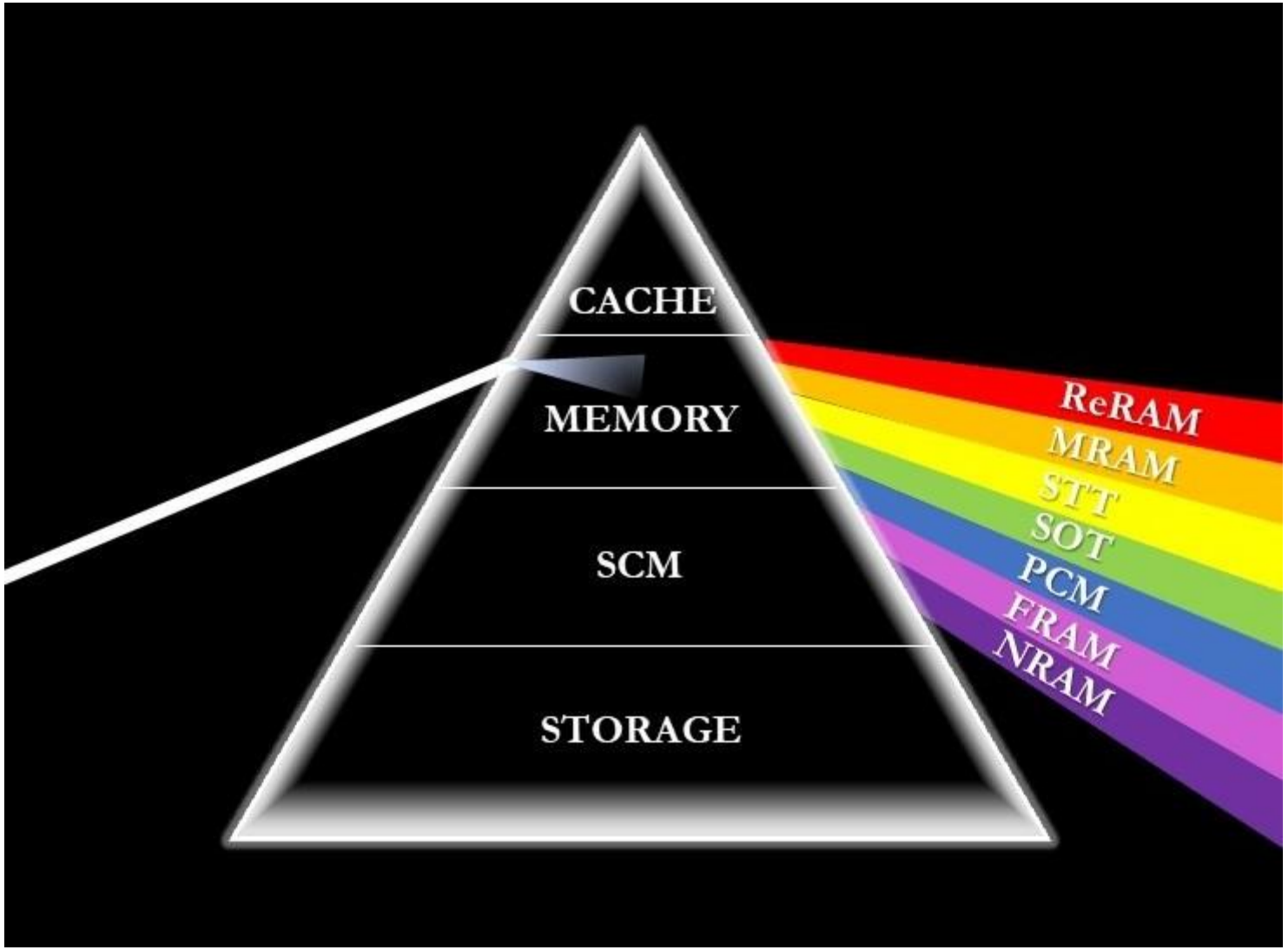
ReRAM



FRAM

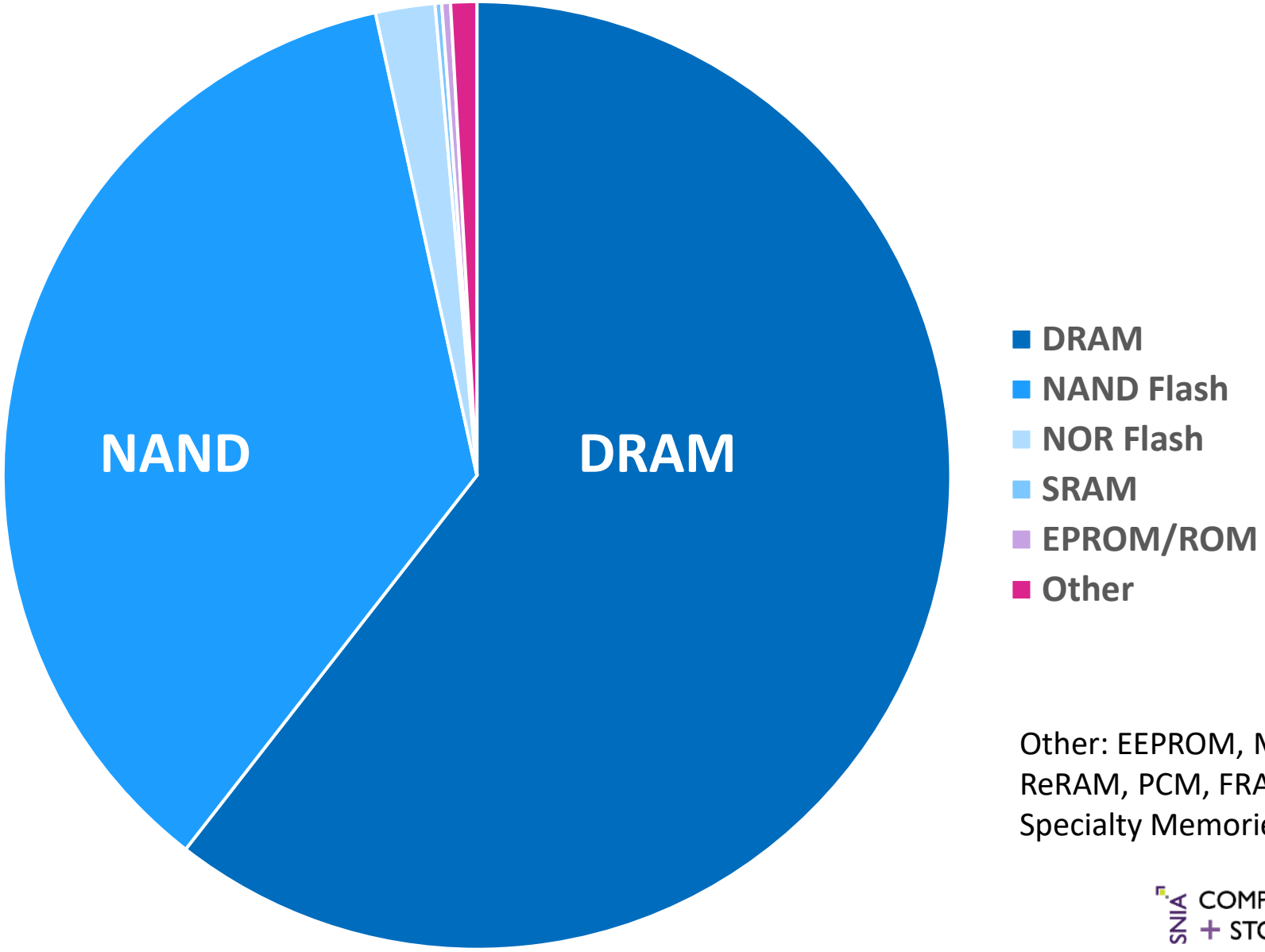


The Spectrum of Emerging Memories



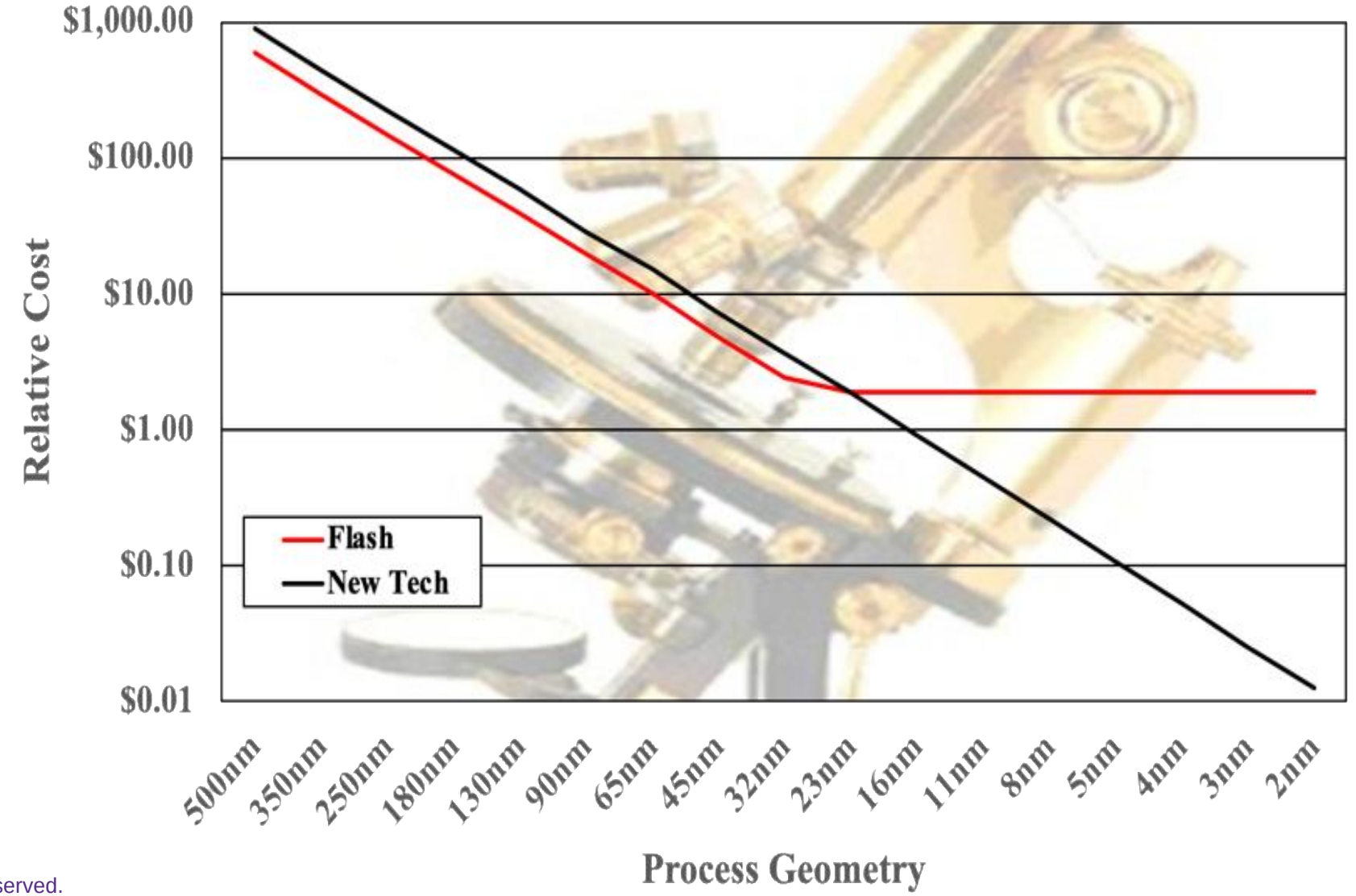
The New Spectrum Will Be More Fiscally Focused

Today's Memory Market Is Mostly DRAM & NAND Flash



Other: EEPROM, MRAM, ReRAM, PCM, FRAM, & Specialty Memories

How to Cannibalize the DRAM & NAND Markets



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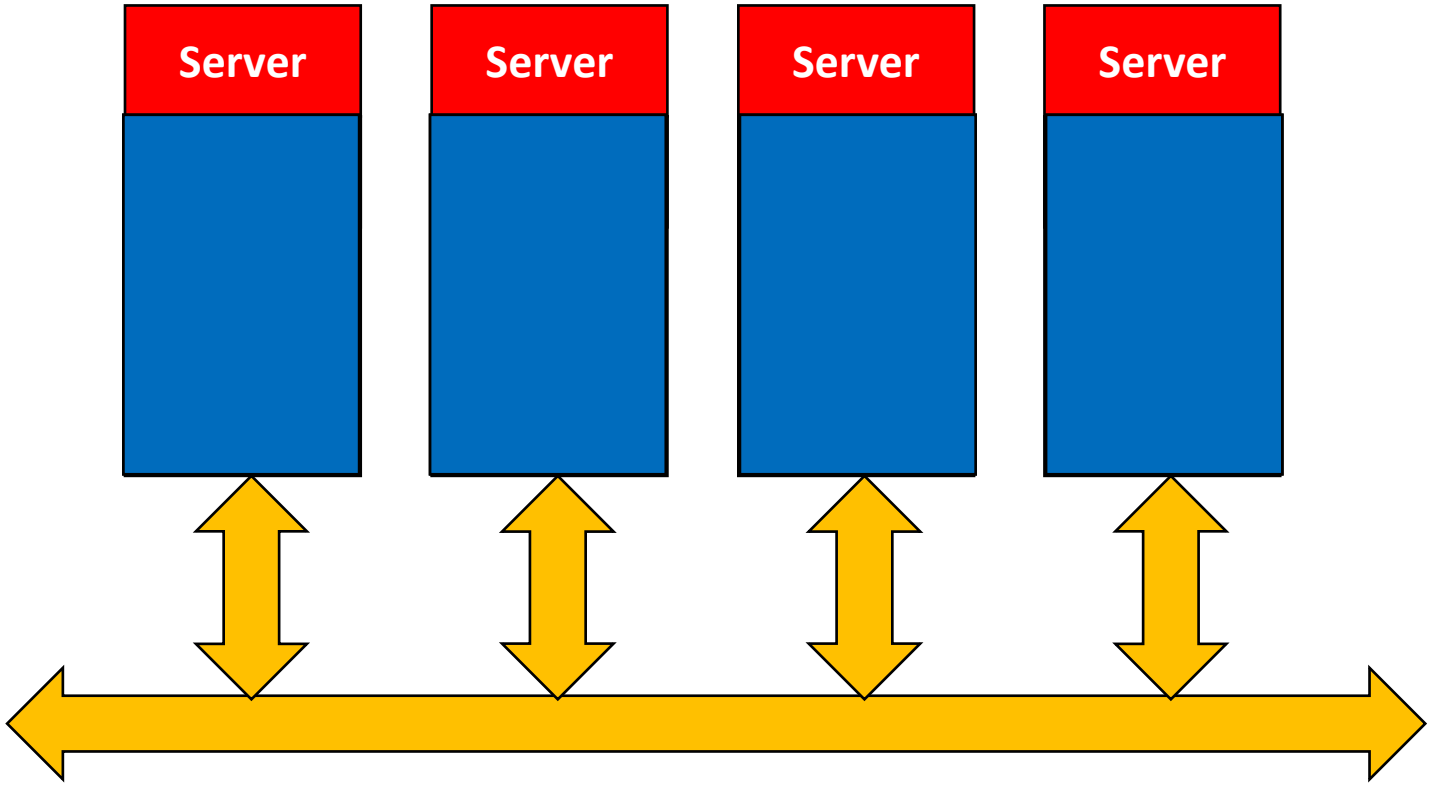
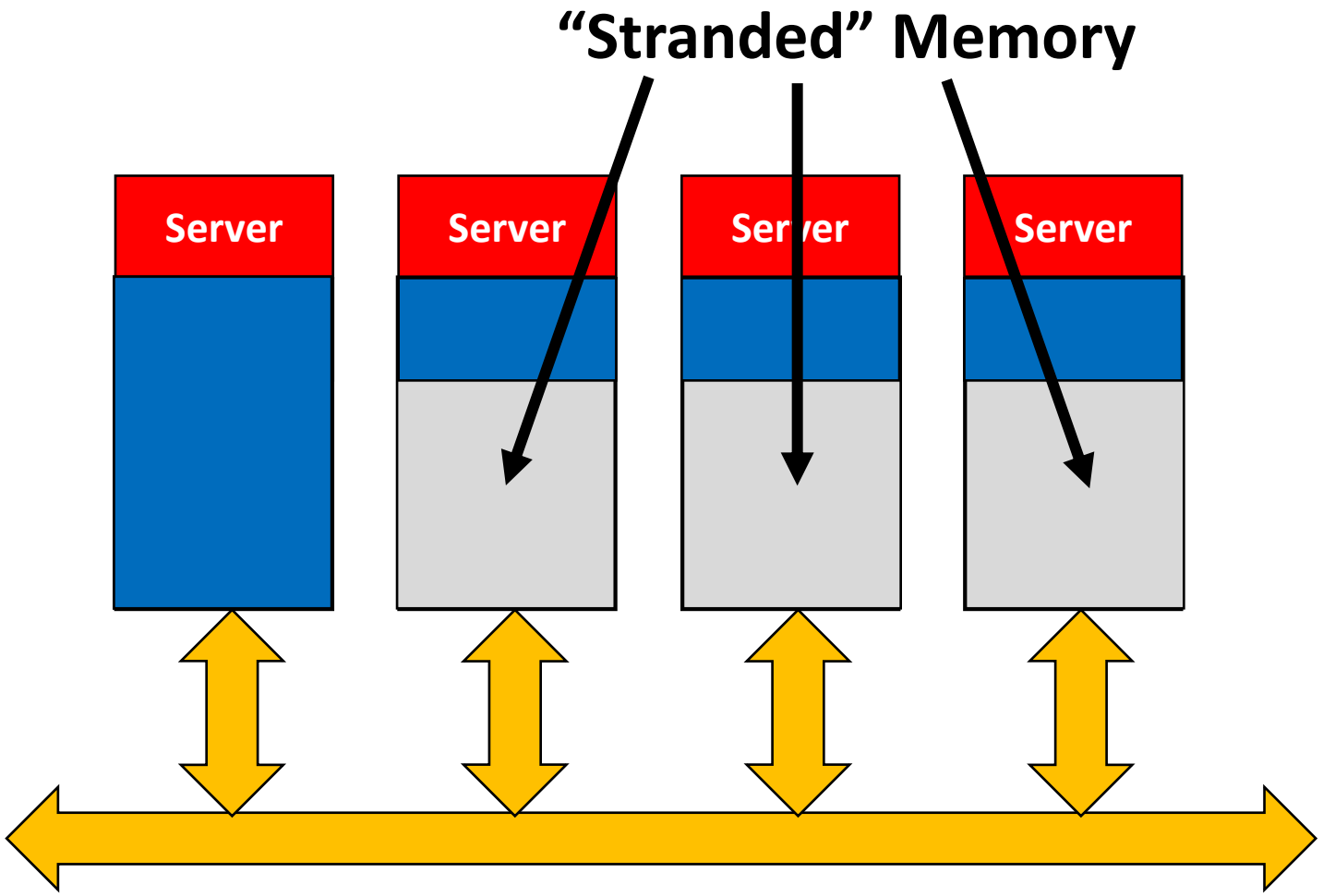
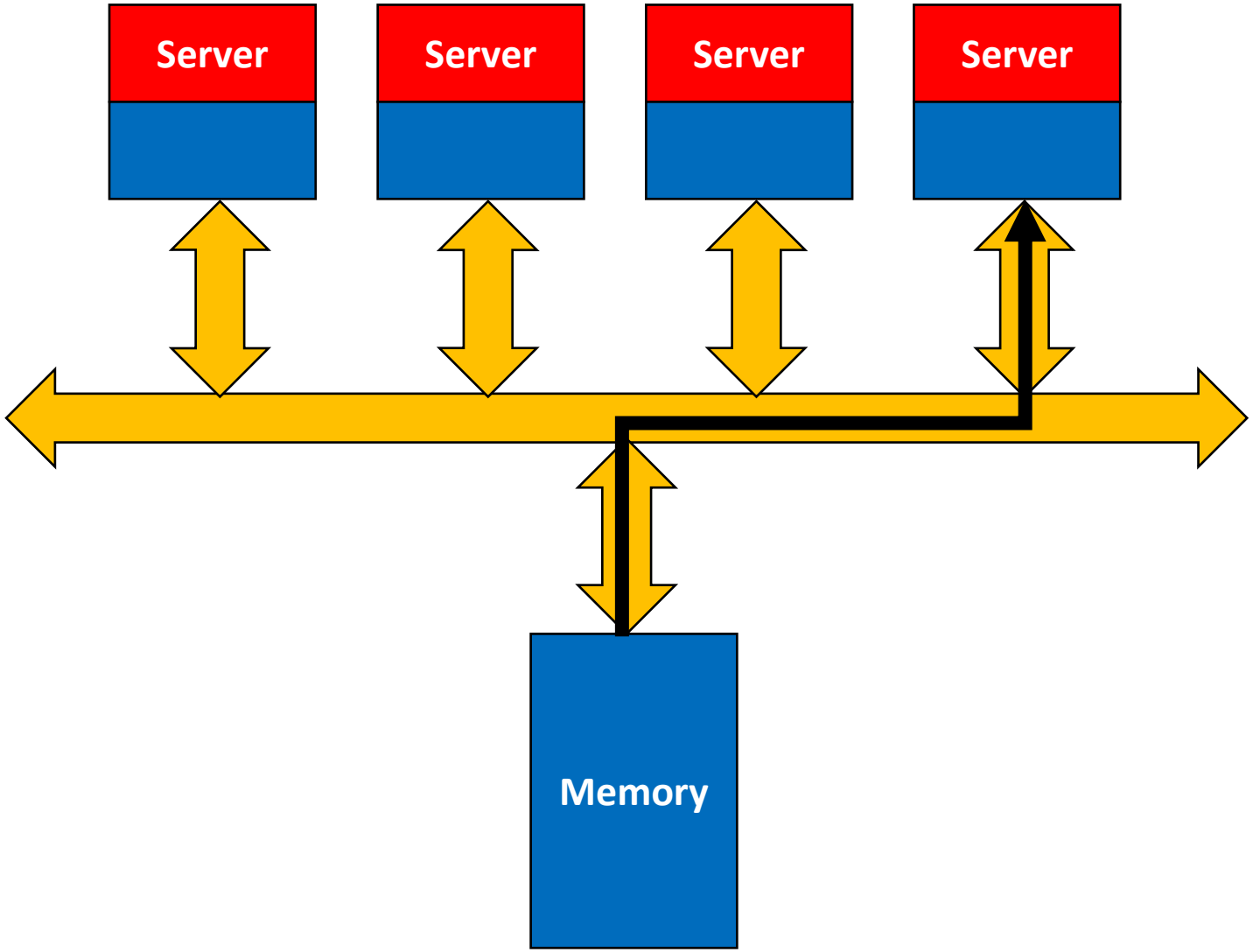
CXL: The Wave of Future Memories

CXL Will Change the Rules

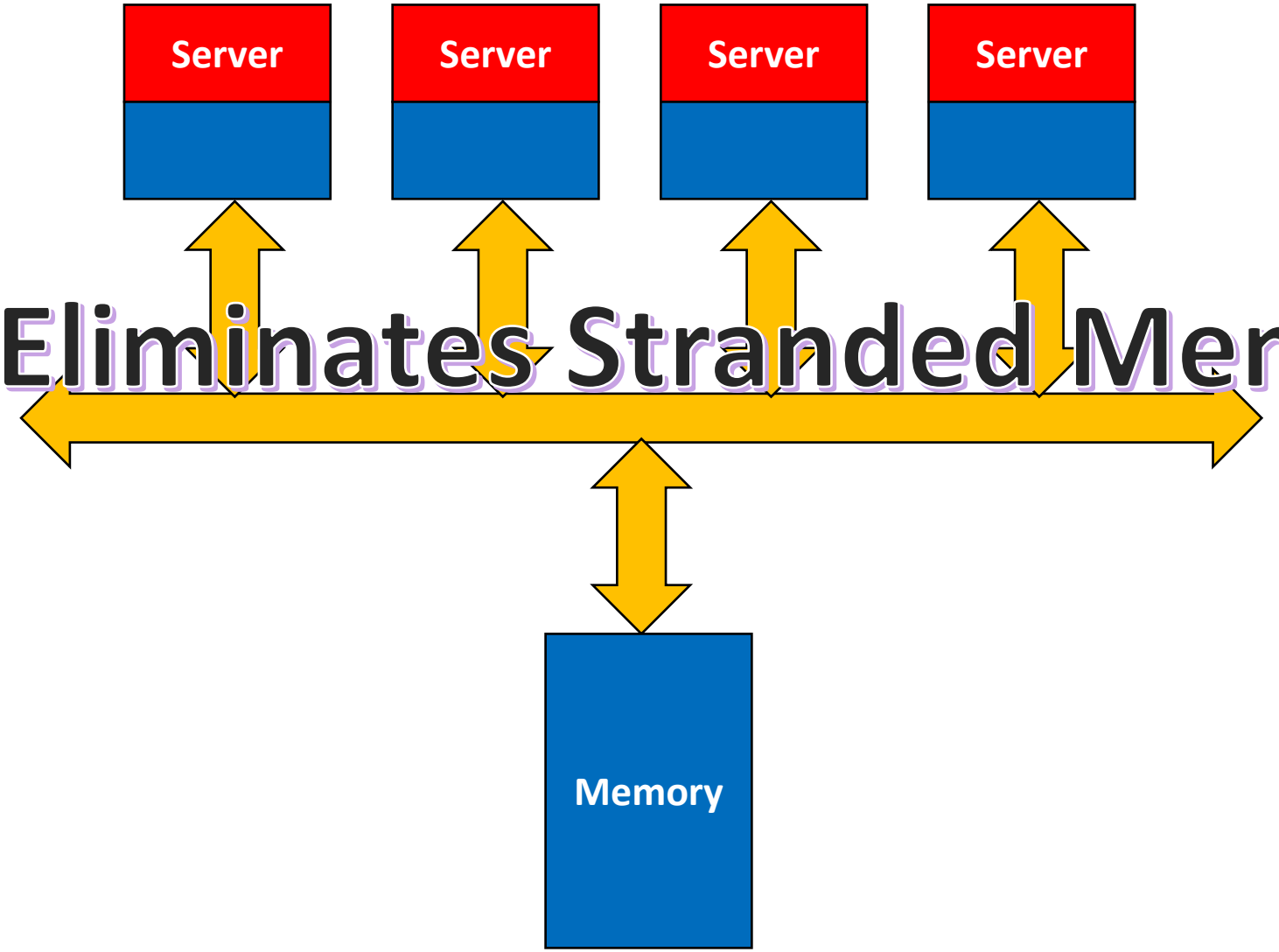
- What is CXL for?
  - Hyperscalers: Eliminates Stranded Memory
  - Memory makers: Supports enormous memory sizes







CXL Eliminates Stranded Memory



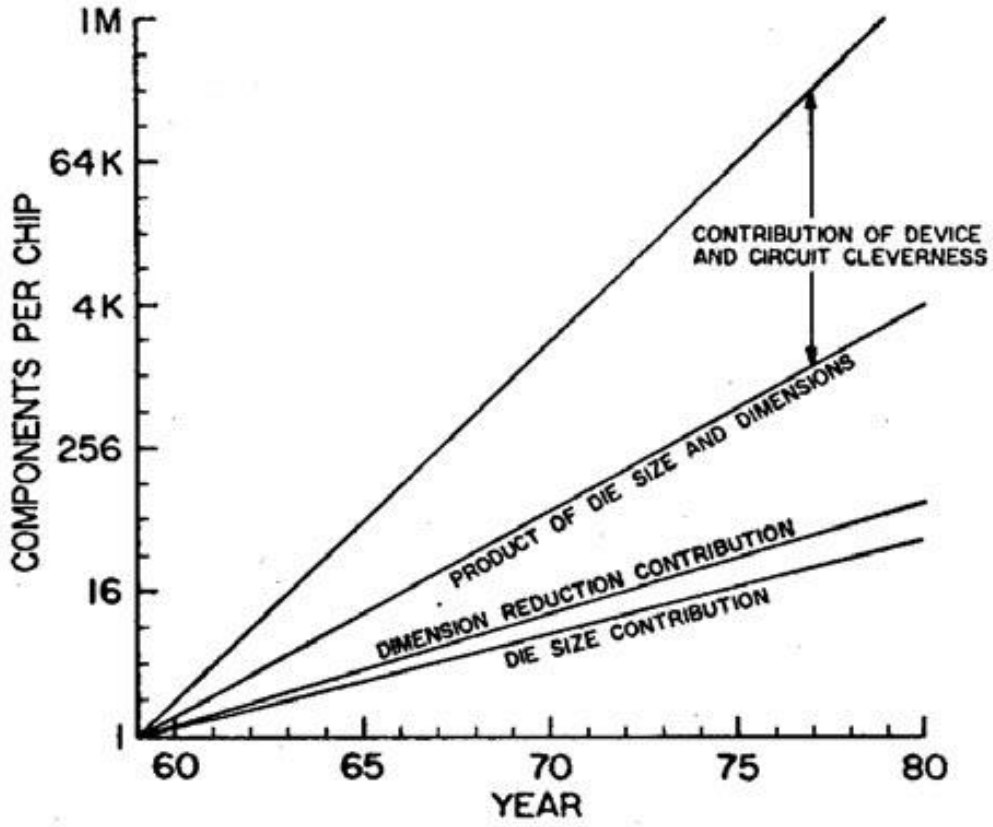
How CXL Supports Emerging Memories

- CXL manages mixed memory speeds
  - Multiple memory types can tie to a single memory channel
    - Supports NUMA: Nonuniform Memory Architecture
      - Speeds no longer must be uniform
    - Emerging memories have slower writes than reads
      - Unlike flash, they can write in place (no “Erase Before Write”)
- CXL supports persistent memory
  - Optane was one CXL application
  - Other emerging memories may fill that slot
  - Meanwhile, watch for Memory Semantic SSDs: MS-SSD

Why Chiplets Are Now Cool

Chiplets are the Wave of the Future

- Die sizes have stopped growing
  - That removes this chart's bottom line
- Processor complexity still rising
  - Where to put all those transistors?
- Chiplets "Virtually" increase die size
  - HBM is a step in that direction
  - Diverse functions can be subdivided
  - Emerging memories are a natural fit
    - Use a different process from CMOS Logic



Moore, G.E. ***Progress in Digital Integrated Electronics*** Technical Digest, International Electron Devices Meeting IEEE, 1975, pp. 11-13.

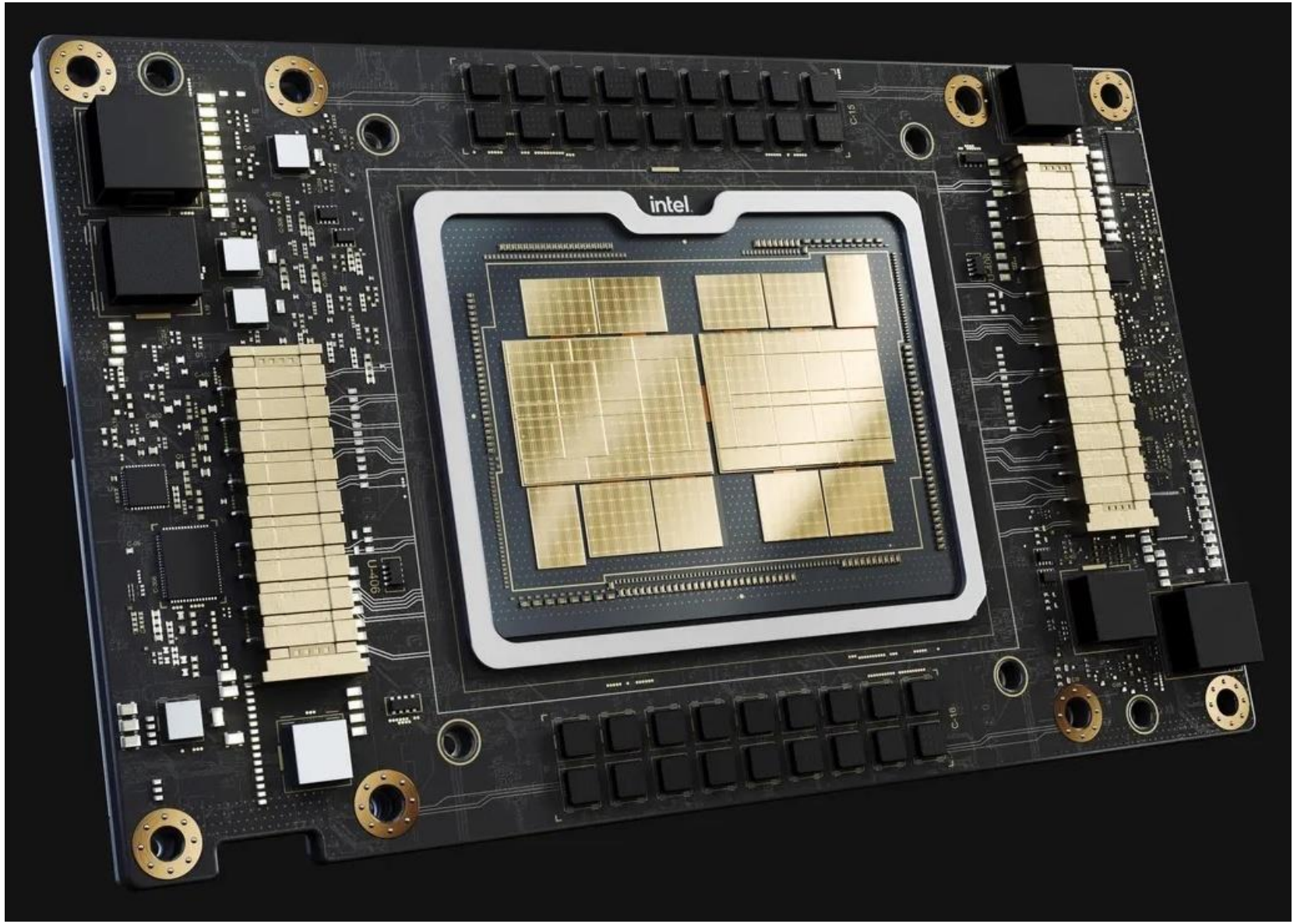


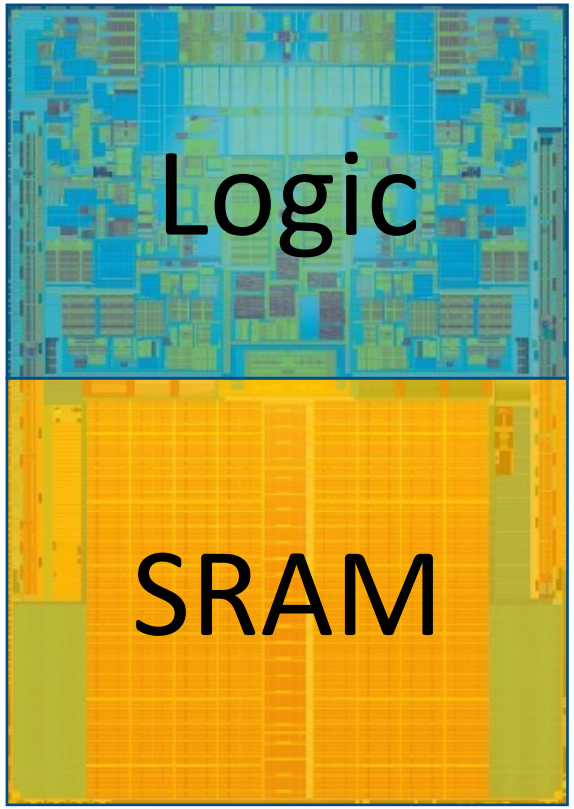
Photo Source: NVIDIA

UCIe is Based on the CXL Protocol

- UCIe = Chiplets with CXL interface
- Chiplets are encouraging for emerging memories
  - Can reduce costs vs. embedded memory
  - Provides nonvolatile option to SRAM

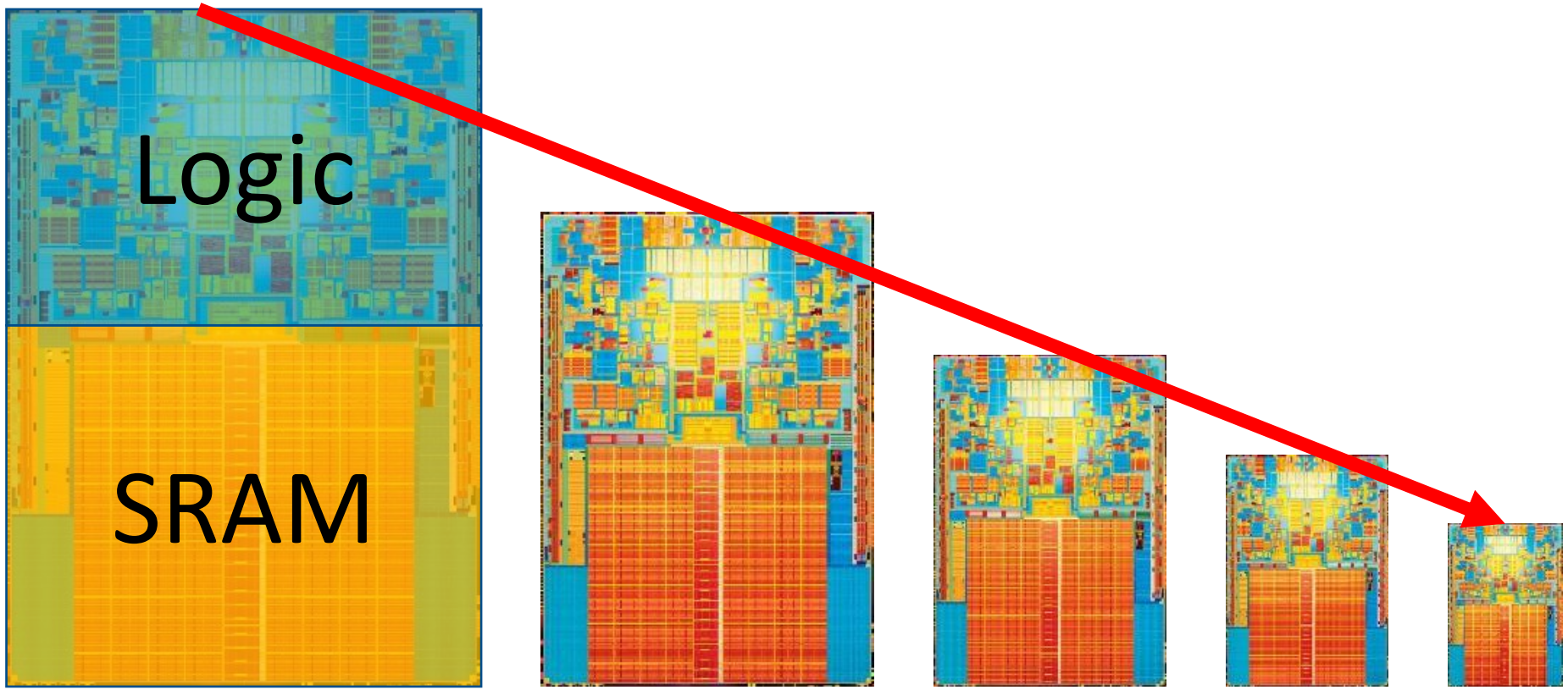
Why Chiplets Will Use Emerging Memories

- Embedded NOR stopped shrinking
- Embedded SRAM running into trouble
- Emerging Memories use different processes
  - Emerging memories shrink with process
- Embedded SRAM is the most expensive SRAM on the planet!
  - But it's fast
    - But fast can be traded off against big
    - A big slow off-chip memory chiplet can be really cheap

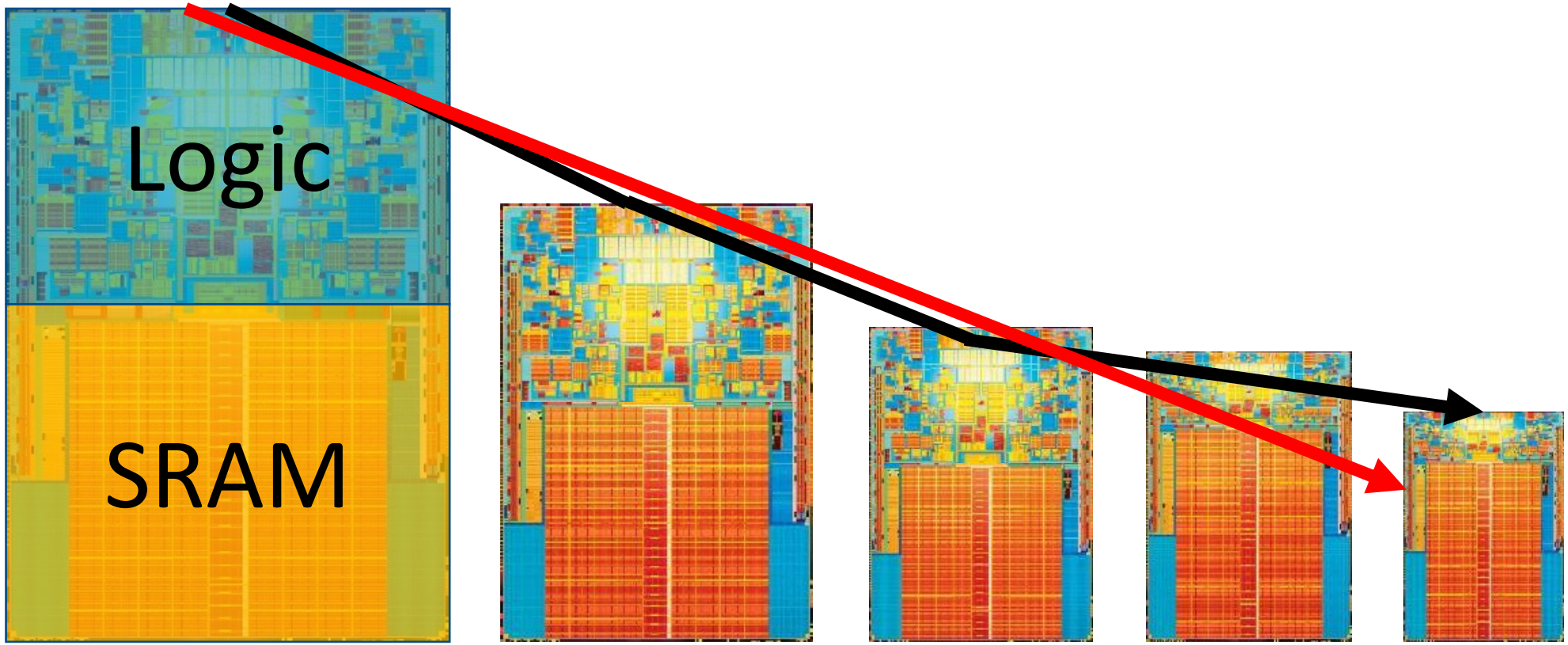


Remove the SRAM to cut this chip's cost >50%!

SRAM No Longer Scales with Logic's Process Shrinks



SRAM No Longer Scales with Logic's Process Shrinks



Summary

- Emerging memories are on their way
  - Anticipate persistent caches
- CXL will change computing architecture
  - Memory pools and persistent memory
- Chiplets will prevail
  - Emerging memories will be one important use of chiplets

Report: Emerging Memories Enter the Next Phase
https://Objective-Analysis.com/reports/#Emerging
http://www.tomcoughlin.com/techpapers.htm

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