SNIA COMPUTE + MEMORY + STORAGE SUMMIT

Architectures, Solutions, and Community
VIRTUAL EVENT, APRIL 11-12, 2023

JEDEC®

The Key Foundations and Future of Memory: Industry Standards

An overview of the latest standards and work of the JEDEC Solid State Technology Association

Presented by

Jonathan Hinkle, Distinguished Systems Architect for Storage, Micron

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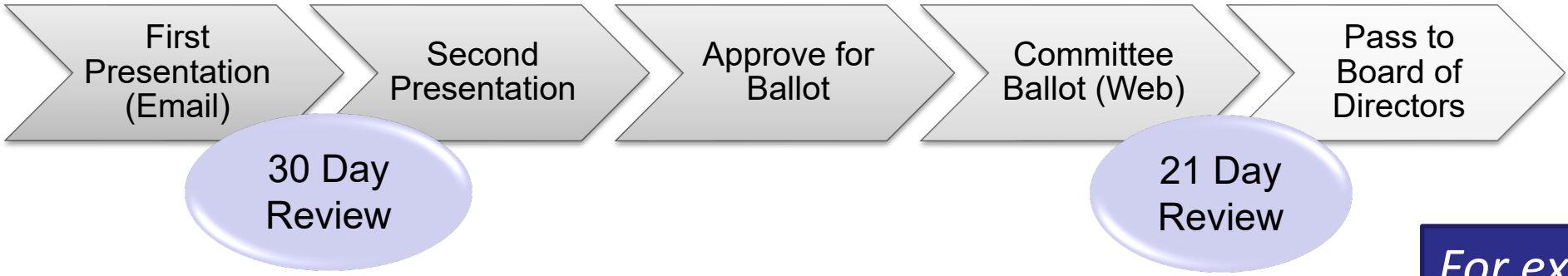
JEDEC: Global Industry Standards Leader

- **JEDEC** develops open standards for the microelectronics industry. They are adopted industry-wide and throughout the world, since the early 20th century.
  - JEDEC has published and maintains over 1,000 open standards and publications serving all industry segments
  - The JEDEC website tracked over 250,000 document downloads annually for the past many years
- Over 340 member companies worldwide, representing a large majority of total global semiconductor revenue.
- Over 3,000 volunteers working together in 100+ technical committees and task groups, but welcome all to join and participate in this critical work.
- JEDEC standards are available for download at www.jedec.org

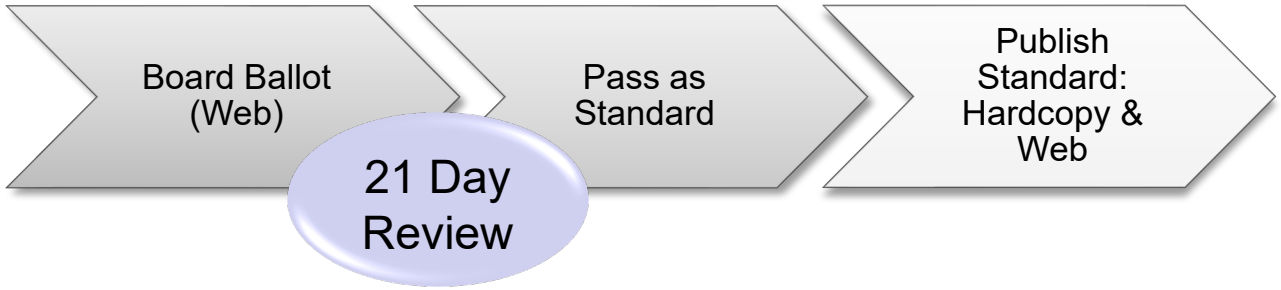
JEDEC Strengths Lay a Foundation for Success

Fast, Flexible Process

Committee

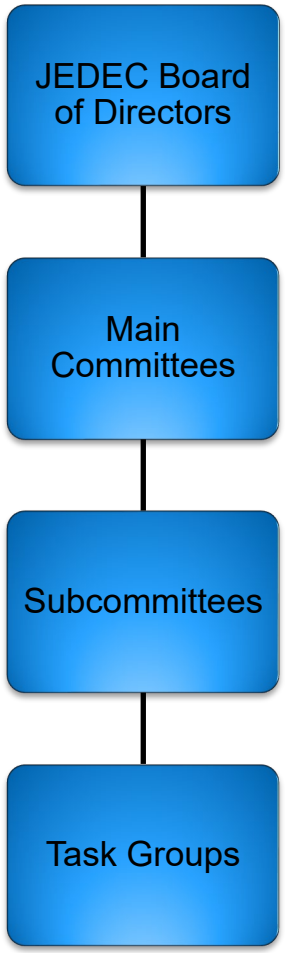


Board of Directors



For example:
9 month development cycle for the UFS Card Standard

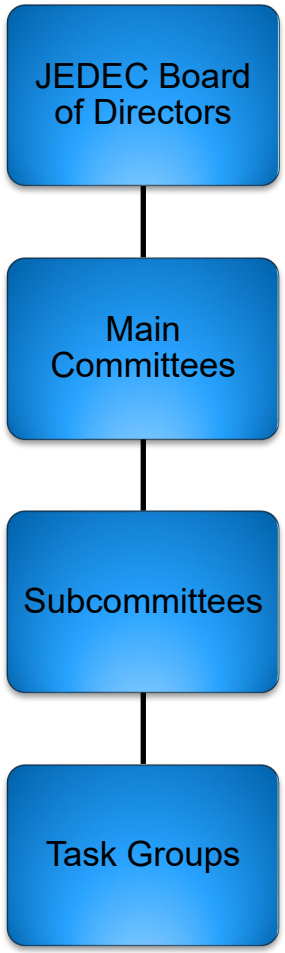
JEDEC Organizational Structure



Include:

JC-11 Mechanical Standardization
JC-13 Government Liaison
JC-14 Quality and Reliability
JC-16 Interface Technology
JC-40 Digital Logic
JC-42 Solid State Memories
JC-45 DRAM Modules
JC-63 Multiple Chip Packages
JC-64 Embedded Memory Storage & Removable Memory Cards
JC-70 Wide Bandgap Power Semiconductors

JEDEC Organizational Structure



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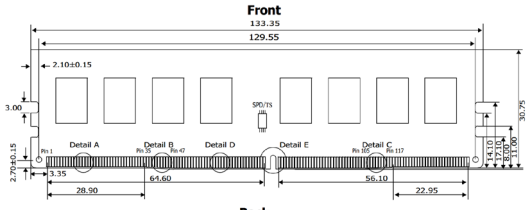
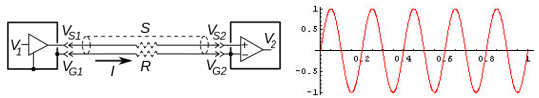


JC-11 Mechanical Standardization

JC-13 Government Liaison

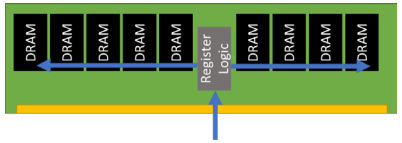
JC-14 Quality and Reliability



JC-16 Interface Technology

JC-40 Digital Logic

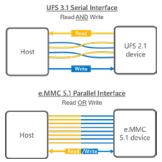
JC-42 Solid State Memories



JC-45 DRAM Modules

JC-63 Multiple Chip Packages

JC-64 Embedded Memory Storage & Removable Memory Cards



JC-70 Wide Bandgap Power Semiconductors

(memory-related committees)

A few recent, noteworthy standards

- DDR5 – Next generation performance memory
- LPDDR5 – Further improving low power memory performance
- CMM – The industry's first CXL Memory Module specification

DDR5 DRAM

Overview of System/Application Requirements for the Definition of DDR5

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Computing memory needs - DRAM

- The DRAM Market Anticipated to Surpass USD 221.67 Billion by 2030, with a CAGR of 9.2%.*

- Along with NAND Flash, DRAM is one of the two key commodity memories used universally worldwide in computing and electronics.

*Market Research Future (MRFR) - 2020

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What are the main use cases for DDR5 DRAM?

Client Systems - Personal Computers

Data Center

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Main Characteristic for DRAM - Performance

- Why use DRAM? **Performance**.
- To get data to the CPU as soon as possible, DDR DRAM is designed to provide data with **low latency** access.
- The CPU also keeps getting faster with increasing core counts, so need **high bandwidth** to move the data needed quickly to the cores that need it.

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Another critical factor for DRAM - Capacity

- DRAM capacity is also critical to computing systems – to make sure the data needed can be stored there.
- The larger the memory capacity, the more likely the Operating System will be able to keep the next needed data there instead of slow storage.
- Over the past many decades as fab process shrinks have made more space on the silicon, DRAM die density has consistently grown. With modern production facilities, DDR4 DRAM is currently able to achieve up to 16Gb per die.

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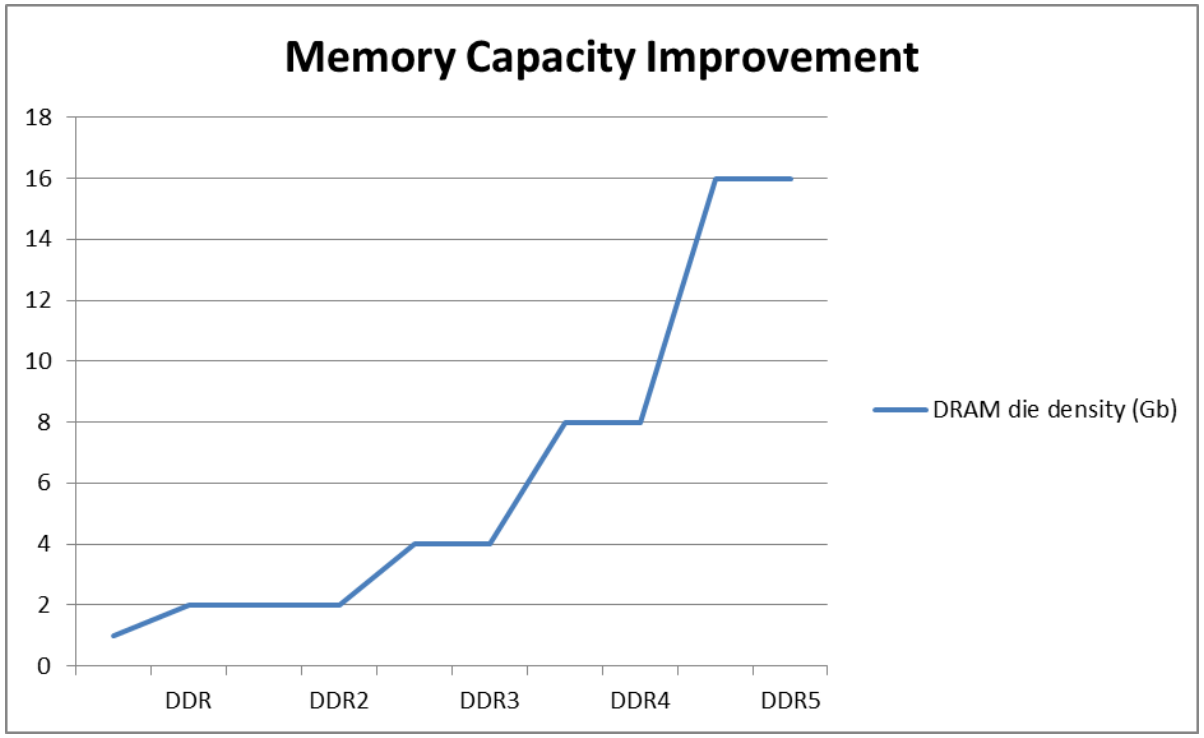
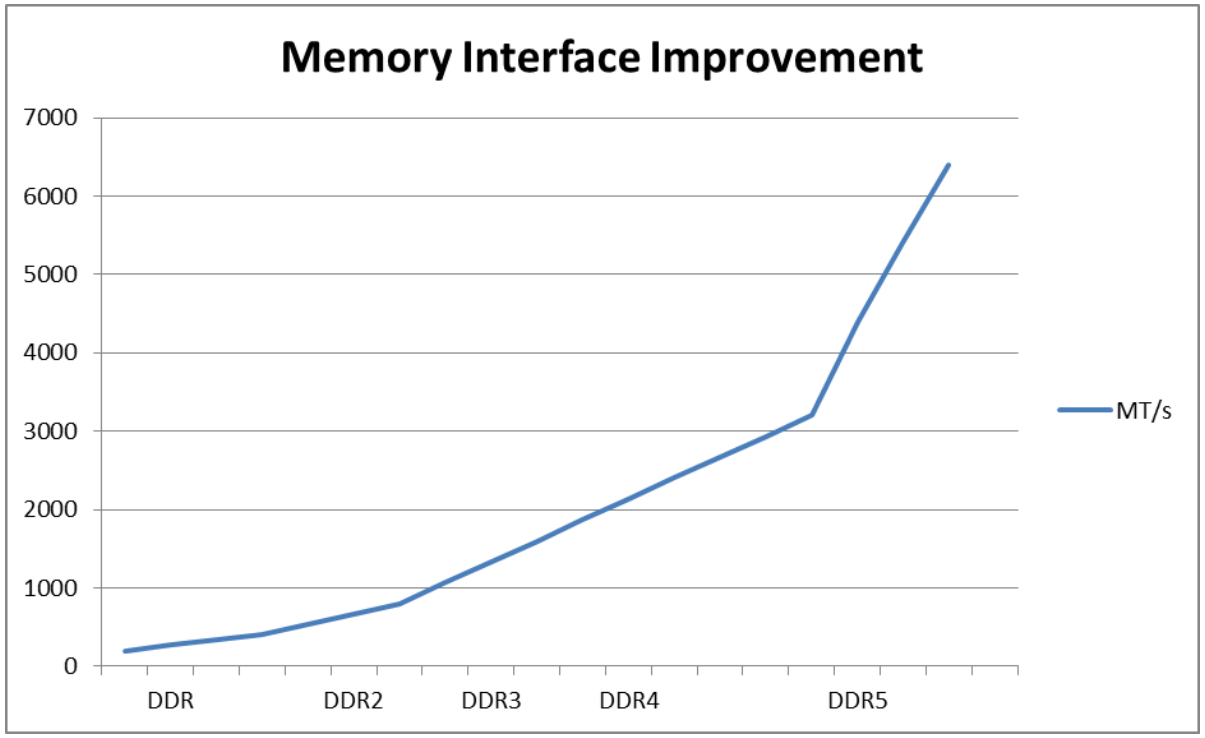
Evolution of DDR DRAM





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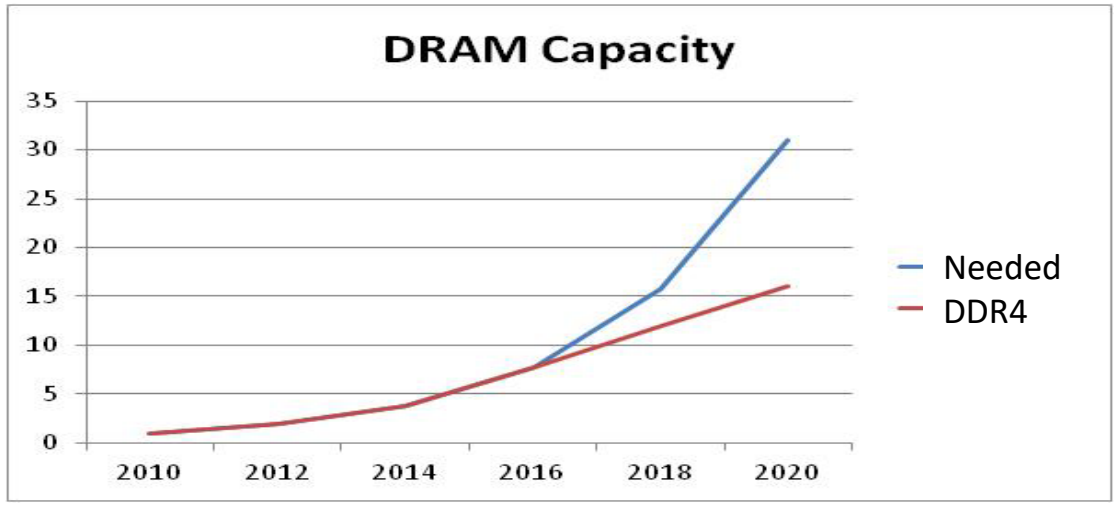
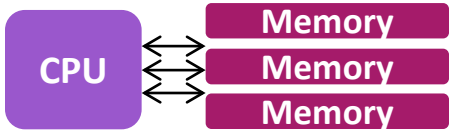
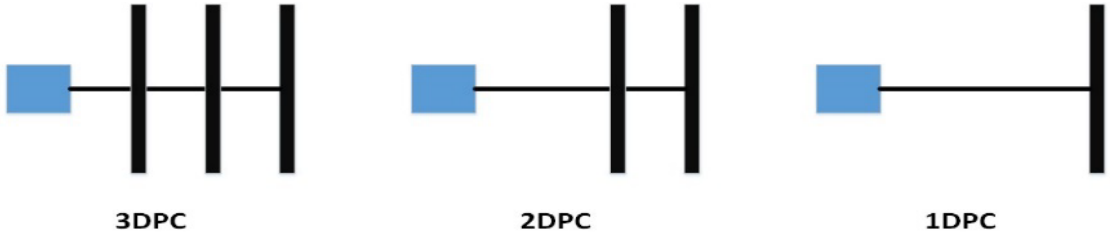
Challenges to continuing the trend

- System memory challenges have been met with new memory tech and through scaling improvements, but that is starting to slow. Without further scaling, memory capacity will not meet growth requirements.
- DDR4 interface utilization at higher data rates becomes highly inefficient.





Memory performance and capacity challenges



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Implications for Datacenter

- Without new technologies, systems won’t keep the current pace of improvement and significant value that can be extracted from the data will be lost.
- Considering very strong data growth and further rising numbers of users, Cloud and Enterprise could significantly miss meeting global IT needs.

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Implications for Client

- Without higher capacity DRAM devices, client devices would need more chips to satisfy growing capacity needs.
- Larger numbers of DRAM die in a client system for the same total memory capacity raises cost and power.
- Power has to reduce or stay low to maintain system battery life.

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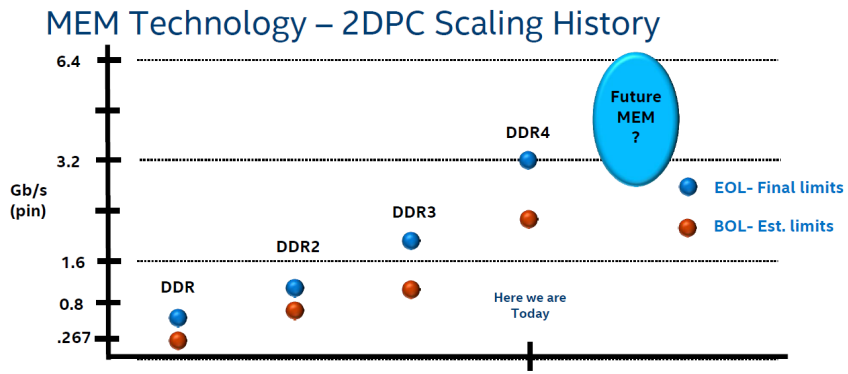
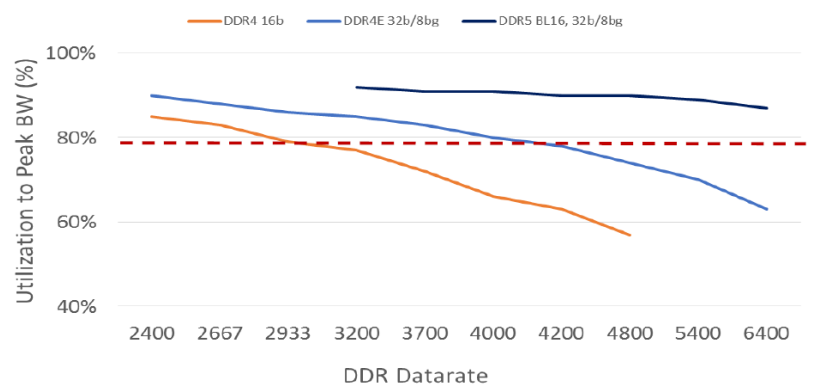
Just in time – enter DDR5

DDR5 enables:

- Higher Performance
  - Higher signaling rates – up to minimum of 6400 Mbps
  - Much improved memory channel utilization
- Scaling
  - On-die ECC allows for next process shrinks without driving higher cost
  - Core timing changes to improve design scaling
  - Higher die density enabling higher capacity at lower power





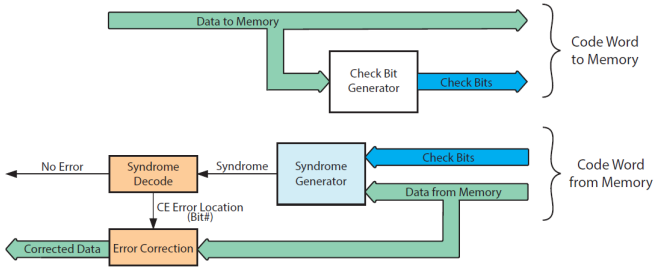
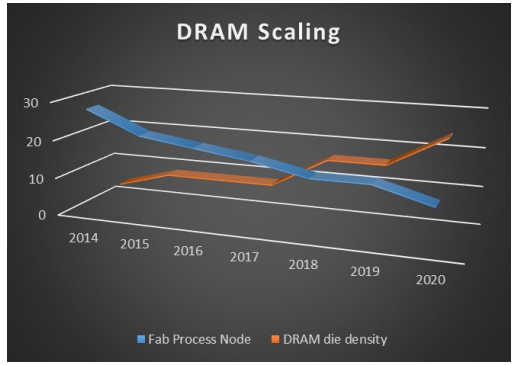


Figure 127 — On Die ECC Block Diagram



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DDR5 Adoption in Systems

- Now with DDR5, new systems can be developed that will continue to meet customer needs
- Future data center systems can further expand TBs of memory capacity while not sacrificing performance and satisfying processor data needs.
- Next generation client systems can become even more capable and become even more efficient.

- The industry is now in process of adopting DDR5 to enable the next generations of computing systems.

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Global Standards for the Microelectronics Industry

LPDDR5 brief overview

Special thanks to content creator:
Osamu Nagashima
Micron, MBU

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LPDDR – Low Power DRAM

- Key focus on meeting needs of mobile applications – smartphones, tablets and now some laptop PC
- LPDDR4 and now LPDDR5 are broadly successful, especially providing significantly lower idle power
- Usage and applications – 5G and multimedia applications continue to drive usage models & memory BW
- From LPDDR4 at speeds around 4266, LPDDR5 and extended spec variants now target >6400

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LPDDR5 Architecture

- Simplify Die Architecture
  - Only Single Channel configuration
    - No dual channel definition
- Rotated ball out concept for dual / quad channel PKG
- X16 and X8 are defined as native configuration
- Addressing are defined from 2Gb/die to 32Gb/die
- Lower power consumption
  - Lower VDD2 and VDDQ supply than LPDDR4
  - Dynamic Supply Voltage Control

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LPDDR5 Architecture

- Support various requirements
  - Flexible Architecture
    - Programable Bank organization
    - Byte mode and x16 mode
  - High reliability function
- High data rate friendly clocking system
  - Dual Clock for CA bus and DQ bus
- Low Power features
  - Reduce data transfer
  - Clocking power optimize

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LPDDR5 Architecture

- Flexible training schemes
  - QD training : FIFO, pre-programed
  - CA training : Consolidated CBT
  - Foreground / background ZQ calibration
- Support equivalent form factor as LPDDR4
  - POP
  - MCP
  - FBGA

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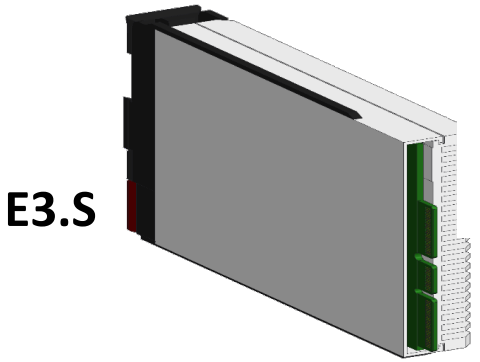
CXL Memory Module (CMM) Specification

- Industry aligned to define a few specific implementations of CXL-attached memory modules to enable systems to be designed for first adoption
- JEDEC formed the CXL Memory Module Task Group and has just published the industry's first CMM specification: JESD317
- The defined CMMs leverage SNIA-SFF EDSFF device form factors and align with defined NVMe drive pinout. JESD317 standard modules will support an CXL 2.0 interface with x4 and x8.
- The specification is available for download on the JEDEC website.



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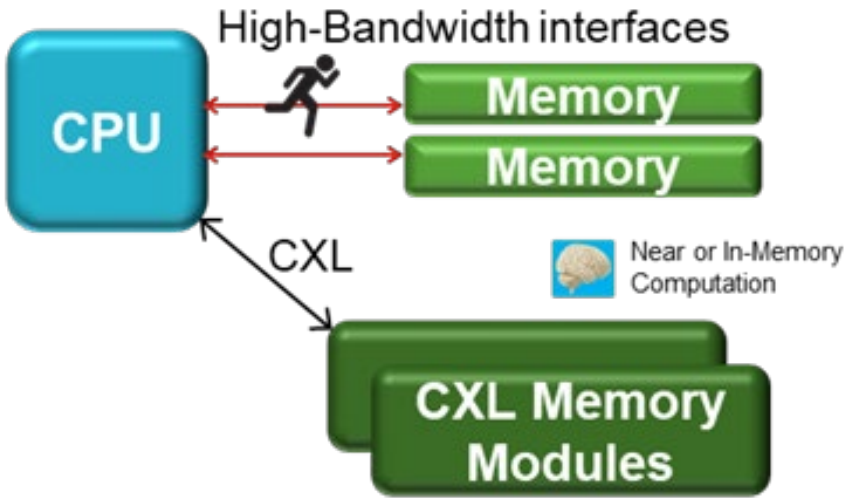
Upcoming work

- CXL Memory TG – further definition of CXL-attached memory standards
- PIM – processor in memory, near memory compute
- MRDIMM – High bandwidth DDR memory modules



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Thank you

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