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NVDIMM Technology Overview
NVDIMM’S

- Reside on the Memory Channel (DDR3/DDR4)
- Retain data in the event of an unexpected power loss
- Combine memory technologies (DRAM & Flash)
- Require independent power source to ensure main memory persistence.

- Fits well with the NVM Programming Model (as pre-cursor to SCM)
- Deliver new levels of Storage Performance
- Databases can Run Faster & Recover Quicker
- Can enhance both SSD endurance and reliability.
MEMORY/STORAGE HIERARCHY

- Data-Intensive Applications Need Fast Access To Storage
- Large Performance Gap Between Main Memory And HDD
- SSDs Have Narrowed The Gap, But a Big Gap Still Exists
- Until “The SCM” Emerges – Opportunity For Innovation!

![Memory Storage Hierarchy Diagram]

- CPU
- CACHE
- New Memory Technology
- SSD
- HDD

**Performance Gap**

- SRAM
- DRAM
- ReRAM/MRAM/PCM?
- NAND
- Magnetic

**ACCESS TIME (ns)**

- $10^0$
- $10^1$
- $10^2$
- $10^3$
- $10^4$
- $10^5$
- $10^6$
Benchmark: VDBENCH, Platform: Intel Sandybridge, Linux, Two DDR3-1333 NVDIMMs as interleaved pair (channel interleaving), PRAMFS vs. SATA SSD as Linux block device.
NVDIMM TECHNICAL COMPARISON

IOPS

<table>
<thead>
<tr>
<th>Memory Channel Storage (MCS)</th>
<th>150K IOPS - Random Read (4K)</th>
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<tbody>
<tr>
<td>PCIe SSD</td>
<td>785K IOPS - Random Read (4K)</td>
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<tr>
<td>2.5 in. SAS SSD</td>
<td>145K IOPS - Random Read (4K)</td>
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<tr>
<td></td>
<td>100K IOPS - Random Write (4K)</td>
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</tbody>
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Latency

10’s nano seconds Latency

10 microseconds Latency

68 microseconds Latency

110 microseconds Latency

• Is $/GB the right metric beyond HDD
• $/IOP or Cost per PB Written?

* PCIe & SAS SSD Latency & IOPS are averages from multiple vendors
NVDIMM SIG: SNIA-SSSI

NVDIMM SiG Formed

Organized under SNIA-SSSI to help:
• Accelerate awareness & Adoption of NVDIMMs
• Vendors collaborate to Broaden Industry Support & Knowledge

SNIA’s history of developing Standards & providing education:
• The NVM Programming Model / TWG
• Ideal venue for NVDIMM SiG Support

NVDIMM SiG will educate on:
• How system vendors can design in NVDIMM
• Communicate Industry Standards as they evolve
• Develop market understanding of NVDIMM Technology
• Communicate how New Programming models help deliver value
HIGH LEVEL SYSTEM CONSIDERATIONS

The “Pieces of the Puzzle” that are required for NVDIMM Integration

- System Management (Power Health)
- Application
- “NVDIMM – Aware” BIOS
- NVDIMM
- System Support H/W Trigger (ADR)
- Mechanical (Power Source)
ECOSYSTEM, STANDARDS & STATUS

JEDEC: DDR4 Pinout Definition (DRAM)
      DDR4 Optional 12V Power Pins (284 to 288-pin)
      Module Mechanical Outline

NVDIMM Modules: Multiple Vendor Support

NVDIMM Enabled Platforms: DDR3 – Limited OEM/ODM Support
                           DDR4 /Grantley – Widespread Support

BIOS: OEMs/ODMs: POR NVDIMM Support for Grantley

SW/OS/Application: In Process…

* Next Speaker to review Hyperscale/Megacloud NVDIMM Use Cases