SNIA SSSI PCIe SSD Round Table

Storage Developers Conference

Eden Kim, Chair
PCIe Solid State Storage - Higher Performance / Lower Latencies

Solid State Storage PCIe . . .

a Round Table

What are issues facing Adoption of PCIe Solid State Storage devices?

- Standards for PCIe Attached Storage
- Technology & Architectural Issues
- Mass Storage Ecosystem Adoption & Optimization
- Market & Product Positioning
- Deployment Strategies
Panelists

Moderator: Eden Kim, Calypso Systems, Inc.

11:20 – 11:30: Eden Kim, Calypso - Introduction

Speakers

11:30 – 11:40: Easen Ho, Calypso – PCIe Performance Testing

11:40 – 11:50: Marty Czekalski, Seagate – SCSI Express: Extending the SCSI Platform

11:50 – 12:00: Tony Roug, Virident – PCIe & Storage Class Memory

Question & Answer Session – 12:00 – 12:15

Audience Questions Please fill out Questionnaire Cards
SNIA SSSI PCIe SSD Task Force

Open Forum April – July 2012

- SSD OEMs ODMs
- Controller Companies
- Semiconductor Fabs
- VARs, SAN, NAS
- Analysts, Blogs
- Industry Associations
- Standards Groups
- End Users
SNIA SSSI PCIe SSD Task Force

8 MEETINGS  24 PRESENTATIONS

PRESENTING COMPANIES

HP - Marvell - Micron – Toshiba - Seagate
STEC - Fusion-io - Virident - Intel
NVMe - SATA-IO – STA - PCI SIG
Calypso – Agilent – HyperIO - LeCroy – eASIC
Coughlin Associates - Objective Analysis
SNIA IOTTA – NVMP – SSS - Security TWGs

TOPICS

• Standards
• Testing & Instrumentation
• PCIe Performance
• System Integration
• Form Factors
• System Architectures
• PCIe Driver Topics
• Analysts View
• Market Development
• Deployment Strategies

Presentations can be downloaded in mtg minutes at www.snia.org/forums/sssi/pcie
# PCIe SSD Standards

<table>
<thead>
<tr>
<th>ITEM</th>
<th>GROUP</th>
<th>STANDARD</th>
<th>CLIENT PCIe SSD</th>
<th>ENTERPRISE PCIe SSD</th>
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</thead>
<tbody>
<tr>
<td>PHYSICAL INTERFACE</td>
<td>PCI-SIG</td>
<td><strong>PCI Express</strong></td>
<td>up to 2 LANES Drive</td>
<td>Up to 4 LANES</td>
</tr>
<tr>
<td></td>
<td>SATA-IO</td>
<td><strong>SATA Express</strong></td>
<td>up to 4 LANES Card</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SCSI Trade Assn</td>
<td><strong>SCSI Express</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REGISTER INTERFACE &amp; COMMAND SET</td>
<td>Intel</td>
<td><strong>AHCI</strong></td>
<td></td>
<td>SOP / PQI</td>
</tr>
<tr>
<td></td>
<td>NVM Express Group</td>
<td><strong>NVMe</strong></td>
<td>AHCI or NVMe</td>
<td>Or SOP / NVMe</td>
</tr>
<tr>
<td></td>
<td>T10</td>
<td><strong>SOP/PQI w/support for NVMe</strong></td>
<td></td>
<td>Or NVMe</td>
</tr>
<tr>
<td>HOST CONNECTOR</td>
<td>SATA-IO</td>
<td><strong>SATA Express</strong></td>
<td>SATA Express</td>
<td>SFF-8639</td>
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<tr>
<td></td>
<td>SSD FF WG</td>
<td><strong>multifunction connector</strong></td>
<td>Host Connector</td>
<td></td>
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<tr>
<td></td>
<td>Small FF Committee</td>
<td><strong>SFF-8639</strong></td>
<td>Or SFF-8639</td>
<td></td>
</tr>
<tr>
<td>DEVICE CONNECTOR</td>
<td>SATA-IO</td>
<td><strong>SATA Express</strong></td>
<td>SATA Express</td>
<td>SFF-8639</td>
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<tr>
<td></td>
<td>SSD FF WG</td>
<td><strong>multifunction connector</strong></td>
<td>Drive &amp; Card Connectors</td>
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# Easen Ho, Calypso

<table>
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<tr>
<th>Speaker Name</th>
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<tbody>
<tr>
<td>Easen Ho</td>
<td>Calypso</td>
<td>Dr. Ho is the CTO of Calypso Systems, Inc. and has been a principal architect of the recently released SNIA Solid State Storage Performance Test Specification. Dr. Ho has been intimately involved in the development of performance benchmarking for NAND Flash based solid state storage devices. Dr. Ho received his doctorate in laser physics from MIT and his BSEE from the Tokyo Institute of Technology. Dr. Ho previously was founder, CEO and CTO of digital papyrus, inc., a laser optical mass storage technology firm.</td>
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PCIe SSD Roundtable

Testing of PCIe SSDs

Easen Ho
CTO, Calypso Systems, Inc.
From a testing perspective, PCIe SSDs looks just like another drive to the application, however…

- Generally targeted at high end → faster TP, IOPS, and latencies
- Wider variety of architectures possible:
  - no longer gated by a specific protocols such as SATA/SAS → possible to reduced IO latencies
  - host system can become part of the drive by design in some architectures → additional testing metrics needed; standardization becomes important
- Variety of form factors → heat dissipation; power measurement issues
- Variety of protocol standards → how do they affect performance?
RND/4K Writes: Minimum Response Time – Group By Classes

- PCIe
- SLC
- MLC
- HDD
SNIA PTS-E 1.0 IOPS: T2/Q16

P4 2D SS IOPS vs BS-RW

Steady State CPU_SYS vs BS & RW: T2/Q16
SNIA PTS-E 1.0 IOPS: T16/Q32

**Graph 1:**
- Title: P4 2D SS IOPS vs BS-RW
- Y-axis: IOPS (log scale)
- X-axis: Block Size (KIB)

**Graph 2:**
- Title: Steady State CPU_SYS vs BS & RW: T16/Q32
- Y-axis: % Utilization
- X-axis: Block Size (KIB)

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Flash Memory Summit 2012
Santa Clara, CA
### Panelist Marty Czekalski, Seagate

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<tr>
<td>Marty Czekalski</td>
<td>Seagate</td>
<td>Marty Czekalski brings over thirty years of senior engineering management experience in advanced architecture development for Storage and IO subsystem design, ASIC, and Solid State Storage Systems. He is currently Sr. Staff Program Manager within Seagate’s Strategic Planning and Development Group.</td>
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</table>
SAS is the preferred SSD Interface for Storage Systems

Storage-attached SSD Units

Thousands of Units

- PCIe
- SATA
- SAS 2.5"
- FC/SAS 3.5"

Forward-Insights 11-2011
Server Attached SSDs

Server-attached SSD Units


Categories: SATA IO, SAS IO, Boot Drive, PCIe

Forward-Insights 11-2011
Express Bay

- Up to 25 Watts
- SFF-8639 connector
- PCI-SIG electrical specification

Objectives
- Preserve the enterprise storage experience for PCI Express storage
- Meet SSD performance demands
- Serviceable, hot-pluggable Express Bay opens up new possibilities…
SCSI Express Overview

Proven SCSI protocol combined with PCIe creating an industry standard path to PCIe-based storage

- Enterprise storage for PCIe based storage devices
- Increased performance through lower latency
- Coexistence with SAS via Express Bay and common command set
- Unified management and programming interface

STA Member Companies
## SCSI Express Components

### Existing industry initiatives delivering enterprise storage using PCI Express

<table>
<thead>
<tr>
<th>Technology</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>SCSI</td>
<td>The storage command set</td>
</tr>
<tr>
<td>SCSI Over PCIe (SOP)</td>
<td>Packages SCSI for a PQI queuing layer</td>
</tr>
<tr>
<td>PCIe Queuing Interface (PQI)</td>
<td>Flexible, high-performance queuing layer</td>
</tr>
<tr>
<td>Express Bay connector (SFF 8639)</td>
<td>Accommodates PCIe, SAS, and SATA drives</td>
</tr>
<tr>
<td>PCI Express</td>
<td>Leading server I/O interconnect</td>
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Santa Clara, CA
Sept 2012
SCSI/SAS – Looking to the Future

- 12Gb/s, 24Gb/s SAS
- Extended Copy Feature
- Power Limit Control - up to 25W SAS devices
- Atomic Writes
- Hinting & other NVM features
- SCSI Express (SOP/PQI spec out for letter ballot)
So where do we go from here?

- SAS controllers > 1 Million IOPS and increased power for SAS drives diminish PCIe SSD differentiation
  - Standardized SAS solutions exist today and will continue to be deployed
  - Increased power in Express Bays allow SAS devices to achieve similar performance levels to PCIe devices
- PCIe SSD Storage Call to Action
  - Once the PCIe capable bays are available, any PCIe device can be packaged in a 2.5” FF and used, in as long as a driver exists.
    - SCSI Express, NVMe, proprietary, non-storage devices, etc.
  - Interoperability – Electrical spec for SFF-8639 (Express Bay) started
    - Compliance tests
  - Hot plug – work underway (DPC and enhanced DPC)
- New form factors will emerge
  - How will they effect the market?
Panelist Tony Rogue, Virident

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<td>Tony Rogue</td>
<td>Virident</td>
<td>Tony owns end-user datacenter solution architecture at Virident for cloud provider, web provider and enterprise customers including Viridents direction with solid state storage standards. Over the past six years, Tony has defined datacenter solutions based on next generation storage technology for datacenter end users. Tony’s focus in Virident is on proving the ROI value of how PCIe based solid state storage eliminates the performance bottleneck in datacenter deployments. Previously, Tony had been employed by Intel as a principal engineer for 12 years focusing on applications and technologies deployed by web and telecom services providers including Intel’s SSD products. Previous to Intel, Tony worked at Dialogic and AT&amp;T building and deploying technology with service providers and hosting companies. In addition Tony has worked with industry standards bodies including SNIA, T10, SPEC, TPC, ETSI, INForum and ECTF. Tony has an MS degree in computer engineering from Carnegie-Mellon University and a BS degree in computer engineering from Iowa State University.</td>
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<tr>
<td></td>
<td>Dir Solution Architecture</td>
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## Storage Class Memory (SCM) in Datacenter
New Layer In Storage Hierarchy

### Attribute Comparison

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Disk</th>
<th>SATA/SAS SSDs</th>
<th>PCIe SSD</th>
<th>Memory-class SCM</th>
<th>DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity (GB)</td>
<td>100’s - 1000’s</td>
<td>100’s</td>
<td>100’s – 1000’s</td>
<td>100’s-1000’s</td>
<td>10’s-100’s</td>
</tr>
<tr>
<td>Read performance</td>
<td>10’s ms, ~100 MB/s</td>
<td>100’s us, ~100’s MB/s</td>
<td>10’s us, 1’s GB/s</td>
<td>100’s ns, 1’s GB/s</td>
<td>~100 ns, 10’s GB/s</td>
</tr>
<tr>
<td>Write performance</td>
<td>10’s ms, ~100 MB/s</td>
<td>100’s us, ~100’s MB/s</td>
<td>~10’s us, ~1’s GB/s</td>
<td>1’s us, 1’s GB/s</td>
<td></td>
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PCIe SSDs established, Memory-class SCM emerging
Optimization required for applications to realize memory class benefit.
Storage Class Memory (SCM) in Datacenter: An industry activity mapping...

Industry agreement for optimized architecture in place
Thank you!
Questions for Q & A

Questions:

1. Please explain the roles of NVM and SOP/PQI – will SOP/PQI play on NVM? What is the future of the inter relationships of these, and other, specs?

2. What issues do you see needing to be solved before PCIe becomes a standard mass storage bus? Please comment on hot plugging, scatter gather, heat and performance and other issues.

3. What are some of the key issues facing test & qualification of PCIe Storage?

4. Please comment on the pros/cons of adding a Flash Translation Layer and its future impact to current system design architecture and performance.

5. PCIe SSDs already produce prodigious throughput which is usually measured in GB/s, and IOPs on the order of hundreds of thousands. With the advent of PCIe Gen3, that may double. How does one get all that performance to move outside of the system that houses the SSD and into the system requesting the data?
Thank You Very Much!